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(54) **ACTIVE MATRIX SUBSTRATE, LIQUID CRYSTAL DISPLAY PANEL, LIQUID CRYSTAL DISPLAY DEVICE, METHOD FOR MANUFACTURING ACTIVE MATRIX SUBSTRATE, METHOD FOR MANUFACTURING LIQUID CRYSTAL DISPLAY PANEL AND METHOD FOR DRIVING LIQUID CRYSTAL DISPLAY PANEL**

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SUBSTRAT DE MATRICE ACTIVE, PANNEAU D'AFFICHAGE À CRISTAUX LIQUIDES, DISPOSITIF D'AFFICHAGE À CRISTAUX LIQUIDES, PROCÉDÉ DE FABRICATION DE SUBSTRAT DE MATRICE ACTIVE, PROCÉDÉ DE FABRICATION DE PANNEAU D'AFFICHAGE À CRISTAUX LIQUIDES ET PROCÉDÉ DE COMMANDE D'AFFICHAGE À CRISTAUX LIQUIDES

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Description

Technical Field

[0001] The present invention relates to active matrix substrates, liquid crystal display panels, liquid crystal display devices, methods for manufacturing active matrix substrates, and methods for manufacturing liquid crystal display panels, in order to display an image by controlling the alignment of liquid crystal molecules and, in particular, to: an active matrix substrate, a liquid crystal display panel, and a liquid crystal display device, each of which is manufactured by a method including a PSA (polymer sustained alignment) treatment; a method for manufacturing an active matrix substrate and a method for manufacturing a liquid crystal display panel, each of which includes a PSA treatment; and a method for driving a liquid crystal display panel.

Background Art

[0002] In recent years, along with the popularization of information equipment, there has been a growing demand for higher levels of performance of display panels (liquid crystal display devices). In a liquid crystal display device, the passage and blockage of transmitted light is controlled by changing the direction of alignment of the liquid crystal molecules according to applied voltage. For the liquid crystal display device to have a higher level of performance, the state of alignment of the liquid crystal molecules in the absence of voltage being applied to the liquid crystals is important. Therefore, for a satisfactory state of alignment, it is necessary to control an initial formed angle (pretilt angle) between the liquid crystal layer and the liquid crystal molecules.

[0003] A known example of a method for controlling a pretilt angle is a technique disclosed in Patent Literature 1 listed below, i.e., a technique so called PSA. PSA is a technique by which the direction in which the liquid crystals lean is memorized by mixing polymerizable monomers into the liquid crystals and polymerizing the monomers with light, heat, or the like in the presence of voltage being applied to the liquid crystals. For example, first, a liquid crystal material containing monomers is injected into a cell obtained by so joining two substrates each provided with an alignment film to each other that the alignment films face each other. Then, the monomers are polymerized by irradiating them with ultraviolet rays with the liquid crystal molecules aligned along a predetermined direction, for example, by applying an electric field to the cell.

[0004] Thus formed on each of the alignment films is a polymer layer having a tilt. As a result, those liquid crystal molecules in contact with the polymer layer can be fixed with a pretilt angle given thereto. According to PSA, even a pixel structure that is weak in alignment controllability for the purpose of a larger aperture ratio or the like becomes faster in response speed and unlikely to suffer from a disturbance in liquid crystal alignment, for example, even when pressed with a finger.

[0005] Furthermore, at the step of aligning liquid crystal molecules according to PSA (such a step being hereinafter called "PSA step"), a method for applying voltage is important because when there is a variation in magnitude of voltage that is applied during ultraviolet irradiation, there occurs a difference in pretilt angle that leads to a variation in transmittance characteristic. For this reason, in Patent Literature 2 listed below, for example, there is proposed a method for manufacturing a liquid crystal display device through a PSA step under a scheme to avoid the influence of a defect in wiring by driving the liquid crystals through the use of a capacitor formed by AC application, i.e., under a Cs-COM voltage application scheme.

[0006] According to the method for manufacturing a liquid crystal display device described in Patent Literature 2, a first substrate is provided with a common electrode through which voltage is applied to the entire substrate, and a second substrate has gate bus lines and data bus lines disposed thereon in a matrix manner. Provided at an intersection between two bus lines are a thin-film transistor, a pixel electrode connected thereto, and a Cs bus line that forms a capacitor with the pixel electrode. Further provided in a space between the first and second substrates is a liquid crystal layer formed by filling the space with a liquid crystal composition containing a photosensitive material, with a capacitor formed by the common electrode and the pixel electrode with the liquid crystal layer sandwiched therebetween. Moreover, according to the method for manufacturing a liquid crystal display device described in Patent Literature 2, the liquid crystal layer is irradiated with light by applying AC voltage between the common electrode and the pixel electrode.

[0007] Thus, during application of voltage to the liquid crystals, the voltage is written by applying it between two common electrodes, instead of being written through a data bus line. This makes it possible to prevent a problem associated with a defective part made by a breakage or short circuit in a bus line during writing through the data bus line, i.e., to prevent such an obstacle that only the defective part shows a different level of brightness due to a pretilt angle formed in the defective part.

[0008] US 2007/211187 A1 discloses an MVA type liquid crystal display device including a pair of substrates disposed to be opposite to each other, a liquid crystal sealed between the pair of substrates, plural pixel areas each including a pixel electrode formed on one of the substrates and a pixel electrode separated from the pixel electrode, a TFT disposed in each of the pixel areas and including, a source electrode electrically connected to the pixel electrode, a linear projection formed on the other substrate and to regulate alignment of the liquid crystal, and a control capacitance section to capacity couple the source electrode and the pixel electrode and including a control capacitance electrode which is electrically connected to the source electrode is opposite to at least part

of the pixel electrode through an insulating film, and at least part of which is disposed to overlap with the linear projection when viewed perpendicularly to a substrate surface and extends along the linear projection.

Citation List

[0009]

Patent Literature 1
Japanese Patent Application Publication, Tokukai, No. 2003-149647 (Publication Date: May 21, 2003)
Patent Literature 2
Japanese Patent Application Publication, Tokukai, No. 2003-177408 (Publication Date: June 27, 2003)

Summary of Invention

Technical Problem

[0010] However, the configuration of Patent Literature 2 poses such a problem that the PSA step under the Cs-COM voltage application scheme causes a disturbance in alignment in a position where a pixel electrode slit and an auxiliary capacitor line cross each other.

[0011] In general, the alignment of liquid crystal molecules is controlled, for example, by providing a pixel electrode with a slit, and the alignment of liquid crystal molecules depends on equipotential surfaces that are formed when voltage is applied to the pixel electrode. That is, the inclination of liquid crystal molecules is controlled by the orientation of an electric field. At this time, in a region of intersection between the slit in the pixel electrode and the auxiliary capacitor line, there is a variation in orientation of the electric field due to the potential of the auxiliary capacitor line.

[0012] Fig. 9 shows those lines of electric force (indicated by arrows) and equipotential surfaces (indicated by dotted lines) in proximity to a slit between a pixel electrode provided with the slit and a counter substrate, (a) showing those lines of electric force and equipotential surfaces in a region where the slit does not intersect with an auxiliary capacitor line, (b) showing those lines of electric force and equipotential surfaces in a region of intersection between the slit intersects and an auxiliary capacitor line, with the auxiliary capacitor line being equal in potential to a COM potential, (c) showing those lines of electric force and equipotential surfaces in the region of intersection between the slit and the auxiliary capacitor line, with the auxiliary capacitor line being higher in potential than the COM potential.

[0013] See the case of those equipotential surfaces and lines of electric forces shown in (a) and (b) of Fig. 9. At respective ends of two pixel electrodes adjacent to each other with a space therebetween, there are lines of electric force inclined from the respective ends toward the center of the space. In this case, it is possible to align liquid crystal molecules along an appropriate direction as will be mentioned later. On the other hand, see the case of those equipotential surfaces and lines of electric forces shown in (c) of Fig. 9. At the respective ends of the two pixel electrodes, there are lines of electric force inclined from the vicinity of the center of the space to positions above the respective ends of the pixel electrodes in directions opposite to the lines of electric force of (b) of Fig. 9. In this case, it is impossible to align liquid crystal molecules along an appropriate direction as will be mentioned later.

[0014] Fig. 10 shows the appearance of a disturbance in alignment due to the PSA step under the Cs-COM voltage application scheme near a position where a pixel electrode slit and an auxiliary capacitor line cross each other. In Fig. 10, the white regions indicate regions of normal alignment, and the black stripe pattern indicates dark lines caused by the disturbance in alignment. Such a disturbance in alignment occurs when, at the PSA step under the Cs-COM voltage application scheme, a potential difference obtained by subtracting the potential of the common electrode (Vcom) from the potential of the auxiliary capacitor line (Vcs) is equal in polarity to a potential difference obtained by subtracting the potential of the common electrode (Vcom) from the potential of the pixel electrode (Vd) and the absolute value of a difference between the potential of the auxiliary capacitor line (Vcs) and the potential of the common electrode (Vcom) is greater than the absolute value of a difference between the potential of the pixel electrode (Vd) and the potential of the common electrode (Vcom) (i.e., when Vcs-Vcom is equal in polarity to Vd-Vcom and $|Vcs-Vcom|>|Vd-Vcom|$). In this case, the equipotential surfaces are shaped as shown in (c) of Fig. 9 under the influence of the potential of the auxiliary capacitor line below the slit; therefore, it is impossible to give an appropriate pretilt angle to the liquid crystal molecules. Moreover, such equipotential surfaces as those shown in (c) of Fig. 9 pose a further problem when the common electrode of the counter substrate is provided with a liquid crystal alignment control structure.

[0015] This problem is discussed in more detail below. Fig. 11 shows the appearance of alignment of liquid crystal molecules in a liquid crystal display device including an auxiliary capacitor line, a pixel electrode having a slit, and a common electrode having a projection, (a) showing the appearance of alignment of liquid crystal molecules during normal driving, (b) showing alignment of liquid crystal molecules as formed by the PSA step under the Cs-COM voltage application scheme. The projection provided on the common electrode is an alignment control structure for controlling the pretilt of liquid crystal molecules, as with the slit formed in the pixel electrode. It should be noted that the alignment control structure provided to the common electrode is not limited to the projection and may be a slit.

[0016] In the case of normal driving, as shown in (a) of Fig. 11, such voltage is applied to the common electrode, the pixel electrode, and the auxiliary capacitor line

that "Potential of Common Electrode (Vcom) = Potential of Auxiliary Capacitor Line (Vcs)". As a result, those equipotential lines in proximity to the slit provided in the pixel electrode are convex toward the auxiliary capacitor line (which corresponds to (b) of Fig. 9). In this case, those liquid crystals aligned near the projection provided on the common electrode and those liquid crystals aligned near the slit provided in the pixel electrode lean in the same direction, so that there occurs no disturbance in alignment. As a result, there appear no dark lines.

[0017] Meanwhile, at the PSA step under the Cs-COM voltage application scheme, as shown in (b) of Fig. 11, such voltage is applied to the common electrode, the pixel electrode, and the auxiliary capacitor line that Vcs-Vcom is equal in polarity to Vd-Vcom and that |Vcs-Vcom|>|Vd-Vcom|. As a result, those equipotential lines in proximity to the slit provided in the pixel electrode are convex toward the common electrode (which corresponds to (c) of Fig. 9) in a direction opposite to the case of normal driving. In this case, those liquid crystals aligned near the projection provided on the common electrode and those liquid crystals aligned near the slit provided in the pixel electrode lean in opposite directions, so that there occurs a disturbance in alignment. As a result, there appear such dark lines as those shown in Fig. 10.

[0018] That is, the PSA step under the Cs-COM voltage application scheme cannot form a pretilt angle unidirectionally within a single domain formed by aligning liquid crystal molecules along a predetermined direction within a single pixel.

[0019] Therefore, after the conventional PSA step, the pretilt angle is fixed in the state shown in (b) of Fig. 11, and the dark lines of Fig. 10 appear even during normal driving, thus ending up inviting deterioration in display quality.

[0020] Further, even during normal driving of a liquid crystal display device manufactured by a manufacturing method not including a PSA step, there occurs a disturbance in alignment of those liquid crystals in proximity to a slit provided in a pixel electrode and intersecting with an auxiliary capacitor line, when such voltage is applied to the auxiliary capacitor line that (Potential of Auxiliary Capacitor Line - Potential of Common Electrode) is equal in polarity to (Potential of Pixel Electrode - Potential of Common Electrode) and that Potential of Auxiliary Capacitor Line - Potential of Common Electrode | > |Potential of Pixel Electrode - Potential of Common Electrode|. After all, there appear such dark lines as those shown in Fig. 10.

[0021] Furthermore, when, in a liquid crystal display device having such a structure that a scanning signal line is disposed below a pixel electrode and a slit provided in the pixel electrode intersects with the scanning signal line, such voltage is applied to the scanning signal line that (Potential of Auxiliary Capacitor Line - Potential of Common Electrode) is equal in polarity to (Potential of Pixel Electrode - Potential of Common Electrode) and that |Potential of Auxiliary Capacitor Line - Potential of Common Electrode| > |Potential of Pixel Electrode - Potential of Common Electrode |, there occurs a disturbance in alignment of those liquid crystals in proximity to the slit provided in the pixel electrode and intersecting with the scanning signal line. After all, there appear such dark lines as those shown in Fig. 10.

[0022] The present invention has been made in view of the foregoing problems, and it is an object of the present invention to provide an active matrix substrate, a liquid crystal display panel, a liquid crystal display device, a method for manufacturing an active matrix substrate, a method for manufacturing a liquid crystal display panel, and a method for driving a liquid crystal display panel, each of which can achieve a high-quality display suppressing a disturbance in alignment of liquid crystals.

Solution to Problem

[0023] The above objects are solved by the claimed matter according to the independent claims.

[0024] In order to solve the foregoing problems, an active matrix substrate according to the present invention is an active matrix substrate including: a plurality of scanning signal lines; a plurality of signal wires disposed in such a way as to intersect with the scanning signal lines; a pixel section constituted by pixel electrode sections each provided in correspondence with a combination of each of the scanning signal lines and each of the signal wires, the pixel section having an alignment control space section that controls a state of alignment of liquid crystal molecules; a switching element that switches a signal wire as one of the signal wires and a pixel electrode section as one of the pixel electrode sections into a conducting state or a non-conducting state in accordance with a scanning signal supplied from a scanning signal line as one of the scanning signal lines; a metal wire, connected to the switching element, through which when the switching element is in a conducting state, a data signal from the signal wire is supplied to the pixel electrode section; and an auxiliary capacitor line that forms a capacitor with the pixel electrode section, in a region of intersection between the alignment control space section and the auxiliary capacitor line or the scanning signal line, a metal layer being provided between a layer of the pixel section and a layer of the scanning signal line in such a way as to cover at least the auxiliary capacitor line or the scanning signal line.

[0025] According to the foregoing configuration, the active matrix substrate includes: a plurality of scanning signal lines; a plurality of signal wires disposed in such a way as to intersect with the scanning signal lines; a pixel section constituted by pixel electrode sections each provided in correspondence with a combination of each of the scanning signal lines and each of the signal wires, the pixel section having an alignment control space section that controls a state of alignment of liquid crystal molecules.

[0026] The pixel electrode sections may each be constituted by a single pixel electrode or a plurality of subpixel electrodes. Further, the pixel section corresponds to the group of pixel electrode sections provided at the points of intersection between the scanning signal lines and the signal wires. Moreover, the pixel section has, as an alignment control space section that changes a state of alignment of liquid crystal molecules, an ordinary slit or a fine slit provided in each of the pixel electrodes constituting the pixel electrode sections. Alternatively, the pixel section may have as an alignment control space section a space between pixel electrode sections constituting the pixel section.

[0027] Further, according to the foregoing configuration, the active matrix substrate includes: a switching element that switches a signal wire as one of the signal wires and a pixel electrode section as one of the pixel electrode sections into a conducting state or a non-conducting state in accordance with a scanning signal supplied from a scanning signal line as one of the scanning signal lines; a metal wire, connected to the switching element, through which when the switching element is in a conducting state, a data signal from the signal wire is supplied to the pixel electrode section; and an auxiliary capacitor line that forms a capacitor with the pixel electrode section.

[0028] The switching element is constituted, for example, by a TFT, and each of the pixel electrode sections has such a switching element provided between the pixel electrode section and the signal wire. The switching element carries out switching in accordance with a signal from the scanning signal line to switch the electrical connection between the pixel electrode section and the signal wire, i.e., to switch the pixel electrode section and the signal wire between a conducting state and a non-conducting state. The switching element is electrically connected to the pixel electrode section through the metal wire and, in a conducting state, a voltage corresponding to a data signal from the signal wire is supplied to the pixel electrode section. The metal wire is constituted, for example, as a drain line extending from the drain electrode of the TFT. Furthermore, the auxiliary capacitor line is provided to form a capacitor with the pixel electrode section.

[0029] Moreover, according to the foregoing configuration, in a region of intersection between the alignment control space section and the auxiliary capacitor line or the scanning signal line, a metal layer is provided between a layer of the pixel section and a layer of the auxiliary capacitor line or of the scanning signal line in such a way as to cover at least the auxiliary capacitor line or the scanning signal lines. Examples of the metal layer include the metal wire extending from the drain electrode, the signal wire, an intermediate electrode, or a shield metal formed totally independently. The term "intermediate electrode" here means an electrode, connected to a pixel electrode through a contact hole, which is equal in potential to the pixel electrode.

[0030] Conventionally, in the case of manufacture of a liquid crystal display panel having a liquid crystal layer provided between an active matrix substrate and a counter substrate, a PSA step may be carried out to form a pretilt angle of liquid crystal molecules. However, in a liquid crystal display panel including an auxiliary capacitor line, such relationships hold during the PSA step that (Potential of Auxiliary Capacitor Line - Potential of Common Electrode) is equal in polarity to (Potential of Pixel Electrode - Potential of Common Electrode) and that |Potential of Auxiliary Capacitor Line - Potential of Common Electrode | > |Potential of Pixel Electrode - Potential of Common Electrode|; therefore, due to the influence of those equipotential surfaces formed in an area of the liquid crystal layer around the alignment control space section, there occurs a defect in alignment of liquid crystal molecules, and the defect in alignment causes deterioration in display quality.

[0031] Further, conventionally, when, during normal driving of a liquid crystal display device having an intersection between an alignment control space section and an auxiliary capacitor line (or a scanning signal line), as well as a liquid crystal display device subjected to the PSA step, such voltage is applied to the auxiliary capacitor line (or the scanning signal line) that (Potential of Auxiliary Capacitor Line (or Scanning Signal Line) - Potential of Common Electrode) is equal in polarity to (Potential of Pixel Electrode - Potential of Common Electrode) and that |Potential of Auxiliary Capacitor Line (or Scanning Signal Line) - Potential of Common Electrode| > |Potential of Pixel Electrode - Potential of Common Electrode|, there occurs a disturbance in alignment of an area of the liquid crystal layer around the alignment control space section intersecting with the auxiliary capacitor line (or the scanning signal line) and, after all, the disturbance in alignment causes deterioration in display quality.

[0032] On the other hand, the active matrix substrate of the present invention thus configured allows at least the auxiliary capacitor line or the scanning signal line to be covered by the metal layer so that there is no direct overlap between (i) the open region of the alignment control space section, i.e., of a slit or of a space between pixel electrodes and (ii) the auxiliary capacitor line or the scanning signal line.

[0033] Such a configuration allows the potential of the metal layer to be set during the PSA step or during normal driving, for example, to form any one of the following states of potential: a first state of potential where a potential difference obtained by subtracting the potential of the common electrode from the potential of the metal layer is opposite in polarity to a potential difference obtained by subtracting the potential of the common electrode from the potential of the pixel electrode; a second state of potential where the potential of the metal layer is equal to the potential of the common electrode; and a third state of potential where the potential difference obtained by subtracting the potential of the common elec-

trode from the potential of the metal layer is equal in polarity to the potential difference obtained by subtracting the potential of the common electrode from the potential of the pixel electrode section and where the absolute value of a difference between the potential of the pixel electrode section and the potential of the common electrode is greater than or equal to the absolute value of a difference between the potential of the metal layer and the potential of the common electrode.

[0034] Thus, in the region of intersection between the alignment control space section and the auxiliary capacitor line (or the scanning signal line), the metal layer whose potential has been set to form the first, second, or third state of potential is placed between the layer of the auxiliary capacitor line (or of the scanning signal line) and the layer of the pixel electrode; therefore, the influence of the potential of the auxiliary capacitor line (or of the scanning signal line) during the PSA step or during normal driving can be blocked.

[0035] Therefore, the active matrix substrate according the present invention makes it possible, during manufacture of a liquid crystal display panel, to keep the alignment of liquid crystal molecules good and align the liquid crystal molecules appropriately, with no influence on the alignment of the liquid crystal molecules by those equipotential surfaces formed in an area of the liquid crystal layer around the alignment control space section intersecting with the auxiliary capacitor line (or the scanning signal line), thus bringing about an effect of achieving an improvement in display quality of the liquid crystal display panel.

[0036] Further, a method according to the present invention for manufacturing an active matrix substrate is a method for manufacturing an active matrix substrate including (i) a plurality of scanning signal lines, (ii) a plurality of signal wires disposed in such a way as to intersect with the scanning signal lines, (iii) a pixel section constituted by pixel electrode sections each provided in correspondence with a combination of each of the scanning signal lines and each of the signal wires, the pixel section having an alignment control space section that controls a state of alignment of liquid crystal molecules, (iv) a switching element that switches a signal wire as one of the signal wires and a pixel electrode section as one of the pixel electrode section into a conducting state or a non-conducting state in accordance with a scanning signal supplied from a scanning signal line as one of the scanning signal lines, (v) a metal wire, connected to the switching element, through which when the switching element is in a conducting state, a data signal from the signal wire is supplied to the pixel electrode section, and (vi) an auxiliary capacitor line that forms a capacitor with the pixel electrode section, the method including the step of, in a region of intersection between the alignment control space section and the auxiliary capacitor line or the scanning signal line, forming a metal layer in such a way that the metal layer covers at least the auxiliary capacitor line or the scanning signal line.

[0037] The foregoing configuration brings about the same effects as an active matrix substrate according to the present invention.

[0038] In order to solve the foregoing problems, an active matrix substrate according to the present invention is an active matrix substrate including: a plurality of scanning signal lines; a plurality of signal wires disposed in such a way as to intersect with the scanning signal lines; a pixel section constituted by pixel electrode sections each provided in correspondence with a combination of each of the scanning signal lines and each of the signal wires, the pixel section having an alignment control space section that controls a state of alignment of liquid crystal molecules; a switching element that switches a signal wire as one of the signal wires and a pixel electrode section as one of the pixel electrode sections into a conducting state or a non-conducting state in accordance with a scanning signal supplied from a scanning signal line as one of the scanning signal lines; and a metal wire, connected to the switching element, through which when the switching element is in a conducting state, a data signal from the signal wire is supplied to the pixel electrode section, in a region of intersection between the alignment control space section and the scanning signal line, a metal layer being provided between a layer of the pixel section and a layer of the scanning signal line in such a way as to cover at least the scanning signal line.

[0039] According to the foregoing configuration, the active matrix substrate includes: a plurality of scanning signal lines; a plurality of signal wires disposed in such a way as to intersect with the scanning signal lines; a pixel section constituted by pixel electrode sections each provided in correspondence with a combination of each of the scanning signal lines and each of the signal wires, the pixel section having an alignment control space section that controls a state of alignment of liquid crystal molecules.

[0040] The pixel electrode sections may each be constituted by a single pixel electrode or a plurality of subpixel electrodes. Further, the pixel section corresponds to the group of pixel electrode sections provided at the points of intersection between the scanning signal lines and the signal wires. Moreover, the pixel section has, as an alignment control space section that changes a state of alignment of liquid crystal molecules, an ordinary slit or a fine slit provided in each of the pixel electrode sections constituting the pixel section. Alternatively, the pixel section may have as an alignment control space section a space between pixel electrode sections constituting the pixel section.

[0041] Further, according to the foregoing configuration, the active matrix substrate includes: a switching element that switches a signal wire as one of the signal wires and a pixel electrode section as one of the pixel electrode sections into a conducting state or a non-conducting state in accordance with a scanning signal supplied from a scanning signal line as one of the scanning signal lines; and a metal wire, connected to the switching

element, through which when the switching element is in a conducting state, a data signal from the signal wire is supplied to the pixel electrode section.

[0042] The switching element is constituted, for example, by a TFT, and each of the pixel electrode sections has such a switching element provided between the pixel electrode section and the signal wire. The switching element carries out switching in accordance with a signal from the scanning signal line to switch the electrical connection between the pixel electrode section and the signal wire, i.e., to switch the pixel electrode section and the signal wire between a conducting state and a non-conducting state. The switching element is electrically connected to the pixel electrode section through the metal wire and, in a conducting state, a voltage corresponding to a data signal from the signal wire is supplied to the pixel electrode section. The metal wire is constituted, for example, as a drain line extending from the drain electrode of the TFT.

[0043] Moreover, according to the foregoing configuration, in a region of intersection between the alignment control space section and the scanning signal line, a metal layer is provided between a layer of the pixel section and a layer of the scanning signal line in such a way as to cover at least the scanning signal line. Examples of the metal layer include the metal wire extending from the drain electrode, the signal wire, an intermediate electrode, or a shield metal formed totally independently.

[0044] Conventionally, when, during normal driving or manufacturing process of a liquid crystal display device having an intersection between an alignment control space section and a scanning signal line, such voltage is applied to the scanning signal line that (Potential of Scanning Signal Line - Potential of Common Electrode) is equal in polarity to (Potential of Pixel Electrode - Potential of Common Electrode) and that |Potential of Scanning Signal Line - Potential of Common Electrode| > |Potential of Pixel Electrode - Potential of Common Electrode|, there occurs a disturbance in alignment of an area of the liquid crystal layer around the alignment control space section intersecting with the scanning signal line, and the disturbance in alignment causes deterioration in display quality.

[0045] On the other hand, the active matrix substrate of the present invention thus configured allows at least the scanning signal line to be covered by the metal layer so that there is no direct overlap between (i) the open region of the alignment control space section, i.e., of a slit or of a space between pixel electrodes and (ii) the scanning signal line. This metal layer is a metal layer whose potential can be set, for example, to form a first state of potential where a potential difference obtained by subtracting the potential of the common electrode from the potential of the metal layer is opposite in polarity to a potential difference obtained by subtracting the potential of the common electrode from the potential of the pixel electrode; a second state of potential where the potential of the metal layer is equal to the potential of the common electrode; or a third state of potential where the potential difference obtained by subtracting the potential of the common electrode from the potential of the metal layer is equal in polarity to the potential difference obtained by subtracting the potential of the common electrode from the potential of the pixel electrode section and where the absolute value of a difference between the potential of the pixel electrode section and the potential of the common electrode is greater than or equal to the absolute value of a difference between the potential of the metal layer and the potential of the common electrode.

[0046] Thus, in the region of intersection between the alignment control space section and the scanning signal line, the metal layer whose potential has been set to form the first, second, or third state of potential is placed between the layer of the scanning signal line and the layer of the pixel electrode; therefore, the influence of the potential of the scanning signal line can be blocked.

[0047] Therefore, the active matrix substrate according the present invention makes it possible, during manufacture of a liquid crystal display panel, to keep the alignment of liquid crystal molecules good and align the liquid crystal molecules appropriately, with no influence on the alignment of the liquid crystal molecules by those equipotential surfaces formed in an area of the liquid crystal layer around the alignment control space section intersecting with the scanning signal line, thus bringing about an effect of achieving an improvement in display quality of the liquid crystal display panel.

[0048] Further, a method according to the present invention for manufacturing an active matrix substrate is a method for manufacturing an active matrix substrate including (i) a plurality of scanning signal lines, (ii) a plurality of signal wires disposed in such a way as to intersect with the scanning signal lines, (iii) a pixel section constituted by pixel electrode sections each provided in correspondence with a combination of each of the scanning signal lines and each of the signal wires, the pixel section having an alignment control space section that controls a state of alignment of liquid crystal molecules, (iv) a switching element that switches a signal wire as one of the signal wires and a pixel electrode section as one of the pixel electrode sections into a conducting state or a non-conducting state in accordance with a scanning signal supplied from a scanning signal line as one of the scanning signal lines, and (v) a metal wire, connected to the switching element, through which when the switching element is in a conducting state, a data signal from the signal wire is supplied to the pixel electrode section, the method including the step of, in a region of intersection between the alignment control space section and the scanning signal line, forming a metal layer between a layer of the pixel section and a layer of the scanning signal line in such a way that the metal layer covers at least the scanning signal line.

[0049] The foregoing configuration brings about the same effects as an active matrix substrate according to

the present invention.

[0050] Further, the active matrix substrate according to the present invention is preferably configured such that the metal layer is constituted to include at least either the metal wire or the signal wire.

[0051] The foregoing configuration makes it possible to concurrently form the metal layer in the manufacturing step of forming the metal wire or the signal wire.

[0052] This makes it possible to form the metal layer without an increase in the number of manufacturing steps, thus bringing down manufacturing costs.

[0053] Further, the active matrix substrate according to the present invention is preferably configured such that the alignment control space section is a long narrow hole formed individually in the pixel electrode section.

[0054] Further, the active matrix substrate according to the present invention is preferably configured such that the alignment control space section is a space formed between one and another of the plurality of pixel electrode sections constituting the pixel section.

[0055] Further, the active matrix substrate according to the present invention is preferably configured such that the alignment control space section is a long narrow hole formed by making a cut in the pixel electrode section.

[0056] Further, the active matrix substrate according to the present invention is preferably configured such that the pixel electrode section is a multi-pixel electrode including a plurality of subpixel electrodes and is driven by a pixel division method.

[0057] According to the foregoing configuration, the pixel electrode section is a multi-pixel electrode composed of a plurality of subpixel electrodes and is driven by a pixel division method.

[0058] This makes it possible to express a halftone by composing each pixel of a high-luminance subpixel and a low-luminance subpixel, thus improving the dependence of gamma characteristics on viewing angles (e.g., excess brightness). Moreover, the provision of the active matrix substrate makes it possible to prevent a defect in alignment in the region of intersection between the alignment control space section and the auxiliary capacitor line during the PSA step and actual driving, so that there is no deterioration in display quality.

[0059] Further, the active matrix substrate according to the present invention is preferably configured such that in the region of intersection between the alignment control space section and the auxiliary capacitor line, a drain line serving as the metal wire and extending from the switching element formed in a corner portion of the pixel electrode section to the auxiliary capacitor line disposed in such a way as to pass transversely across the pixel electrode section is provided with a covering section that covers at least the auxiliary capacitor line.

[0060] Further, the active matrix substrate according to the present invention is preferably configured such that: the scanning signal line is disposed in such a way as to pass transversely across the pixel electrode section; the auxiliary capacitor line is disposed in such a way as to pass transversely across the pixel electrode section substantially in parallel with the scanning signal line; a drain line serving as the metal wire extends from the switching element formed in the pixel electrode section to at least either the region of intersection between the alignment control space section and the auxiliary capacitor line disposed in such a way as to pass transversely across the pixel electrode section or the region of intersection between the alignment control space section and the scanning signal line; and a covering section that covers at least the auxiliary capacitor line and the scanning signal line in the respective regions is provided as part of the drain line.

[0061] Further, the active matrix substrate according to the present invention is preferably configured such that: the scanning signal line is disposed in such a way as to pass transversely along an edge of the pixel electrode section; the auxiliary capacitor line is disposed in such a way as to pass transversely across a center of the pixel electrode section substantially in parallel with the scanning signal line; and a drain line serving as the metal wire and extending from the switching element formed in a corner portion of the pixel electrode section to at least either the region of intersection between the alignment control space section and the auxiliary capacitor line disposed in such a way as to pass transversely across the pixel electrode section or the region of intersection between the alignment control space section and the scanning signal line is provided with a covering section that covers at least the auxiliary capacitor line and the scanning signal line in the respective regions.

[0062] Further, the active matrix substrate according to the present invention is preferably configured such that: the scanning signal line is disposed in such a way as to pass transversely across a center of the pixel electrode section; the auxiliary capacitor line is disposed in such a way as to pass transversely along an edge of the pixel electrode section substantially in parallel with the scanning signal line; and a drain line serving as the metal wire and extending from the switching element formed in a side edge portion of the pixel electrode section to at least either the region of intersection between the alignment control space section and the auxiliary capacitor line disposed in such a way as to pass transversely across the pixel electrode section or the region of intersection between the alignment control space section and the scanning signal line is provided with a covering section that covers at least the auxiliary capacitor line and the scanning signal line in the respective regions.

[0063] Further, the active matrix substrate according to the present invention is preferably configured such that the pixel electrode section has its longer sides extending substantially in parallel with the scanning signal line.

[0064] Further, the active matrix substrate according to the present invention is preferably configured such that: the auxiliary capacitor line is provided in such a way as to overlap a site where another alignment control space section adjoining the alignment control space sec-

tion within each of the pixel electrode sections are close to the alignment control space section at a sharp angle; and in the region of intersection between the auxiliary capacitor line and those of the other alignment control space section and the alignment control space section, a drain line serving as the metal wire and extending from the switching element formed in a corner portion of the pixel electrode section to the auxiliary capacitor line is provided with a covering section that covers at least the auxiliary capacitor line.

[0065] Further, the active matrix substrate according to the present invention is preferably configured such that: the auxiliary capacitor line is provided in such a way as to pass transversely across the alignment control space section formed as a space between the plurality of pixel electrode sections; and in the region of intersection between the alignment control space section and the auxiliary capacitor line, a drain line serving as the metal wire and extending from the switching element formed in a corner portion of the pixel electrode section to the auxiliary capacitor line is provided with a covering section that covers at least the auxiliary capacitor line.

[0066] Further, the active matrix substrate according to the present invention is preferably configured such that: the auxiliary capacitor line is provided in such a way as to pass transversely across the alignment control space section formed as a space between the plurality of pixel electrode sections; and in the region of intersection between the alignment control space section and the auxiliary capacitor line, a data signal line serving as the signal line and extending from the switching element formed in a corner portion of the pixel electrode section in such a way as to intersect with the auxiliary capacitor line is provided with a covering section that covers at least the auxiliary capacitor line.

[0067] Further, the active matrix substrate according to the present invention is preferably configured such that in the region of intersection between the alignment control space section and the scanning signal line, a drain line serving as the metal wire and extending from the switching element formed in the pixel electrode section to the scanning signal line disposed in such a way as to pass transversely across the pixel electrode section is provided with a covering section that covers at least the scanning signal line.

[0068] A liquid crystal display panel according to the present invention includes: such an active matrix substrate as described above; a counter substrate provided with a common electrode; and a liquid crystal layer sandwiched between the active matrix substrate and the counter substrate.

[0069] According to the foregoing configuration, the active matrix substrate can block the influence of the potential of the scanning signal line or of the auxiliary capacitor line in the region of intersection between the alignment control section and the scanning signal line or the auxiliary capacitor line during normal driving or at the PSA step in the process of manufacture. This makes it possible to keep the alignment of liquid crystal molecules good and align the liquid crystal molecules appropriately, thus making it possible to achieve a liquid crystal display panel of high display quality.

[0070] The liquid crystal display panel according to the present invention is preferably configured such that the counter substrate includes an alignment control section that controls a state of alignment of liquid crystal molecules.

[0071] In the liquid crystal display panel thus configured, the counter substrate includes an alignment control section. The alignment control section may be, but is not particularly limited to, a rib or a slit.

[0072] This allows the alignment of liquid crystal molecules within the liquid crystal layer to be controlled, i.e., the liquid crystal molecules to be given a desired alignment. Moreover, the provision of the active matrix substrate makes it possible to prevent a defect in alignment in the region of intersection between the alignment control space section and the scanning signal line or the auxiliary capacitor line during normal driving, at the PSA step in the process of manufacture, etc., so that there is no deterioration in display quality.

[0073] A liquid crystal display device according to the present invention includes: such a liquid crystal display panel as described above; and a driving circuit that drives the liquid crystal display panel.

[0074] According to the foregoing configuration, the active matrix substrate can block the influence of the potential of the scanning signal line or of the auxiliary capacitor line in the region of intersection between the alignment control section and the scanning signal line or the auxiliary capacitor line during normal driving or at the PSA step in the process of manufacture. This makes it possible to keep the alignment of liquid crystal molecules good and give an appropriate pretilt angle to the liquid crystal molecules, thus making it possible to achieve a liquid crystal display device of high display quality.

[0075] A method according to the present invention for manufacturing a liquid crystal display panel is a method for manufacturing such a liquid crystal display panel as described above, the method preferably including a polymer alignment supporting step of giving a pretilt angle to liquid crystal molecules of the liquid crystal layer by polymerizing monomers mixed in advance into the liquid crystal layer, with voltage being applied to the liquid crystal layer in any one of the following states of potential: a first state of potential where a potential difference obtained by subtracting a potential of the common electrode from a potential of the metal layer is opposite in polarity to a potential difference obtained by subtracting the potential of the common electrode from a potential of the pixel electrode section; a second state of potential where the potential of the metal layer is equal to the potential of the common electrode; and a third state of potential where the potential difference obtained by subtracting the potential of the common electrode from the potential of the metal layer is equal in polarity to the potential dif-

ference obtained by subtracting the potential of the common electrode from the potential of the pixel electrode section and where an absolute value of a difference between the potential of the pixel electrode section and the potential of the common electrode is greater than or equal to an absolute value of a difference between the potential of the metal layer and the potential of the common electrode.

[0076] The foregoing configuration allows the scanning signal line or the auxiliary capacitor line to be covered by the metal layer so that there is no direct overlap between (i) the open region of the alignment control space section, i.e., of a slit or of a space between pixel electrodes and (ii) the scanning signal line or the auxiliary capacitor line.

[0077] Moreover, at the polymer alignment supporting step, i.e., at the PSA step, the potential of the metal layer can be set to form the first state of potential where the potential difference obtained by subtracting the potential of the common electrode from the potential of the metal layer is opposite in polarity to the potential difference obtained by subtracting the potential of the common electrode from the potential of the pixel electrode section, the second state of potential where the potential of the metal layer is equal to the potential of the common electrode, or the third state of potential where the potential difference obtained by subtracting the potential of the common electrode from the potential of the metal layer is equal in polarity to the potential difference obtained by subtracting the potential of the common electrode from the potential of the pixel electrode section and where the absolute value of the difference between the potential of the pixel electrode section and the potential of the common electrode is greater than or equal to the absolute value of the difference between the potential of the metal layer and the potential of the common electrode.

[0078] Thus, in the region of intersection between the alignment control space section and the scanning signal line or the auxiliary capacitor line, the metal layer whose potential has been set to form the first, second, or third state of potential is placed between the layer of the scanning signal line or of the auxiliary capacitor line and the layer of the pixel electrode; therefore, the influence of the potential of the scanning signal line or of the auxiliary capacitor line can be blocked.

[0079] Therefore, the method according to the present invention for manufacturing a liquid crystal display panel makes it possible to keep the alignment of liquid crystal molecules good and align the liquid crystal molecules appropriately, with no influence on the alignment of the liquid crystal molecules by those equipotential surfaces formed in an area of the liquid crystal layer around the alignment control space section intersecting with the scanning signal line or the auxiliary capacitor line, thus bringing about an effect of achieving an improvement in display quality of the liquid crystal display panel.

[0080] A method according to the present invention for driving a liquid crystal display panel is a method for driving such a liquid crystal display panel as described above, the method preferably including applying voltage to the liquid crystal layer in any one of the following states of potential: a first state of potential where a potential difference obtained by subtracting a potential of the common electrode from a potential of the metal layer is opposite in polarity to each other a potential difference obtained by subtracting the potential of the common electrode from a potential of the pixel electrode section; a second state of potential where the potential of the metal layer is equal to the potential of the common electrode; and a third state of potential where the potential difference obtained by subtracting the potential of the common electrode from the potential of the metal layer is equal in polarity to the potential difference obtained by subtracting the potential of the common electrode from the potential of the pixel electrode section and where an absolute value of a difference between the potential of the pixel electrode section and the potential of the common electrode is greater than or equal to an absolute value of a difference between the potential of the metal layer and the potential of the common electrode.

[0081] The foregoing configuration allows the auxiliary capacitor line or the scanning signal line to be covered by the metal layer so that there is no direct overlap between (i) the open region of the alignment control space section, i.e., of a slit or of a space between pixel electrodes and (ii) the auxiliary capacitor line or the scanning signal line.

[0082] Moreover, during actual driving of the liquid crystal display panel, the potential of the metal layer can be set to form the first state of potential where the potential difference obtained by subtracting the potential of the common electrode from the potential of the metal layer is opposite in polarity to the potential difference obtained by subtracting the potential of the common electrode from the potential of the pixel electrode section, the second state of potential where the potential of the metal layer is equal to the potential of the common electrode, or the third state of potential where the potential difference obtained by subtracting the potential of the common electrode from the potential of the metal layer is equal in polarity to the potential difference obtained by subtracting the potential of the common electrode from the potential of the pixel electrode section and where the absolute value of the difference between the potential of the pixel electrode section and the potential of the common electrode is greater than or equal to the absolute value of the difference between the potential of the metal layer and the potential of the common electrode.

[0083] Thus, in the region of intersection between the alignment control space section and the scanning signal line or the auxiliary capacitor line, the metal layer whose potential has been set to form the first, second, or third state of potential is placed between the layer of the scanning signal line or of the auxiliary capacitor line and the layer of the pixel electrode; therefore, the influence of the potential of the scanning signal line or of the auxiliary

capacitor line can be blocked.

[0084] Therefore, the method according to the present invention for driving a liquid crystal display panel makes it possible to keep the alignment of liquid crystal molecules good and align the liquid crystal molecules appropriately, with no influence on the alignment of the liquid crystal molecules by those equipotential surfaces formed in an area of the liquid crystal layer around the alignment control space section intersecting with the scanning signal line or the auxiliary capacitor line, thus bringing about an effect of achieving an improvement in display quality of the liquid crystal display panel.

Advantageous Effects of Invention

[0085] In order to solve the foregoing problems, an active matrix substrate according to the present invention is an active matrix substrate including: a plurality of scanning signal lines; a plurality of signal wires disposed in such a way as to intersect with the scanning signal lines; a pixel section constituted by pixel electrode sections each provided in correspondence with a combination of each of the scanning signal lines and each of the signal wires, the pixel section having an alignment control space section that controls a state of alignment of liquid crystal molecules; a switching element that switches a signal wire as one of the signal wires and a pixel electrode section as one of the pixel electrode sections into a conducting state or a non-conducting state in accordance with a scanning signal supplied from a scanning signal line as one of the scanning signal lines; a metal wire, connected to the switching element, through which when the switching element is in a conducting state, a data signal from the signal wire is supplied to the pixel electrode section; and an auxiliary capacitor line that forms a capacitor with the pixel electrode section, in a region of intersection between the alignment control space section and the auxiliary capacitor line or the scanning signal line, a metal layer being provided between a layer of the pixel section and a layer of the scanning signal line in such a way as to cover at least the auxiliary capacitor line or the scanning signal line.

[0086] In order to solve the foregoing problems, an active matrix substrate according to the present invention is an active matrix substrate including: a plurality of scanning signal lines; a plurality of signal wires disposed in such a way as to intersect with the scanning signal lines; a pixel section constituted by pixel electrode sections each provided in correspondence with a combination of each of the scanning signal lines and each of the signal wires, the pixel section having an alignment control space section that controls a state of alignment of liquid crystal molecules; a switching element that switches a signal wire as one of the signal wires and a pixel electrode section as one of the pixel electrode sections into a conducting state or a non-conducting state in accordance with a scanning signal supplied from a scanning signal line as one of the scanning signal lines; and a metal wire, connected to the switching element, through which when the switching element is in a conducting state, a data signal from the signal wire is supplied to the pixel electrode section, in a region of intersection between the alignment control space section and the scanning signal line, a metal layer being provided between a layer of the pixel section and a layer of the scanning signal line in such a way as to cover at least the scanning signal line.

[0087] Therefore, in the region of intersection between the alignment control space section and the scanning signal line or the auxiliary capacitor line, the metal layer whose potential has been set to form (i) a first state of potential where a potential difference obtained by subtracting the potential of the common electrode from the potential of the metal layer is opposite in polarity to a potential difference obtained by subtracting the potential of the common electrode from the potential of the pixel electrode section, (ii) a second state of potential where the potential of the metal layer is equal to the potential of the common electrode, and (iii) a third state of potential where the potential difference obtained by subtracting the potential of the common electrode from the potential of the metal layer is equal in polarity to the potential difference obtained by subtracting the potential of the common electrode from the potential of the pixel electrode section and where the absolute value of a difference between the potential of the pixel electrode section and the potential of the common electrode is greater than or equal to the absolute value of a difference between the potential of the metal layer and the potential of the common electrode, is placed between the layer of the scanning signal line or of the auxiliary capacitor line and the layer of the pixel electrode; therefore, the influence of the potential of the scanning signal line or of the auxiliary capacitor line during normal driving or at a PSA step in the process of manufacture can be blocked.

[0088] This makes it possible to keep the alignment of liquid crystal molecules good and align the liquid crystal molecules appropriately, with no influence on the alignment of the liquid crystal molecules by those equipotential surfaces formed in an area of the liquid crystal layer around the alignment control space section intersecting with the scanning signal line or the auxiliary capacitor line, thus bringing about an effect of achieving an improvement in display quality of the liquid crystal display panel.

Brief Description of Drawings

[0089]

Fig. 1

Fig. 1 is a cross-sectional view schematically showing the configuration of a main part of a liquid crystal display panel according to the present embodiment.

Fig. 2

Fig. 2 includes block diagrams (a) and (b) each schematically showing the configuration of a liquid crystal

display device according to the present embodiment, (a) showing a liquid crystal display device that is driven by using auxiliary capacitors, (b) showing a liquid crystal display device that is driven without using auxiliary capacitors.

Fig. 3

Fig. 3 includes plan views (a) to (e) schematically showing example configurations of liquid crystal display panels having pixel electrodes provided with ordinary slits according to the present embodiment, respectively.

Fig. 4a

Fig. 4a is a plan view schematically showing the configuration of a liquid crystal display panel provided with an inter-pixel slit according to the present embodiment.

Fig. 4b

Fig. 4b is a cross-sectional view schematically showing the configuration of the liquid crystal display panel shown in Fig. 4a.

Fig. 5

Fig. 5 is a plan view schematically showing the configuration of another liquid crystal display panel provided with an inter-pixel slit according to the present embodiment.

Fig. 6

Fig. 6 is a plan view schematically showing the configuration of a liquid crystal display panel having a pixel electrode provided with fine slits according to the present embodiment.

Fig. 7

Fig. 7 includes (a) a plan view showing the configuration of a liquid crystal display panel having a pixel structure of horizontally long pixel elements according to the present embodiment, with a scanning signal line formed in the center of each pixel electrode, and (b) a plan view showing the configuration of a liquid crystal display panel having a pixel structure of horizontally long pixel elements according to the present embodiment, with each pixel electrode overlapping a scanning signal line in the vicinity of a longer side.

Fig. 8

Fig. 8 shows the configuration of a liquid crystal display panel having a multi-pixel structure according to the present embodiment.

Fig. 9

Fig. 9 shows those lines of electric force and equipotential surfaces in proximity to a slit between a pixel electrode provided with the slit and a counter substrate, (a) showing those lines of electric force and equipotential surfaces in a region where the slit does not intersect with an auxiliary capacitor line, (b) showing those lines of electric force and equipotential surfaces in a region of intersection between the slit and an auxiliary capacitor line, with the auxiliary capacitor line being equal in potential to a COM potential, (c) showing those lines of electric force and equipotential surfaces in the region of intersection between the slit and the auxiliary capacitor line, with the auxiliary capacitor line being higher in potential than the COM potential.

Fig. 10

Fig. 10 shows the appearance of a disturbance in alignment due to a PSA step under a Cs-COM voltage application scheme.

Fig. 11

Fig. 11 shows the appearance of alignment of liquid crystal molecules in a liquid crystal display device including an auxiliary capacitor line, a pixel electrode having a slit, and a common electrode having a projection, (a) showing the appearance of alignment of liquid crystal molecules during normal driving, (b) showing alignment of liquid crystal molecules as formed by the PSA step under the Cs-COM voltage application scheme.

Fig. 12

Fig. 12 is a block diagram schematically showing the configuration of another liquid crystal display device according to the present embodiment.

Description of Embodiments

(Overview of a Liquid Crystal Display Device 1)

[0090] An embodiment of the present invention is described below with reference to Figs. 1 through 8. First, an overview of a liquid crystal display device 1 according to the present embodiment is given. Fig. 1 is a cross-sectional view schematically showing the configuration of a main part of a liquid crystal display panel 2 according to the present embodiment. Fig. 2 includes block diagrams (a) and (b) each schematically showing the configuration of a liquid crystal display device according to the present embodiment, (a) showing a liquid crystal display device 1 that is driven by using auxiliary capacitors, (b) showing a liquid crystal display device 1' that is driven without using auxiliary capacitors.

[0091] As shown in (a) of Fig. 2, the liquid crystal display device 1 according to the present embodiment includes a liquid crystal display panel 2, a driving circuit for driving the liquid crystal display panel 2, a control circuit 3 for controlling driving of the driving circuit, and, as needed, a backlight unit (not illustrated), etc.

[0092] The driving circuit includes a gate driving circuit 4 for driving scanning signal lines (gate bus lines) 21 in the liquid crystal display panel 2, a source driving circuit 5 for driving data signal lines (signal wires, source bus lines) 22 in the liquid crystal display panel 2, and a Cs driving circuit 6 for driving auxiliary capacitor lines (Cs bus lines) 14 in the liquid crystal display panel 2.

[0093] The gate driving circuit 4, the source driving circuit 5, and the Cs driving circuit 6 are electrically connected to the scanning signal lines 21, the data signal lines 22, and the auxiliary capacitor lines 14, respectively, and are designed to give potentials to their respective

bus lines independently of outside. These driving circuits are each electrically connected to the control circuit 3, and are controlled by control signals and video signals supplied from the control circuit 3.

[0094] The scanning signal lines 21 and the data signal lines 22 intersect with each other as shown in (a) of Fig. 2. Each of those regions surrounded by the scanning signal lines 21 and the data signal lines 22 corresponds to a single pixel. The liquid crystal display panel 2 includes an active matrix substrate 10 (thin-film transistor substrate), which will be described later, and a counter substrate 20. The active matrix substrate 10 has a plurality of pixels 7 arrayed in a matrix manner. Further, as will be described in detail later, the pixels 7 are each constituted by a pixel electrode and a switching element. It should be noted that the term "pixel section" in the Claims corresponds to a group of pixels 7 arrayed in a matrix manner and that the term "pixel electrode section" in the Claims corresponds to a pixel electrode constituting each pixel 7.

[0095] The liquid crystal display device 1' shown in (b) of Fig. 2 differs from the liquid crystal display device 1 shown in (a) of Fig. 2 only in the absence of auxiliary capacitor lines (Cs bus lines) 14 and a driving circuit 6 for driving them. The other components of the liquid crystal display device 1' have the same functions as those of the liquid crystal display device 1. Therefore, the liquid crystal display device 1' is not described here.

(Active Matrix Substrate 10)

[0096] A characteristic configuration of the active matrix substrate 10 is described with reference to Fig. 1. As shown in Fig. 1, the active matrix substrate 10 constitutes the liquid crystal display panel 2 in combination with the counter substrate 20 and a liquid crystal layer 30. The active matrix substrate 10 includes a transparent insulating substrate 11, pixel electrodes 12, drain lines (metal wires) 13, and the auxiliary capacitor lines 14. The pixel electrodes 12 are each provided with a slit (alignment control space section) 15. The provision of the slit 15 causes a change in the shape of equipotential surfaces, thereby controlling the orientation of alignment of liquid crystal molecules.

[0097] Moreover, as shown in Fig. 1, the active matrix substrate 10 is **characterized in that** in a region of intersection between a slit 15 in a pixel electrode 12 and a scanning signal line 21 or an auxiliary capacitor line 14, a metal layer constituted by a drain line 13 is provided in such a way as to cover at least the scanning signal line 21 or the auxiliary capacitor line 14.

[0098] Alternatively, the active matrix substrate 10 may also be configured such that in a region of intersection between a slit 15 in a pixel electrode 12 and a scanning signal line 21 or an auxiliary capacitor line 14, a metal layer constituted by a data signal line 22 is provided in such a way as to cover the scanning signal line 21 or the auxiliary capacitor line 14.

[0099] Alternatively, the active matrix substrate 10 may also be configured such that in a region of intersection between a slit 15 in a pixel electrode 12 and a scanning signal line 21 or an auxiliary capacitor line 14, a metal layer constituted by an intermediate electrode or by an independent shield metal is provided in such a way as to cover the scanning signal line 21 or the auxiliary capacitor line 14.

[0100] In the case of formation of the metal layer by an independent shield metal, a shield-metal voltage driving circuit is provided to freely set the potential of the metal layer in the most preferable one of first to third states of potential, which will be described later. Fig. 12 shows a liquid crystal display device 1A obtained by incorporating a shield-metal voltage driving circuit 41 into a liquid crystal display device 1 as shown in (a) of Fig. 2.

[0101] In Fig. 12, the shield-metal voltage driving circuit 41 is disposed opposite the source driving circuit 5 across the liquid crystal display panel 2. This does not imply any limitation, and it is possible to use any circuit layout.

[0102] A process for manufacturing an active matrix substrate includes the step of, in a region of intersection between a slit 15 in a pixel electrode 12 and an auxiliary capacitor line 14 or a scanning signal line 21, forming at least a data signal line 22, a drain line 13, an intermediate electrode, or an independent shield metal between a layer of the pixel electrode 12 and a layer of the auxiliary capacitor line 14 or of the scanning signal line 21 in such a way that at least the auxiliary capacitor line 14 or the scanning signal line 21 is covered.

(PSA Step)

[0103] For an improvement in display performance of a liquid crystal display device, it is necessary, at the stage of manufacturing the liquid crystal display panel, to control a pretilt angle for a satisfactory state of alignment of liquid crystal molecules. An example of a method for controlling a pretilt angle is a PSA (polymer sustained alignment) treatment. The PSA treatment is a process by which the direction in which the liquid crystals lean is memorized by mixing polymerizable monomers into the liquid crystals and polymerizing the monomers with light, heat, or the like in the presence of voltage being applied to the liquid crystals. This makes it possible to achieve a structure that is faster in response speed and unlikely to suffer from a disturbance in liquid crystal alignment, for example, even when pressed with a finger, even if the structure is based on a pixel design that is weak in alignment controllability for the purpose of a larger aperture ratio or the like.

[0104] Further, a liquid crystal display panel of the CS-COM voltage application type, i.e., a type of liquid crystal display panel that is driven by applying voltage to each auxiliary capacitor line (CS) and a common electrode (COM) and thereby applying voltage between each pixel electrode and the common electrode via an auxiliary capacitor, has conventionally been configured as shown in

Fig. 11. In the case of normal driving of a liquid crystal display panel of the CS-COM voltage application type, those liquid crystals aligned near a projection provided on the common electrode and those liquid crystals aligned near a slit provided in the pixel electrode lean in the same direction, as shown in (a) of Fig. 11.

[0105] However, in such a conventional configuration, those liquid crystals aligned near the projection provided on the common electrode and those liquid crystals aligned near the slit provided in the pixel electrode lean in opposite directions, as shown in (b) of Fig. 11, due to voltage that is applied to the common electrode, the pixel electrode, and the auxiliary capacitor line at a PSA step in the process of manufacturing the liquid crystal display panel.

[0106] On the other hand, because of the active matrix substrate 10 configured as described above, the liquid crystal display panel 2 according to the present invention makes it possible to give a desired pretilt angle to liquid crystal molecules at a PSA step in the process of manufacturing the liquid crystal display panel 2. The liquid crystal display panel 2 according to the present invention is described in more detail below.

(Liquid Crystal Display Panel 2)

[0107] The liquid crystal display panel 2 has a pair of substrates disposed to face each other, namely the active matrix substrate 10 and the counter substrate 20, with the liquid crystal layer 30 sandwiched between the active matrix substrate 10 and the counter substrate 20. Wave plates and polarizing plates (not illustrated) may be provided as needed on the outer surfaces of the active matrix substrate 10 and the counter substrate 20 (on those surfaces of the active matrix substrate 10 and the counter substrate 20 which face away from those surfaces of the active matrix substrate 10 and the counter substrate 20 which face each other).

[0108] The counter substrate 20 includes a transparent insulating substrate 16 and a common electrode 17. The common electrode 17 has a rib 18 provided on a surface thereof which faces a pixel electrode 12. The provision of the rib 18 gives a pretilt angle to those liquid crystal molecules located near the rib and, upon application of voltage, allows the other liquid crystal molecules to align themselves along the alignment of those liquid crystal molecules given the pretilt angle. Therefore, the provision of the rib 18 on a surface of the liquid crystal layer makes it possible to more stably control the orientation of alignment of the liquid crystal molecules by applying voltage.

[0109] The common electrode 17, formed substantially all over the transparent insulating substrate 16, is used as an electrode common to all the pixels 7 (i.e., as a common electrode). Moreover, an electric field is applied to the liquid crystal layer 30 by voltage applied to the common electrode 17 and the pixel electrode 12, whereby the liquid crystal layer 30 has its optical transmittance modulated so that an image is formed.

[0110] Although, in the present embodiment, a structure for controlling the alignment of liquid crystal molecules is prepared by providing the common electrode 17 with the rib 18, such a structure may be prepared by providing a slit instead of the rib (alignment control section) 18. Further, in the liquid crystal display panel 2, such a structure needs only be prepared by providing the pixel electrode 12 with a slit, and the common electrode 17 does not necessarily need be provided with such a structure.

[0111] Moreover, as described above, the liquid crystal display panel 2 includes the active matrix substrate 10 wherein in a region of intersection between a slit 15 and an auxiliary capacitor line 14 or a scanning signal line 21, at least a data signal line 22 or a drain line 13 is provided between a layer of a pixel electrode 12 and a layer of the auxiliary capacitor line 14 or of the scanning signal line 21 in such a way as to cover at least the auxiliary capacitor line 14 or the scanning signal line 21.

[0112] This configuration allows at least the auxiliary capacitor line 14 or the scanning signal line 21 to be covered by the metal layer such as the data signal line 22, the drain line 13, the intermediate electrode, or the independent shield metal so that there is no direct overlap between the slit 15 and the auxiliary capacitor line 14 or the scanning signal line 21.

[0113] Moreover, at the PSA step in the process of manufacturing the liquid crystal display panel 2, for example, such voltage may be applied to the auxiliary capacitor line 14 or the scanning signal line 21 that (Potential of Auxiliary Capacitor Line 14 (Scanning Signal Line 21) - Potential of Common Electrode 17) is equal in polarity to (Potential of Pixel Electrode 12 - Potential of Common Electrode 17) and that Potential of Auxiliary Capacitor Line 14 (Scanning Signal Line 21) - Potential of Common Electrode 17| > |Potential of Pixel Electrode 12 - Potential of Common Electrode 17|. . In such a case, the potential of the metal layer is set lower than or equal to that of the pixel electrode. That is, the potential of the metal layer is set to form a first state of potential where a potential difference obtained by subtracting the potential of the common electrode 17 from the potential of the metal layer is opposite in polarity to a potential difference obtained by subtracting the potential of the common electrode 17 from the potential of the pixel electrode 12, a second state of potential where the potential of the metal layer is equal to the potential of the common electrode 17, or a third state of potential where the potential difference obtained by subtracting the potential of the common electrode 17 from the potential of the metal layer is equal in polarity to the potential difference obtained by subtracting the potential of the common electrode 17 from the potential of the pixel electrode 12 and where the absolute value of a difference between the potential of the pixel electrode 12 and the potential of the common electrode 17 is greater than or equal to the absolute value of a difference between the potential of the metal layer and the potential of the common electrode 17. Then, by ap-

plying voltage to the liquid crystal layer 30 to polymerize the monomers mixed in advance into the liquid crystal layer 30, the liquid crystal molecules 101 and 102 of the liquid crystal layer 30 can be given a pretilt angle.

[0114] Further, during normal actual driving of the liquid crystal display panel, such voltage may be applied to the auxiliary capacitor line 14 or the scanning signal line 21 that (Potential of Auxiliary Capacitor Line 14 (Scanning Signal Line 21) - Potential of Common Electrode 17) is equal in polarity to (Potential of Pixel Electrode 12 - Potential of Common Electrode 17) and that Potential of Auxiliary Capacitor Line 14 (Scanning Signal Line 21) - Potential of Common Electrode 17| > |Potential of Pixel Electrode 12 - Potential of Common Electrode 17|. In such a case, the potential of the metal layer is set lower than or equal to that of the pixel electrode. That is, the potential of the metal layer set to form the first state of potential where the potential difference obtained by subtracting the potential of the common electrode 17 from the potential of the metal layer is opposite in polarity to the potential difference obtained by subtracting the potential of the common electrode 17 from the potential of the pixel electrode 12, the second state of potential where the potential of the metal layer is equal to the potential of the common electrode 17, or the third state of potential where the potential difference obtained by subtracting the potential of the common electrode 17 from the potential of the metal layer is equal in polarity to the potential difference obtained by subtracting the potential of the common electrode 17 from the potential of the pixel electrode 12 and the absolute value of the difference between the potential of the pixel electrode 12 and the potential of the common electrode 17 is greater than or equal to the absolute value of the difference between the potential of the metal layer and the potential of the common electrode 17. Then, voltage can be applied to the liquid crystal layer 30.

[0115] That is, the potential V of the metal layer can be set in one of the following states (1) to (3):

(1) V-Vcom is opposite in potential to Vd-Vcom;
(2) V=Vcom; and
(3) V-Vcom is equal in potential to Vd-Vcom, and |Vd-Vcom| ≥ |V-Vcom|,

where V is the potential of the metal layer, Vcom is the potential of the common electrode, and Vd is the potential of the pixel electrode.

It should be noted here that the first to third states of potential correspond to the states (1) to (3), respectively.

[0116] Thus, in the region of intersection between the slit 15 and the auxiliary capacitor line 14 or the scanning signal line 21, the metal layer whose potential has been set to form the first, second, or third state of potential is placed between the layer of the scanning signal line 21 or of the auxiliary capacitor line 14 and the layer of the pixel electrode 12; therefore, the influence of the potential of the scanning signal line 21 or of the auxiliary capacitor line 14 can be blocked.

[0117] This makes it possible to prevent a defect in alignment that has conventionally been caused when such voltage is applied to the auxiliary capacitor line 14 or the scanning signal line 21 during the PSA step or during normal driving that (Potential of Auxiliary Capacitor Line 14 (Scanning Signal Line 21) - Potential of Common Electrode 17) is equal in polarity to (Potential of Pixel Electrode 12 - Potential of Common Electrode 17) and that |Potential of Auxiliary Capacitor Line 14 (Scanning Signal Line 21) - Potential of Common Electrode 17| > |Potential of Pixel Electrode 12 - Potential of Common Electrode 17|.

[0118] This makes it possible, during actual driving or manufacture of the liquid crystal display panel 2, to keep the alignment of the liquid crystal molecules 101 good and align the liquid crystal molecules appropriately, with no influence on the alignment of the liquid crystal molecules 101 by those equipotential surfaces formed in an area of the liquid crystal layer 30 around the slit 15 intersecting with the scanning signal line 21 or the auxiliary capacitor line 14, thus bringing about an improvement in display quality of the liquid crystal display panel 2.

[0119] It should be noted that in which one of the first to third states of potential the potential V of the metal layer can be set during actual driving of the liquid crystal display panel 2 depends on what is used as the metal. This point is discussed more specifically.

[0120] First, when the metal layer is constituted by an independent shield metal, the shield-metal voltage driving circuit 41 makes it possible to freely set the potential V of the shield metal; therefore, it is possible to freely choose any one of the states of potential (1) to (3) as the potential V.

[0121] Next, when the metal layer is constituted by a drain line 13 or an intermediate electrode, the drain line 13 or the intermediate electrode is always equal in potential to the pixel electrode 12; therefore, the potential V is set as V-Vcom=Vd-Vcom included in the state of potential (3).

[0122] Furthermore, when the metal layer is constituted by a data signal line 22, the potential V of the data signal line 22 swings between positive and negative polarities with the potential Vcom of the common electrode as the center and therefore is equal to the potential Vcom on an average. Therefore, the potential V is set in the state of potential (2) (V=Vcom).

[0123] It should be noted that the active matrix substrate 10 may be configured to have such a structure that a metal wiring layer including scanning signal lines 21 and auxiliary capacitor lines 14, a gate insulating layer, a metal wiring layer including data signal lines 22 and drain lines (metal wires) 13, an insulating layer, a resin layer, and pixel electrodes 12 have been formed in this order on a transparent insulating substrate made of glass or the like.

[0124] Further, the counter substrate 20 may be a CF substrate obtained, for example, by stacking a color filter

layer, a black matrix, and a common electrode in this order on that surface of a transparent insulating layer which faces the active matrix substrate 10. Further, the counter substrate 20 may be provided, as needed, with functional layers (not illustrated) such as an undercoat layer (foundation layer) and an overcoat layer (planarizing layer).

[0125] Further, the common electrode 17 and the pixel electrodes 12 may each be a transparent electrode formed by a transparent conductive film made of ITO (indium tin oxide) or the like.

[0126] Meanwhile, examples of a slit 15 in a pixel electrode include: an ordinary slit, which is a long narrow hole provided partially in the pixel electrode; a fine slit, which is a long narrow space provided, for example, by making a combtooth cut in the pixel electrode; a slit that is a space between adjacent pixel electrodes (such a slit being hereinafter referred to as "inter-pixel slit"); and the like. Accordingly, the following describes specific example configurations according to categories of slits in pixel electrodes.

(Slit 15a)

[0127] Fig. 3 includes plan views schematically showing example configurations of liquid crystal display panels 2a having pixel electrodes provided with ordinary slits according to the present embodiment, respectively. As shown in (a) to (e) of Fig. 3, provided at each of the intersections between the scanning signal lines 21 and the data signal lines 22 are a pixel electrode 12a serving as a pixel electrode section and a TFT (thin-film transistor) 25 serving as a switching element. Further, the TFT 25 is provided in a corner (corner portion) of or in the vicinity of a side of (in a side edge portion of) the pixel electrode 12a. The pixel electrode 12a and the TFT 25 constitute a pixel 7 of Fig. 1 in combination with a common electrode 17 (not illustrated).

[0128] Further, as shown in (a) to (e) of Fig. 3, the pixel electrode 12a is provided with long narrow holes serving as slits 15a, and the common electrode 17 (not illustrated) is provided with ribs 18. In the configurations shown in (a) to (e) of Fig. 3, the slits 15a and the ribs 18 extend substantially in parallel with each other. Further, with the relationship of disposition between the slits 15a and the ribs 18 viewed two-dimensionally, the slits 15a and the ribs 18 appear to be alternately disposed. Moreover, if, in the configurations shown in (a) to (e) of Fig. 3, each pixel were divided into two regions by drawing a boundary parallel to the scanning signal line 21 so that the boundary passes transversely across the center of the pixel electrode 12a, those slits 15a and ribs 18 disposed in one of the regions and those slits 15a and ribs 18 disposed in the other region would be disposed in such a way as to be close to each other at a sharp angle at the boundary, respectively, and to be symmetrical with each other.

[0129] Thus, at the site where the plurality of slits 15a and ribs 18 are close to each other at a sharp angle, respectively, the alignment of liquid crystal molecules is different from that which is originally intended to be obtained, so that there appear dark lines. Therefore, such a site constitutes a non-display region and, as shown (a) to (c) of Fig. 3, serves as a convenient site for an auxiliary capacitor line 14 to pass through. The same applies to those configurations shown in Figs. 6 to 8, which will be described later.

[0130] It should be noted that there may be a configuration having a scanning signal line 21 passing through the site where the plurality of slits 15a and ribs 18 are close to each other at a sharp angle, respectively, as shown in (d) of Fig. 3. Furthermore, there may be a configuration having no auxiliary capacitor line 14 passing through the site, as shown in (e) of Fig. 3. The present invention is not limited to any one of these configurations.

[0131] As shown in (a) to (e) of Fig. 3, the TFT 25 includes a gate electrode, a gate insulating film, a semiconductor layer, a source electrode 26, and a drain electrode 27. Electrically connected to the gate electrode of the TFT 25 is a scanning signal line 21, part of which functions as the gate electrode. Further electrically connected to the source electrode 26 is a data signal line 22.

[0132] The TFT 25 carries out a switching operation in accordance with a scanning signal supplied from the scanning signal line 21 to switch the pixel electrode 12a and the data signal line 22 between a conducting state and a non-conducting state. Moreover, in the conducting state, a voltage corresponding to a data signal representing an image supplied from the data signal line 22 is supplied to the pixel electrode 12a through a drain line 13.

[0133] Further, the auxiliary capacitor line 14 is provided in the same layer as the scanning signal line 21. Furthermore, each of the pixel electrodes 12a has a drain line 13, provided in a layer above the auxiliary capacitor line 14 with a gate insulating film (not illustrated) sandwiched therebetween, which extends from the drain electrode 27 to a position directly above the auxiliary capacitor line 14 or the scanning signal line 21. Moreover, the drain line 13, disposed directly above the auxiliary capacitor line 14 or the scanning signal line 21, has an auxiliary capacitor electrode section 130 (see (a) of Fig. 3), provided in an overlap section with the auxiliary capacitor line 14, which serves to enlarge the area of overlap between the auxiliary capacitor line 14 and the drain line 13. Furthermore, the drain line 13 is electrically connected to the pixel electrode 12a through a contact hole 24 provided in the auxiliary capacitor electrode section 130. Thus, in a configuration having an auxiliary capacitor line 14, the auxiliary capacitor line 14 forms an auxiliary capacitor with a pixel electrode 12a in each pixel. This makes it possible to stabilize the potential of each pixel.

[0134] In an example configuration of a liquid crystal display panel 2a as shown in (a) of Fig. 3, the scanning signal lines 21 extend along upper and lower edges of the pixel electrode 12a, respectively, and the auxiliary capacitor line 14 extends in such a way as to pass transversely across the center of the pixel electrode 12a sub-

stantially in parallel with the scanning signal lines 21. Moreover, in each region of intersection (surrounded by a dotted line) between the open region of a slit 15a provided in the pixel electrode 12a and the auxiliary capacitor line 14 passing transversely across the center of the pixel electrode 12a, a covering metal section 19 (metal layer) composed of the drain line 13 in such a way as to cover at least the auxiliary capacitor line 14 is provided as part of the auxiliary capacitor electrode section 130 between the layer of the pixel electrode 12a and the layer of the auxiliary capacitor line 14.

[0135] In an example configuration of a liquid crystal display panel 2a as shown in (b) of Fig. 3, the scanning signal lines 21 extend along upper and lower edges of the pixel electrode 12a, respectively, and the auxiliary capacitor line 14 extends in such a way as to pass transversely across the center of the pixel electrode 12a substantially in parallel with the scanning signal lines 21. Moreover, in each region of intersection (surrounded by a dotted line) between the open region of a slit 15a provided in the pixel electrode 12a and the scanning signal line 21 passing transversely along the upper or lower edge of the pixel electrode 12a, a covering metal section 19 (metal layer) composed of the drain line 13 in such a way as to cover at least the scanning signal line 21 is provided between the layer of the pixel electrode 12a and the layer of the scanning signal line 21.

[0136] In an example configuration of a liquid crystal display panel 2a as shown in (c) of Fig. 3, the scanning signal lines 21 extend along upper and lower edges of the pixel electrode 12a, respectively, and the auxiliary capacitor line 14 extends in such a way as to pass transversely across the center of the pixel electrode 12a substantially in parallel with the scanning signal lines 21. Moreover, in each region of intersection (surrounded by a dotted line) between the open region of a slit 15a provided in the pixel electrode 12a and the auxiliary capacitor line 14 passing transversely across the center of the pixel electrode 12a, a covering metal section 19 (metal layer) composed of the drain line 13 in such a way as to cover at least the auxiliary capacitor line 14 is provided as part of the auxiliary capacitor electrode section 130 between the layer of the pixel electrode 12a and the layer of the auxiliary capacitor line 14. Furthermore, in each region of intersection (surrounded by a dotted line) between the open region of a slit 15a provided in the pixel electrode 12a and the scanning signal line 21 passing transversely along the upper or lower edge of the pixel electrode 12a, a covering metal section 19 (metal layer) composed of the drain line 13 in such a way as to cover at least the scanning signal line 21 is provided between the layer of the pixel electrode 12a and the layer of the scanning signal line 21.

[0137] In an example configuration of a liquid crystal display panel 2a as shown in (d) of Fig. 3, the scanning signal line 21 extends in such a way as to pass transversely across the center of the pixel electrode 12a, and the auxiliary capacitor lines 14 extend along upper and lower edges of the pixel electrode 12a, respectively. Moreover, in each region of intersection (surrounded by a dotted line) between the open region of a slit 15a provided in the pixel electrode 12a and the auxiliary capacitor line 14 passing transversely along the upper or lower edge of the pixel electrode 12a, a covering metal section 19 (metal layer) composed of the drain line 13 in such a way as to cover at least the auxiliary capacitor line 14 is provided between the layer of the pixel electrode 12a and the layer of the auxiliary capacitor line 14.

[0138] Alternatively, the example configuration of the liquid crystal display panel 2a as shown in (d) of Fig. 3 may also be configured such that in each region of intersection between the open region of a slit 15a provided in the pixel electrode 12a and the scanning signal line 21 passing transversely across the center of the pixel electrode 12a, a covering metal section 19 (metal layer) composed of the drain line 13 in such a way as to cover at least the scanning signal line 21 is provided between the layer of the pixel electrode 12a and the layer of the scanning signal line 21.

[0139] In an example configuration of a liquid crystal display panel 2a as shown in (e) of Fig. 3, no auxiliary capacitor line 14 is provided, and the scanning signal lines 21 extend along upper and lower edges of the pixel electrode 12a, respectively. That is, the liquid crystal display panel 2a shown in (e) of Fig. 3 is a liquid crystal display panel that constitutes a liquid crystal display device 1 as shown in (b) of Fig. 2. Moreover, in each region of intersection (surrounded by a dotted line) between the open region of a slit 15a provided in the pixel electrode 12a and the scanning signal line 21 passing transversely along the upper or lower edge of the pixel electrode 12a, a covering metal section 19 (metal layer) composed of the drain line 13 in such a way as to cover at least the scanning signal line 21 is provided between the layer of the pixel electrode 12a and the layer of the scanning signal line 21.

[0140] Further, although, in each of the examples shown in (a) through (e) of Fig. 3, the covering metal section 19 is constituted by the drain line 13, the covering metal section 19 may be constituted by a data signal line 22, an intermediate electrode (not illustrated), or an independent shield metal (not illustrated).

[0141] It should be noted that each of the examples shown in Fig. 3 shows a configuration in which the covering metal section 19 stretches into a region where there is no intersection between the open region of the slit 15 and the scanning signal line 21 or the auxiliary capacitor line 14. The greater the extent to which the covering metal section 19 stretches into the region is, the more profound the effect of suppressing a disturbance in alignment becomes. However, this adversely results in a disadvantageous aperture ratio. Therefore, the extent to which the covering metal section 19 stretches into the region is determined by a balance between disturbance in alignment and aperture ratio according to the required specifications.

(Slit 15b)

[0142] Figs. 4a and 4b show the configuration of a liquid crystal display panel 2b provided with an inter-pixel slit according to the present embodiment. Fig. 4a is a plan view schematically showing the configuration of the liquid crystal display panel, and Fig. 4b is a cross-sectional view of a region taken along line A-B in Fig. 4a.

[0143] As shown in Fig. 4a, provided at each of the intersections between the scanning signal lines 21 and the data signal lines 22 are a pixel electrode 12b serving as a pixel electrode section and a TFT (thin-film transistor) 25 serving as a switching element. The configuration shown in Fig. 4a is the same as those shown in Fig. 3 in that the pixel electrode 12b and the TFT 25 constitute a pixel 7 of Fig. 1 in combination with a common electrode 17 (not illustrated). Further, the structure and operation of the TFT 25 are the same as those shown in Fig. 3 and, as such, are not described here. However, the configuration shown in Fig. 4a is different from those shown in Fig. 3 in that the space between the pixel electrode 12b and a pixel electrode 12b' adjacent thereto functions as a slit 15b. Further, the common electrode 17 (not illustrated) is provided with a rib 18, and the rib 18 extends substantially in parallel with the inter-pixel slit 15b.

[0144] Further, as shown in Fig. 4a, the auxiliary capacitor line 14 extends substantially in parallel with the scanning signal lines 21, passing transversely across the pixel electrode 12b. It should be noted that the scanning signal lines 21 are provided in the same layer in which the auxiliary capacitor line 14 shown in Fig. 4b is provided. Furthermore, the auxiliary capacitor line 14 also extends along longer sides of the pixel electrode 12b (the longer sides being substantially perpendicular to the scanning signal lines 21) in a position directly below the pixel electrode 12b. It should be noted that the common electrode 17 is provided with the rib 18, which extends in parallel with that part of the auxiliary capacitor line 14 which extends along the longer sides of the pixel electrode 12b.

[0145] Furthermore, as shown in Figs. 4a and 4b, each of the pixel electrodes 12 has a drain line 13 provided in a layer above the auxiliary capacitor line 14 formed on a glass substrate 33, with a gate insulating film 32 sandwiched between the drain line 13 and the auxiliary capacitor line 14, and the drain line 13 extends from the drain electrode 27 along that part of the auxiliary capacitor line 14 which extends along the longer sides of the pixel electrode 12b.

[0146] Moreover, the drain line 13, extending along the longer sides of the pixel electrode 12b, has an auxiliary capacitor electrode section 131 provided in a position of intersection between the drain line 13 and that part of the auxiliary capacitor line 14 which extends in parallel with the scanning signal lines 21, and the auxiliary capacitor electrode section 131 serves to enlarge the area of overlap between the auxiliary capacitor line 14 and the drain line 13. Furthermore, the drain line 13 is electrically connected to the pixel electrode 12b through a contact hole 24 provided in an interlayer insulating film 31. Thus, the auxiliary capacitor line 14 and the pixel electrode 12b form an auxiliary capacitor in each pixel. This makes it possible to stabilize the potential of each pixel.

[0147] In the configuration shown in Figs. 4a and 4b, the region in the common electrode 17 (not illustrated) where the rib 18 is provided is low in efficiency of transmission. This low-transmittance region is utilized for a greater auxiliary capacitance by providing the auxiliary capacitor line 14 so that it not only extends in parallel with the scanning signal lines 21 but also extends along the longer sides of the pixel electrode 12b.

[0148] Moreover, in the liquid crystal panel 2b, as shown in Fig. 4a, in a region of intersection (surrounded by a dotted line) between the open region of the slit 15b (i.e., the space between the pixel electrodes 12b and 12b') and the auxiliary capacitor line 14, a covering metal section 19 composed of the drain line 13 in such a way as to cover at least the auxiliary capacitor line 14 is provided as part of the auxiliary capacitor electrode section 131 between the layer of the pixel electrode 12b and the layer of the auxiliary capacitor line 14.

[0149] It should be noted that as with the examples shown in Fig. 3, the example shown in Figs. 4a and 4b shows a configuration in which the covering metal section 19 stretches into a region where there is no intersection between the open region of the slit 15b and the auxiliary capacitor line 14. The extent to which the covering metal section 19 stretches into the region is determined by a balance between disturbance in alignment and aperture ratio according to the required specifications.

[0150] Fig. 5 is a plan view schematically showing the configuration of another liquid crystal display panel 2b' provided with an inter-pixel slit according to the present embodiment. In the liquid crystal panel 2b', as shown in Fig. 5, in a region of intersection (surrounded by a dotted line) between the open region of a slit 15b (i.e., a space between pixel electrodes 12b and 12b') and an auxiliary capacitor line 14, a covering metal section 19 composed of a data signal line 22 in such a way as to cover at least the auxiliary capacitor line 14 is provided between the layer of the pixel electrode 12b and the layer of the auxiliary capacitor line 14. It should be noted that the covering metal section 19 is formed by locally expanding the width of the data signal line 22.

[0151] That is, although the configuration shown in Figs. 4a and 4b is a configuration having a drain line 13 formed in such a way as to cover that region of an auxiliary capacitor line 14 which intersect with the open region of a slit 15b, there may be a configuration having a data signal line 22 formed in such a way as to cover that region of an auxiliary capacitor line 14 which intersects with the open region of a slit 15b, as shown in Fig. 5. It should be noted that the configuration shown in Fig. 5 is the same as those shown in Fig. 3, except for the data signal line 22 is provided in such a way as to cover that region of the auxiliary capacitor line 14 which intersects with the

open region of the slit 15b, and, as such, is not described here.

(Slit 15c)

[0152] Fig. 6 is a plan view schematically showing the configuration of a liquid crystal display panel 2c having a pixel electrode provided with fine such fine slits as mentioned above according to the present embodiment. As shown in Fig. 6, provided at each of the intersections between the scanning signal lines 21 and the data signal lines 22 are a pixel electrode 12c serving as a pixel electrode section and a TFT 25 serving as a switching element. It should be noted that in Fig. 6, those black lines in the pixel electrode 12c represent fine slits 15c; that is, those areas excluding the black lines represent the pixel electrode 12c.

[0153] Further, the configuration shown in Fig. 6 is the same as those shown in Fig. 3 in that the pixel electrode 12c and the TFT 25 constitute a pixel 7 of Fig. 1 in combination with a common electrode 17 (not illustrated). Further, the structure and operation of the TFT 25 are the same as those shown in Fig. 3 and, as such, are not described here. However, The configuration shown in Fig. 6 is different from those shown in Fig. 3 in that the pixel electrode is a combtooth electrode and those slits provided in the pixel electrodes are fine slits 15c.

[0154] In the configuration shown in Fig. 6, the common electrode 17 (not illustrated) is not provided with a rib 18, but may be provided with a rib 18 for better alignment controllability, without implying any particular limitation on the presence or absence of a rib 18.

[0155] Further, each of the fine slits 15c has its longer sides inclined at approximately 45 degrees to the drain line 13, and the fine slits 15c are divided into four groups of fine slits extending along four directions that differ by approximately 90 degrees one after the other, respectively. In such a configuration, when voltage is applied to the pixel electrode 12c, the liquid crystal molecules lean along the longer sides of each of the fine slits 15c, so that four domains different in orientation of alignment can be formed in each pixel. It should be noted that two domains may be formed by forming two groups of fine slits extending longitudinally and transversely, respectively.

[0156] Further provided in the same layer as the scanning signal lines 21 is an auxiliary capacitor line 14 extending substantially in parallel with the scanning signal lines 21 and passing transversely across the center of each of the corresponding pixel electrodes 12c. Furthermore, each of the pixel electrodes 12c has a drain line 13, provided in a layer above the auxiliary capacitor line 14 with a gate insulating film (not illustrated) sandwiched therebetween, which extends from the drain electrode 27 along longer sides of the pixel electrode 12c. Moreover, the drain line 13 has an auxiliary capacitor electrode section 132, provided in a position of intersection between the drain line 13 and the auxiliary capacitor line 14, which serves to enlarge the area of overlap between the auxiliary capacitor line 14 and the drain line 13. The drain line 13 is electrically connected to the pixel electrode 12c through a contact hole 24 provided in the auxiliary capacitor electrode section 132. Thus, the auxiliary capacitor line 14 and the pixel electrode 12c form an auxiliary capacitor in each pixel. This makes it possible to stabilize the potential of each pixel.

[0157] Moreover, in the liquid crystal display panel 2c, as shown in Fig. 6, in a region of intersection (surrounded by a dotted line) between the open region of a slit 15c provided in the pixel electrode 12c and the auxiliary capacitor line 14, a covering metal section 19 is provided as part of the auxiliary capacitor line 132 between the layer of the pixel electrode 12c and the layer of the auxiliary capacitor line 14 in such a way as to cover the auxiliary capacitor line 14.

[0158] It should be noted that as with the examples shown in Fig. 3, the example shown in Fig. 6 shows a configuration in which the covering metal section 19 stretches into a region where there is no intersection between the open region of the slit 15c and the auxiliary capacitor line 14. The extent to which the covering metal section 19 stretches into the region is determined by a balance between disturbance in alignment and aperture ratio according to the required specifications.

(Horizontally Long Picture Element)

[0159] Figs. 3 through 5 show the configurations of vertically long picture elements. However, depending on the design of a liquid crystal display panel, there may be a case where each pixel is structured to have a vertical arrangement of horizontally long RGB picture elements. Fig. 7 shows the configuration of a liquid crystal display panel having a pixel structure of horizontally long picture elements, (a) showing a configuration having a scanning signal line 21 formed in such a way as to pass transversely through the region of a pixel electrode 12 along longer sides of the pixel electrode 12, (b) showing a configuration having an auxiliary capacitor line 14 formed in such a way as to pass transversely through the region of a pixel electrode 12 along longer sides of the pixel electrode 12, with the pixel electrode 12 overlapping a scanning signal line 21 in the vicinity of one of the two longer sides.

[0160] In Fig. 7, those members which have the same functions as those shown in Figs. 3 through 5 are given the same reference numerals. Such members are therefore not described here. In the liquid crystal display panel shown in Fig. 7, the pixel electrode overlaps not only an auxiliary capacitor line but also a scanning signal line.

[0161] As shown in (a) of Fig. 7, there is a scanning signal line 21 formed toward the center of a pixel electrode 12 having its longer sides extending in parallel with the scanning signal line 21, and there is provided auxiliary capacitor lines 14 extending in parallel with the scanning signal line 21 in such a way as to have overlaps near the longer sides of the pixel electrode 12, respectively. Fur-

thermore, one of the two auxiliary capacitor lines 14 overlapping the pixel electrode 12 has an extended section 141 extending from an area near the center of the longer side of the pixel electrode 12 to the scanning signal line 21 in parallel with the shorter sides of the pixel electrode 12. There are also a plurality of slits 15 formed symmetrically with each other about a center line that divides each of the longer sides of the pixel electrode 12 into two and at sharp angles to the center line.

[0162] In such a configuration, there exist a plurality of regions of intersection between the scanning signal line 21 and slits 15 provided in the pixel electrode 12, and there exist a plurality of regions of intersection between the auxiliary capacitor line 14 and slits 15.

[0163] Moreover, in the liquid crystal display panel 2', as shown in (a) of Fig. 7, in each of the plurality of regions of intersection (each surrounded by a dotted line) between the open regions of the slits 15 provided in the pixel electrode 12 and the scanning signal line 21, a covering metal section 19 stretching from part of the drain line 13 along the shorter sides of the pixel electrode 12 is provided between the layer of the pixel electrode 12 and the layer of the scanning signal line 21 in such a way as to cover the scanning signal line 21.

[0164] Furthermore, the drain line 13 extends up to the auxiliary capacitor line 14 while overlapping the extended section 141 of the auxiliary capacitor line 14 and, further, extends along the longer side of the pixel electrode 12 into the plurality of regions of intersection between the auxiliary capacitor line 14 and the slits 15. In the plurality of regions of intersection between the auxiliary capacitor line 14 and the slits 15, there are provided a plurality of covering metal sections 19 stretching from the drain line 13 in such a way as to cover the respective regions.

[0165] Further, even in a case where, as shown in (b) of Fig. 7, the pixel electrode 12 overlaps one of the two scanning signal lines 21 near a longer side of the pixel electrode 12 and there is an auxiliary capacitor line 14 formed toward the center of the pixel electrode 12, there exit a plurality of regions of intersection between the scanning signal line 21 and slits 15 provided in the pixel electrode 12 in the same manner as described above, and there exit a plurality of regions of intersection between the auxiliary capacitor line 14 and slits 15.

[0166] Moreover, in the liquid crystal display panel 2', as shown in (b) of Fig. 7, in each of the plurality of regions of intersection (each surrounded by a dotted line) between the open regions of the slits 15 provided in the pixel electrode 12 and the scanning signal line 21, a covering metal section 19 stretching from part of the drain line 13 along the shorter sides of the pixel electrode 12 is provided between the layer of the pixel electrode 12 and the layer of the scanning signal line 21 in such a way as to cover the scanning signal line 21.

[0167] Furthermore, in each of the plurality of regions of intersection between the open regions of the slits 15 and the auxiliary capacitor line 14, a covering metal section 19 obtained by widening part of the drain line 13 is provided between the layer of the pixel electrode 12 and the layer of the auxiliary capacitor line 14 in such a way as to cover the auxiliary capacitor line 14. Although, in Fig. 7, the covering metal section 19 is constituted by the drain line 13, the covering metal section 19 may be constituted by a data signal line 22, an intermediate electrode (not illustrated), or an independent shield metal (not illustrated).

[0168] Although, in the example shown in Fig. 7, the pixel electrode 12 is horizontally long; that is, the pixel electrode has its longer sides extending in parallel with the scanning signal lines 21, the pixel electrode may be vertically long; that is, the pixel electrode 12 may have its longer sides extending perpendicularly to the scanning signal lines 21.

(Multi-pixel Structure)

[0169] As a technique for improving the dependence of the gamma characteristics of a liquid crystal display panel on viewing angles (difference between the gamma characteristics of a liquid crystal display device as viewed squarely and the gamma characteristics of the device as viewed obliquely), there is a pixel division method (so-called multi-pixel technology). A liquid crystal display panel of the pixel division type has a multi-pixel structure in which each pixel is constituted by a plurality of subpixels. Moreover, the present invention can also be applied to a liquid crystal display panel having a multi-pixel structure.

[0170] First, the pixel division method is described. Fig. 8 shows the configuration of a liquid crystal display panel 200 having a multi-pixel structure. As shown in Fig. 8, the liquid crystal display panel 200 includes: data signal lines 220 and scanning signal lines 220, which are orthogonal to each other; auxiliary capacitor lines 140a and 140b; and pixels disposed in a matrix manner.

[0171] Each of the pixels is provided at an intersection between its corresponding one of the data signal lines 220 and its corresponding one of the scanning signal line 210, and includes subpixel electrodes (pixel electrode sections) 120a and 120b and TFTs 250a and 250b. The auxiliary capacitor lines 140a and 140b are disposed in such a way as to pass transversely along the upper edge of the subpixel electrode 120a and the lower edge of the subpixel electrode 120b, respectively. Moreover, the scanning signal line 210 extends in parallel with the auxiliary capacitor lines 140a and 140b in such a way as to overlap the space between the subpixel electrodes 120a and 120b disposed one above the other.

[0172] The TFT 250a is provided in a corner portion of the subpixel electrode 120a proximate to the point of intersection between the data signal line 220 and the scanning signal line 210. A drain line 130a extends along the data signal line 220 up to the auxiliary capacitor line 140a, and further includes an auxiliary capacitor electrode section 330a that overlaps the auxiliary capacitor line 140a.

[0173] Further, in the auxiliary capacitor electrode sec-

tion 330a, the drain line 130a is electrically connected to the subpixel electrode 120a through a contact hole 240a.

[0174] Similarly, the TFT 250b is provided in a corner portion of the subpixel electrode 120b proximate to the point of intersection between the data signal line 220 and the scanning signal line 210. A drain line 130b extends along the data signal line 220 up to the auxiliary capacitor line 140b, and further includes an auxiliary capacitor electrode section 330b that overlaps the auxiliary capacitor line 140b.

[0175] Further, in the auxiliary capacitor electrode section 330b, the drain line 130b is electrically connected to the subpixel electrode 120b through a contact hole 240b.

[0176] Thus, the subpixel electrodes 120a and 120b form capacitors with the auxiliary capacitor lines 140a and 140b, respectively, and also form capacitors with the common electrode. Further, the TFTs 250a and 250b have their gate electrodes electrically connected to the scanning signal line 210, and their source electrodes 260a and 260b to the data signal lines 220.

[0177] The TFTs 250a and 250b carry out a switching operation in accordance with a scanning signal supplied from the scanning signal line 210 to switch the pixel electrodes 120a and 120b and the data signal line 220 between a conducting state and a non-conducting state. Moreover, in the conducting state, voltages corresponding to a data signal representing an image supplied from the data signal line 220 are supplied to the pixel electrode 120a and 120b through the drain lines 130a and 130b, respectively.

[0178] In the liquid crystal display panel 200, the subpixel electrodes 120a and 120b are supplied with voltages corresponding to the same data signal from the data signal line 220. However, by controlling the voltages of the auxiliary capacitor lines 140a and 140b individually, the subpixel electrodes 120a and 120b can be made different in effective voltage through the auxiliary capacitors between the subpixel electrodes and the auxiliary capacitor lines.

[0179] For example, the voltages of the auxiliary capacitor lines 140a and 140b are individually controlled by voltage-reversing the auxiliary capacitor lines 140a and 140b every horizontal scanning period such that when the auxiliary capacitor line 140a level-shifts in voltage in a plus direction, the auxiliary capacitor line 140b level-shifts in voltage in a minus direction, and that when, after one horizontal scanning period, the auxiliary capacitor line 140a level-shifts in voltage in a minus direction, the auxiliary capacitor line 140b level-shifts in voltage in a plus direction. That is, by supplying the auxiliary capacitor lines 140a and 140b with rectangular waves that are out of phase by 180 degrees, the subpixel electrodes 120a and 120b are made different in potential due to the capacitor formed by the subpixel electrode 120a and the auxiliary capacitor line 140a and the capacitor formed by the subpixel electrode 120b and the auxiliary capacitor line 140b.

[0180] Thus, in a liquid crystal display panel of the multi-pixel structure, a halftone can be expressed by composing each pixel of a high-luminance subpixel (bright subpixel) and a low-luminance subpixel (dark subpixel), whereby the dependence of gamma characteristics on viewing angles (e.g., excess brightness) is improved.

[0181] However, in a liquid crystal display panel of the multi-pixel structure having its subpixel electrodes provided with slits, such equipotential lines as those shown in (c) of Fig. 9 appear due to the relationship among the common electrode, the subpixel electrodes, and the auxiliary capacitor lines not only at the PSA step in the process of manufacturing the liquid crystal display panel but also during actual driving according to the pixel division method. Therefore, even during actual driving, there may occur a defect in alignment of liquid crystal molecules, and such a defect in alignment ends up causing deterioration in display quality.

[0182] Accordingly, in the liquid crystal display panel 200 having a multi-pixel structure, as shown in Fig. 8, in a region of intersection (surrounded by a dotted line) between the open region of a slit 150a provided in the subpixel electrode 120a and the auxiliary capacitor line 140, the drain line 130a has a covering section 190a, provided between the layer of the pixel electrode 120a and the layer of the auxiliary capacitor line 140a, which covers the auxiliary capacitor line 140a. In other words, the drain line 130a has a covering section 190 stretching from the auxiliary capacitor electrode section 330a in such a way as to cover the region of intersection between the open region of the slit 150a and the auxiliary capacitor line 140a.

[0183] Similarly, in a region of intersection (surrounded by a dotted line) between the open region of a slit 150b provided in the subpixel electrode 120b and the auxiliary capacitor line 140b, the drain line 130b has a covering section 190b, provided between the layer of the pixel electrode 120b and the layer of the auxiliary capacitor line 140b, which covers the auxiliary capacitor line 140b.

[0184] The present invention is not limited to the description of the embodiments above, but may be altered by a skilled person within the scope of the claims. An embodiment based on a proper combination of technical means disclosed in different embodiments is encompassed in the technical scope of the present invention.

Industrial Applicability

[0185] The present invention can be applied to a liquid crystal display panel including a substrate structured such that a slit in a pixel electrode intersects with a scanning signal line or an auxiliary capacitor line and, in particular, is suitable to a liquid crystal display device in which a pretilt angle of liquid crystal molecules are formed through a PSA step under a Cs-COM voltage application scheme.

Reference Signs List

[0186]

1	Liquid crystal display device
2	Liquid crystal display panel
3	Control circuit
4	Gate driving circuit
5	Source driving circuit
6	CS driving circuit
7	Pixel
10	Active matrix substrate
11	Transparent insulating substrate
12	Pixel electrode (pixel electrode section)
13	Drain line (metal wire)
14	Auxiliary capacitor wire
15	Slit (alignment control space section)
16	Transparent insulating substrate
17	Common electrode
18	Rib (alignment control section)
19	Covering metal section (metal layer, covering section)
20	Counter substrate
21	Scanning signal line
22	Data signal line (signal wire)
24	Contact hole
25	TFT (switching element)
26	Source electrode
27	Drain electrode
30	Liquid crystal layer
31	Interlayer insulating film
32	Gate insulating film
33	Glass substrate

Claims

1. An active matrix substrate (10) comprising:

a plurality of scanning signal lines (21);
a plurality of signal wires (22) disposed in such a way as to intersect with the scanning signal lines (21);
a pixel section constituted by pixel electrode sections (12) each provided in correspondence with a combination of each of the scanning signal lines (21) and each of the signal wires (22), the pixel section having an alignment control space section (15) that controls a state of alignment of liquid crystal molecules;
a switching element (25) that switches a signal wire (22) as one of the signal wires (22) and a pixel electrode section (12) as one of the pixel electrode sections (12) into a conducting state or a non-conducting state in accordance with a scanning signal supplied from a scanning signal line (21) as one of the scanning signal lines (21); and
a metal wire (13), connected to the switching element (25), through which when the switching element (25) is in a conducting state, a data signal from the signal wire (22) is supplied to the pixel electrode section (12), **characterized in that**
in a region of intersection between the alignment control space section (15) and the scanning signal line (21), a metal layer (19) is provided between a layer of the pixel section and a layer of the scanning signal line (21) in such a way as to cover at least the scanning signal line (21).

2. The active matrix substrate (10) as set forth in claim 1, further comprising an auxiliary capacitor line (14) that forms a capacitor with the pixel electrode section (12), wherein
in a region of intersection between the alignment control space section (15) and the auxiliary capacitor line (14), the metal layer (19) is provided between a layer of the pixel section and a layer of the auxiliary capacitor line (14) in such a way as to cover at least the auxiliary capacitor line (14).

3. The active matrix substrate (10) as set forth in claim 1 or 2, wherein the metal layer (19) is constituted to include at least either the metal wire (13) or the signal wire (22).

4. The active matrix substrate (10) as set forth in any one of claims 1 to 3, wherein the alignment control space section (15) is a long narrow hole formed individually in the pixel electrode section (12).

5. The active matrix substrate (10) as set forth in any one of claims 1 to 3, wherein the alignment control space section (15) is a space formed between one and another of the plurality of pixel electrode sections (12) constituting the pixel section.

6. The active matrix substrate (10) as set forth in any one of claims 1 to 3, wherein the alignment control space section (15) is a long narrow hole formed by making a cut in the pixel electrode section (12).

7. The active matrix substrate (10) as set forth in any one of claims 1 to 6, wherein the pixel electrode section (12) is a multi-pixel electrode including a plurality of subpixel electrodes and is driven by a pixel division method.

8. The active matrix substrate (10) as set forth in claim 2, wherein in the region of intersection between the alignment control space section (15) and the auxiliary capacitor line (14), a drain line serving as the metal wire (13) and extending from the switching element (25) formed in a corner portion of the pixel electrode section (12) to the auxiliary capacitor line

(14) disposed in such a way as to pass transversely across the pixel electrode section (12) is provided with a covering section (19) that covers at least the auxiliary capacitor line (14).

9. The active matrix substrate (10) as set forth in claim 2, wherein:

the scanning signal line (21) is disposed in such a way as to pass transversely across the pixel electrode section (12);
the auxiliary capacitor line (14) is disposed in such a way as to pass transversely across the pixel electrode section (12) substantially in parallel with the scanning signal line (21);
a drain line serving as the metal wire (13) extends from the switching element (25) formed in the pixel electrode section (12) to at least either the region of intersection between the alignment control space section (15) and the auxiliary capacitor line (14) disposed in such a way as to pass transversely across the pixel electrode section (12) or the region of intersection between the alignment control space section (15) and the scanning signal line (21); and
a covering section (19) that covers at least the auxiliary capacitor line (14) and the scanning signal line (21) in the respective regions is provided as part of the drain line (13).

10. The active matrix substrate (10) as set forth in claim 2, wherein:

the scanning signal line (21) is disposed in such a way as to pass transversely along an edge of the pixel electrode section (12);
the auxiliary capacitor line (14) is disposed in such a way as to pass transversely across a center of the pixel electrode section (12) substantially in parallel with the scanning signal line (21); and
a drain line serving as the metal wire (13) and extending from the switching element (25) formed in a corner portion of the pixel electrode section (12) to at least either the region of intersection between the alignment control space section (15) and the auxiliary capacitor line (14) disposed in such a way as to pass transversely across the pixel electrode section (12) or the region of intersection between the alignment control space section (15) and the scanning signal line (21) is provided with a covering section (19) that covers at least the auxiliary capacitor line (14) and the scanning signal line (21) in the respective regions.

11. The active matrix substrate (10) as set forth in claim 2, wherein:

the scanning signal line (21) is disposed in such a way as to pass transversely across a center of the pixel electrode section (12);
the auxiliary capacitor line (14) is disposed in such a way as to pass transversely along an edge of the pixel electrode section (12) substantially in parallel with the scanning signal line (21); and
a drain line serving as the metal wire (13) and extending from the switching element (25) formed in a side edge portion of the pixel electrode section (12) to at least either the region of intersection between the alignment control space section (15) and the auxiliary capacitor line (14) disposed in such a way as to pass transversely across the pixel electrode section (12) or the region of intersection between the alignment control space section (15) and the scanning signal line (21) is provided with a covering section (19) that covers at least the auxiliary capacitor line (14) and the scanning signal line (21) in the respective regions.

12. The active matrix substrate (10) as set forth in claim 10 or 11, wherein the pixel electrode section (12) has its longer sides extending substantially in parallel with the scanning signal line (21).

13. The active matrix substrate (10) as set forth in claim 2, wherein:

the auxiliary capacitor line (14) is provided in such a way as to overlap a site where another alignment control space section adjoining the alignment control space section (15) within each of the pixel electrode sections (12) are close to the alignment control space section (15) at a sharp angle; and
in the region of intersection between the auxiliary capacitor line (14) and those of the other alignment control space section and the alignment control space section (15), a drain line serving as the metal wire (13) and extending from the switching element (25) formed in a corner portion of the pixel electrode section (12) to the auxiliary capacitor line (14) is provided with a covering section (19) that covers at least the auxiliary capacitor line (14).

14. The active matrix substrate (10) as set forth in claim 2, wherein:

the auxiliary capacitor line (14) is provided in such a way as to pass transversely across the alignment control space section (15) formed as a space between the plurality of pixel electrode sections (12); and
in the region of intersection between the align-

ment control space section (15) and the auxiliary capacitor line (14), a drain line serving as the metal wire (13) and extending from the switching element (25) formed in a corner portion of the pixel electrode section (12) to the auxiliary capacitor line (14) is provided with a covering section (19) that covers at least the auxiliary capacitor line (14).

15. The active matrix substrate (10) as set forth in claim 2, wherein:

the auxiliary capacitor line (14) is provided in such a way as to pass transversely across the alignment control space section (15) formed as a space between the plurality of pixel electrode sections (12); and
in the region of intersection between the alignment control space section (15) and the auxiliary capacitor line (14), a data signal line serving as the signal line (22) and extending from the switching element (25) formed in a corner portion of the pixel electrode section (12) in such a way as to intersect with the auxiliary capacitor line (14) is provided with a covering section (19) that covers at least the auxiliary capacitor line (14).

16. The active matrix substrate (10) as set forth in claim 1, wherein in the region of intersection between the alignment control space section (15) and the scanning signal line (21), a drain line serving as the metal wire (13) and extending from the switching element (25) formed in the pixel electrode section (12) to the scanning signal line (21) disposed in such a way as to pass transversely across the pixel electrode section (12) is provided with a covering section (19) that covers at least the scanning signal line (21).

17. The active matrix substrate (10) as set forth in claim 1 or 2, wherein the alignment control space section (15) is formed in the pixel electrode section (12).

18. The active matrix substrate (10) as set forth in any one of claims 1 to 17, wherein a potential of the metal layer (19) is set so that any one of the following states of potential is formed:

(1) a first state of potential where a potential difference obtained by subtracting a potential of the common electrode (17), which is provided on a substrate opposite the active matrix substrate, from a potential of the metal layer (19) is opposite in polarity to a potential difference obtained by subtracting the potential of the common electrode (17) from a potential of the pixel electrode section (12);
(2) a second state of potential where the potential of the metal layer (19) is equal to the potential of the common electrode (17); and
(3) a third state of potential where the potential difference obtained by subtracting the potential of the common electrode (17) from the potential of the metal layer (19) is equal in polarity to the potential difference obtained by subtracting the potential of the common electrode (17) from the potential of the pixel electrode section (12) and where an absolute value of a difference between the potential of the pixel electrode section (12) and the potential of the common electrode (17) is greater than or equal to an absolute value of a difference between the potential of the metal layer (19) and the potential of the common electrode (17).

19. A liquid crystal display panel (2) comprising:

an active matrix substrate (10) as set forth in any one of claims 1 to 18;
a counter substrate (20) provided with a common electrode (17); and
a liquid crystal layer (30) sandwiched between the active matrix substrate (10) and the counter substrate (20).

20. The liquid crystal display panel (2) as set forth in claim 19, wherein the counter substrate (20) includes an alignment control section (18) that controls a state of alignment of liquid crystal molecules.

21. A liquid crystal display device (1) comprising:

a liquid crystal display panel (2) as set forth in claim 19 or 20; and
a driving circuit that drives the liquid crystal display panel (2).

22. A method for manufacturing an active matrix substrate (10) including (i) a plurality of scanning signal lines (21), (ii) a plurality of signal wires (22) disposed in such a way as to intersect with the scanning signal lines (21), (iii) a pixel section constituted by pixel electrode sections (12) each provided in correspondence with a combination of each of the scanning signal lines (21) and each of the signal wires (22), the pixel section having an alignment control space section (15) that controls a state of alignment of liquid crystal molecules, (iv) a switching element (25) that switches a signal wire (22) as one of the signal wires (22) and a pixel electrode section (12) as one of the pixel electrode sections (12) into a conducting state or a non-conducting state in accordance with a scanning signal supplied from a scanning signal line (21) as one of the scanning signal lines (21), and (v) a metal wire (13), connected to the switching element (25), through which when the switching element (25)

is in a conducting state, a data signal from the signal wire (22) is supplied to the pixel electrode section (12), **characterized in that**
the method comprising the step of, in a region of intersection between the alignment control space section (15) and the scanning signal line (21), forming a metal layer (19) between a layer of the pixel section and a layer of the scanning signal line (21) in such a way that the metal layer (19) covers at least the scanning signal line (21).

23. The method as set forth in claim 22, wherein the active matrix substrate (10) further comprises an auxiliary capacitor line (14) that forms a capacitor with the pixel electrode section (12),
the method comprising the step of, in a region of intersection between the alignment control space section (15) and the auxiliary capacitor line (14), forming a metal layer (19) between a layer of the pixel section and a layer of the auxiliary capacitor line (14) in such a way that the metal layer (19) covers at least the auxiliary capacitor line (14).

24. A method for manufacturing a liquid crystal display panel (2) as set forth in claim 19 or 20,
the method comprising a polymer alignment supporting step of giving a pretilt angle to liquid crystal molecules of the liquid crystal layer (30) by polymerizing monomers mixed in advance into the liquid crystal layer (30), with voltage being applied to the liquid crystal layer (30) in any one of the following states of potential: a first state of potential where a potential difference obtained by subtracting a potential of the common electrode (17) from a potential of the metal layer (19) is opposite in polarity to a potential difference obtained by subtracting the potential of the common electrode (17) from a potential of the pixel electrode section (12); a second state of potential where the potential of the metal layer (19) is equal to the potential of the common electrode (17); and a third state of potential where the potential difference obtained by subtracting the potential of the common electrode (17) from the potential of the metal layer (19) is equal in polarity to the potential difference obtained by subtracting the potential of the common electrode (17) from the potential of the pixel electrode section (12) and where an absolute value of a difference between the potential of the pixel electrode section (12) and the potential of the common electrode (17) is greater than or equal to an absolute value of a difference between the potential of the metal layer (19) and the potential of the common electrode (17).

25. A method for driving a liquid crystal display panel (2) as set forth in claim 19 or 20,
the method comprising applying voltage to the liquid crystal layer (30) in any one of the following states of potential: a first state of potential where a potential difference obtained by subtracting a potential of the common electrode (17) from a potential of the metal layer (19) is opposite in polarity to each other a potential difference obtained by subtracting the potential of the common electrode (17) from a potential of the pixel electrode section (12); a second state of potential where the potential of the metal layer (19) is equal to the potential of the common electrode (17); and a third state of potential where the potential difference obtained by subtracting the potential of the common electrode (17) from the potential of the metal layer (19) is equal in polarity to the potential difference obtained by subtracting the potential of the common electrode (17) from the potential of the pixel electrode section (12) and where an absolute value of a difference between the potential of the pixel electrode section (12) and the potential of the common electrode (17) is greater than or equal to an absolute value of a difference between the potential of the metal layer (19) and the potential of the common electrode (17).

Patentansprüche

1. Ein Aktiv-Matrix-Substrat (10), umfassend:

eine Mehrzahl an Scansignalleitungen (21);
eine Mehrzahl an Signalleitungen (22), welche so angeordnet sind, dass sie die Scansignalleitungen (21) kreuzen;
einen Pixelabschnitt gebildet aus Pixelelektrodenabschnitten (12), welche jeweils zugehörig zu einer Kombination aus jeweils einer Scansignalleitung (21) und jeweils einer Signalleitung (22) ausgestaltet sind, wobei der Pixelabschnitt einen Ausrichtungssteuerraumabschnitt (15) aufweist, welcher einen Ausrichtungszustand von Flüssigkristallmolekülen steuert;
ein Schaltelement (25), welches eine Signalleitung (22) der Signalleitungen (22) und einen Pixelelektrodenabschnitt (12) der Pixelelektrodenabschnitte (12) in einen leitenden Zustand oder einen nichtleitenden Zustand gemäß einem von einer Scansignalleitung (21) der Scansignalleitungen (21) zugeführten Scansignal schaltet; und
eine mit dem Schaltelement (25) verbundene Metallleitung (13), durch welche ein Datensignal von der Signalleitung (22) dem Pixelelektrodenabschnitt (12) zugeführt wird, wenn sich das Schaltelement (25) in einem leitenden Zustand befindet, **dadurch gekennzeichnet, dass**
in einer Kreuzungsregion zwischen dem Ausrichtungssteuerraumabschnitt (15) und der Scansignalleitung (21) eine Metallschicht (19) zwischen einer Schicht des Pixelabschnitts und

einer Schicht der Scansignalleitung (21) so ausgebildet ist, dass sie zumindest die Scansignalleitung (21) bedeckt.

2. Das Aktiv-Matrix-Substrat (10) wie in Anspruch 1, ferner umfassend eine Hilfskondensatorleitung (14), welche einen Kondensator mit dem Pixelelektrodenabschnitt (12) bildet, wobei
in einer Kreuzungsregion zwischen dem Ausrichtungssteuerraumabschnitt (15) und der Hilfskondensatorleitung (14) die Metallschicht (19) zwischen einer Schicht des Pixelabschnitts und einer Schicht der Hilfskondensatorleitung (14) so ausgebildet ist, dass sie zumindest die Hilfskondensatorleitung (14) bedeckt.

3. Das Aktiv-Matrix-Substrat (10) wie in Anspruch 1 oder 2, wobei die Metallschicht (19) so ausgebildet ist, dass sie zumindest entweder die Metallleitung (13) oder die Signalleitung (22) umfasst.

4. Das Aktiv-Matrix-Substrat (10) wie in einem der Ansprüche 1 bis 3, wobei der Ausrichtungssteuerraumabschnitt (15) ein langes schmales Loch ist, welches individuell in dem Pixelelektrodenabschnitt (12) gebildet ist.

5. Das Aktiv-Matrix-Substrat (10) wie in einem der Ansprüche 1 bis 3, wobei der Ausrichtungssteuerraumabschnitt (15) ein zwischen einem und einem anderen der Mehrzahl an Pixelelektrodenabschnitten (12), welche den Pixelabschnitt bilden, gebildeter Raum ist.

6. Das Aktiv-Matrix-Substrat (10) wie in einem der Ansprüche 1 bis 3, wobei der Ausrichtungssteuerraumabschnitt (15) ein langes schmales Loch ist, welches durch Ausführen eines Schnitts in den Pixelelektrodenabschnitt (12) gebildet ist.

7. Das Aktiv-Matrix-Substrat (10) wie in einem der Ansprüche 1 bis 6, wobei der Pixelelektrodenabschnitt (12) eine Multi-Pixel-Elektrode ist, welche eine Mehrzahl an Subpixel-Elektroden umfasst und durch ein Pixelteilungsverfahren angesteuert wird.

8. Das Aktiv-Matrix-Substrat (10) wie in Anspruch 2, wobei in der Kreuzungsregion zwischen dem Ausrichtungssteuerraumabschnitt (15) und der Hilfskondensatorleitung (14) eine Drain-Leitung, welche als die Metallleitung (13) dient und sich von dem in einem Eckbereich des Pixelelektrodenabschnitts (12) gebildeten Schaltelement (25) zu der Hilfskondensatorleitung (14) erstreckt, welche so angeordnet ist, dass sie quer über den Pixelelektrodenabschnitt (12) verläuft, mit einem Bedeckungsabschnitt (19) ausgebildet ist, welcher zumindest die Hilfskondensatorleitung (14) bedeckt.

9. Das Aktiv-Matrix-Substrat (10) wie in Anspruch 2, wobei:

die Scansignalleitung (21) so angeordnet ist, dass sie quer über den Pixelelektrodenabschnitt (12) verläuft;
die Hilfskondensatorleitung (14) so angeordnet ist, dass sie quer über den Pixelelektrodenabschnitt (12) und im Wesentlichen parallel zu der Scansignalleitung (21) verläuft;
eine Drain-Leitung, welche als die Metallleitung (13) dient, sich von dem in dem Pixelelektrodenabschnitt (12) gebildeten Schaltelement (25) zu zumindest entweder der Kreuzungsregion zwischen dem Ausrichtungssteuerraumabschnitt (15) und der quer über den Pixelelektrodenabschnitt (12) verlaufenden Hilfskondensatorleitung (14) oder der Kreuzungsregion zwischen dem Ausrichtungssteuerraumabschnitt (15) und der Scansignalleitung (21) erstreckt; und
ein Bedeckungsabschnitt (19), welcher zumindest die Hilfskondensatorleitung (14) und die Scansignalleitung (21) in den entsprechenden Regionen bedeckt, als Teil der Drain-Leitung (13) ausgebildet ist.

10. Das Aktiv-Matrix-Substrat (10) wie in Anspruch 2, wobei:

die Scansignalleitung (21) so angeordnet ist, dass sie quer entlang einer Kante des Pixelelektrodenabschnitts (12) verläuft;
die Hilfskondensatorleitung (14) so angeordnet ist, dass sie quer über eine Mitte des Pixelelektrodenabschnitts (12) und im Wesentlichen parallel zu der Scansignalleitung (21) verläuft; und
eine Drain-Leitung, welche als die Metallleitung (13) dient und sich von dem in einem Eckbereich des Pixelelektrodenabschnitts (12) gebildeten Schaltelement (25) zu zumindest entweder der Kreuzungsregion zwischen dem Ausrichtungssteuerraumabschnitt (15) und der quer über den Pixelelektrodenabschnitt (12) verlaufenden Hilfskondensatorleitung (14) oder der Kreuzungsregion zwischen dem Ausrichtungssteuerraumabschnitt (15) und der Scansignalleitung (21) erstreckt, mit einem Bedeckungsabschnitt (19) ausgebildet ist, der zumindest die Hilfskondensatorleitung (14) und die Scansignalleitung (21) in den entsprechenden Regionen bedeckt.

11. Das Aktiv-Matrix-Substrat (10) wie in Anspruch 2, wobei:

die Scansignalleitung (21) so angeordnet ist, dass sie quer über eine Mitte des Pixelelektrodenabschnitts (12) verläuft;
die Hilfskondensatorleitung (14) so angeordnet

ist, dass sie quer entlang einer Kante des Pixelelektrodenabschnitts (12) und im Wesentlichen parallel zu der Scansignalleitung (21) verläuft; und

eine Drain-Leitung, welche als die Metallleitung (13) dient und sich von dem in einem Seitenkantenbereich des Pixelelektrodenabschnitts (12) gebildeten Schaltelement (25) zu zumindest entweder der Kreuzungsregion zwischen dem Ausrichtungssteuerraumabschnitt (15) und der quer über den Pixelelektrodenabschnitt (12) verlaufenden Hilfskondensatorleitung (14) oder der Kreuzungsregion zwischen dem Ausrichtungssteuerraumabschnitt (15) und der Scansignalleitung (21) erstreckt, mit einem Bedeckungsabschnitt (19) ausgebildet ist, der zumindest die Hilfskondensatorleitung (14) und die Scansignalleitung (21) in den entsprechenden Regionen bedeckt.

12. Das Aktiv-Matrix-Substrat (10) wie in Anspruch 10 oder 11, wobei sich die längeren Seiten des Pixelelektrodenabschnitts (12) im Wesentlichen parallel zu der Scansignalleitung (21) erstrecken.

13. Das Aktiv-Matrix-Substrat (10) wie in Anspruch 2, wobei:

die Hilfskondensatorleitung (14) so ausgestaltet ist, dass sie eine Stelle überlappt, wo ein an den Ausrichtungssteuerraumabschnitt (15) angrenzender anderer Ausrichtungssteuerraumabschnitt innerhalb jeder der Pixelelektrodenabschnitte (12) nahe zu dem Ausrichtungssteuerraumabschnitt (15) unter einem spitzen Winkel ist; und

in der Kreuzungsregion zwischen der Hilfskondensatorleitung (14) und jener des anderen Ausrichtungssteuerraumabschnitts und des Ausrichtungssteuerraumabschnitts (15), eine Drain-Leitung, welche als die Metallleitung (13) dient und sich von dem in einem Eckbereich des Pixelelektrodenabschnitts (12) gebildeten Schaltelement (25) zu der Hilfskondensatorleitung (14) erstreckt, mit einem Bedeckungsabschnitt (19) ausgebildet ist, der zumindest die Hilfskondensatorleitung (14) bedeckt.

14. Das Aktiv-Matrix-Substrat (10) wie in Anspruch 2, wobei:

die Hilfskondensatorleitung (14) so ausgestaltet ist, dass sie quer über den als ein Raum zwischen der Mehrzahl an Pixelelektrodenabschnitten (12) gebildeten Ausrichtungssteuerraumabschnitt (15) verläuft; und

in der Kreuzungsregion zwischen dem Ausrichtungssteuerraumabschnitt (15) und der Hilfskondensatorleitung (14), eine Drain-Leitung, welche als die Metallleitung (13) dient und sich von dem in einem Eckbereich des Pixelelektrodenabschnitts (12) gebildeten Schaltelement (25) zu der Hilfskondensatorleitung (14) erstreckt, mit einem Bedeckungsabschnitt (19) ausgebildet ist, der zumindest die Hilfskondensatorleitung (14) bedeckt.

15. Das Aktiv-Matrix-Substrat (10) wie in Anspruch 2, wobei:

die Hilfskondensatorleitung (14) so ausgestaltet ist, dass sie quer über den als ein Raum zwischen der Mehrzahl an Pixelelektrodenabschnitten (12) gebildeten Ausrichtungssteuerraumabschnitt (15) verläuft; und

in der Kreuzungsregion zwischen dem Ausrichtungssteuerraumabschnitt (15) und der Hilfskondensatorleitung (14), eine Datensignalleitung, welche als die Signalleitung (22) dient und sich von dem in einem Eckbereich des Pixelelektrodenabschnitts (12) gebildeten Schaltelement (25) so erstreckt, dass sie die Hilfskondensatorleitung (14) kreuzt, mit einem Bedeckungsabschnitt (19) ausgebildet ist, der zumindest die Hilfskondensatorleitung (14) bedeckt.

16. Das Aktiv-Matrix-Substrat (10) wie in Anspruch 1, wobei in der Kreuzungsregion zwischen dem Ausrichtungssteuerraumabschnitt (15) und der Scansignalleitung (21), eine Drain-Leitung, welche als die Metallleitung (13) dient und sich von dem in dem Pixelelektrodenabschnitt (12) gebildeten Schaltelement (25) zu der Scansignalleitung (21) erstreckt, welche so angeordnet ist, dass sie quer über den Pixelelektrodenabschnitt (12) verläuft, mit einem Bedeckungsabschnitt (19) ausgebildet ist, der zumindest die Scansignalleitung (21) bedeckt.

17. Das Aktiv-Matrix-Substrat (10) wie in Anspruch 1 oder 2, wobei der Ausrichtungssteuerraumabschnitt (15) in dem Pixelelektrodenabschnitt (12) gebildet ist.

18. Das Aktiv-Matrix-Substrat (10) wie in einem der Ansprüche 1 bis 17, wobei ein Potential der Metallschicht (19) so festgelegt ist, dass einer der folgenden Potentialzustände gebildet wird:

(1) ein erster Potentialzustand, wo eine Potentialdifferenz, welche durch Subtrahieren eines Potentials der gemeinsamen Elektrode (17), welche auf einem Substrat gegenüber dem Aktiv-Matrix-Substrat (10) ausgebildet ist, von einem Potential der Metallschicht (19) erhalten wird, an Polarität entgegengesetzt ist zu einer Potentialdifferenz, welche durch Subtrahieren

des Potentials der gemeinsamen Elektrode (17) von einem Potential des Pixelelektrodenabschnitts (12) erhalten wird;
(2) ein zweiter Potentialzustand, wo das Potential der Metallschicht (19) gleich ist zu dem Potential der gemeinsamen Elektrode (17); und
(3) ein dritter Potentialzustand, wo die Potentialdifferenz, welche durch Subtrahieren des Potentials der gemeinsamen Elektrode (17) von dem Potential der Metallschicht (19) erhalten wird, an Polarität gleich ist zu der Potentialdifferenz, welche durch Subtrahieren des Potentials der gemeinsamen Elektrode (17) von dem Potential des Pixelelektrodenabschnitts (12) erhalten wird und wo ein absoluter Wert einer Differenz zwischen dem Potential des Pixelelektrodenabschnitts (12) und dem Potential der gemeinsamen Elektrode (17) größer oder gleich ist wie ein absoluter Wert einer Differenz zwischen dem Potential der Metallschicht (19) und dem Potential der gemeinsamen Elektrode (17).

19. Eine Flüssigkristalltafel (2), umfassend:

ein Aktiv-Matrix-Substrat (10) wie in einem der Ansprüche 1 bis 18;
ein mit einer gemeinsamen Elektrode (17) ausgebildetes Gegensubstrat (20); und
eine zwischen dem Aktiv-Matrix-Substrat (10) und dem Gegensubstrat (20) angeordnete Flüssigristallschicht (30).

20. Die Flüssigkristalltafel (2) wie in Anspruch 19, wobei das Gegensubstrat (20) einen Ausrichtungssteuerabschnitt (18) umfasst, welcher einen Ausrichtungszustand von Flüssigkristallmolekülen steuert.

21. Eine Flüssigkristallanzeigevorrichtung (1), umfassend:

eine Flüssigkristalltafel (2) wie in Anspruch 19 oder 20; und
einen Steuerschaltkreis, welcher die Flüssigkristalltafel (2) ansteuert.

22. Ein Verfahren zum Herstellen eines Aktiv-Matrix-Substrats (10) umfassend (i) eine Mehrzahl an Scansignalleitungen (21), (ii) eine Mehrzahl an Signalleitungen (22), welche so angeordnet sind, dass sie die Scansignalleitungen (21) kreuzen, (iii) einen Pixelabschnitt gebildet aus Pixelelektrodenabschnitten (12), welche jeweils zugehörig zu einer Kombination aus jeweils einer Scansignalleitung (21) und jeweils einer Signalleitung (22) ausgestaltet sind, wobei der Pixelabschnitt einen Ausrichtungssteuerraumabschnitt (15) aufweist, welcher einen Ausrichtungszustand von Flüssigkristallmolekülen steuert, (iv) ein Schaltelement (25), welches eine Signalleitung (22) der Signalleitungen (22) und einen Pixelelektrodenabschnitt (12) der Pixelelektrodenabschnitte (12) in einen leitenden Zustand oder einen nichtleitenden Zustand gemäß einem von einer Scansignalleitung (21) der Scansignalleitungen (21) zugeführten Scansignal schaltet, und (v) einer mit dem Schaltelement (25) verbundenen Metallleitung (13), durch welche ein Datensignal von der Signalleitung (22) dem Pixelelektrodenabschnitt (12) zugeführt wird, wenn sich das Schaltelement (25) in einem leitenden Zustand befindet, **dadurch gekennzeichnet, dass**
das Verfahren den Schritt aufweist von Formen, in einer Kreuzungsregion zwischen dem Ausrichtungssteuerraumabschnitt (15) und der Scansignalleitung (21), einer Metallschicht (19) zwischen einer Schicht des Pixelabschnitts und einer Schicht der Scansignalleitung (21), so dass die Metallschicht (19) zumindest die Scansignalleitung (21) bedeckt.

23. Das Verfahren wie in Anspruch 22, wobei das Aktiv-Matrix-Substrat (10) ferner eine Hilfskondensatorleitung (14) umfasst, welche einen Kondensator mit dem Pixelelektrodenabschnitt (12) bildet, wobei
das Verfahren den Schritt aufweist von Formen, in einer Kreuzungsregion zwischen dem Ausrichtungssteuerraumabschnitt (15) und der Hilfskondensatorleitung (14), einer Metallschicht (19) zwischen einer Schicht des Pixelabschnitts und einer Schicht der Hilfskondensatorleitung (14), so dass die Metallschicht (19) zumindest die Hilfskondensatorleitung (14) bedeckt.

24. Ein Verfahren zum Herstellen einer Flüssigkristalltafel (2) wie in Anspruch 19 oder 20,
wobei das Verfahren einen Polymerausrichtungsunterstützungsschritt des Setzens eines Vor-Neigungswinkels der Flüssigkristallmoleküle der Flüssigkristallschicht (30) durch Polymerisieren von im Vorhinein in die Flüssigkristallschicht (30) gemischten Monomeren umfasst, wobei eine Spannung an die Flüssigkristallschicht (30) in einer der folgenden Potentialzustände angelegt wird: ein erster Potentialzustand, wo eine Potentialdifferenz, welche durch Subtrahieren eines Potentials der gemeinsamen Elektrode (17) von einem Potential der Metallschicht (19) erhalten wird, an Polarität entgegengesetzt ist zu einer Potentialdifferenz, welche durch Subtrahieren des Potentials der gemeinsamen Elektrode (17) von einem Potential des Pixelelektrodenabschnitts (12) erhalten wird; ein zweiter Potentialzustand, wo das Potential der Metallschicht (19) gleich ist zu dem Potential der gemeinsamen Elektrode (17); und ein dritter Potentialzustand, wo die Potentialdifferenz, welche durch Subtrahieren des Potentials der gemeinsamen Elektrode (17) von dem Potential der Metallschicht (19) erhalten wird, an Polarität gleich ist zu der Potentialdifferenz, welche durch Subtra-

hieren des Potentials der gemeinsamen Elektrode (17) von dem Potential des Pixelelektrodenabschnitts (12) erhalten wird und wo ein absoluter Wert einer Differenz zwischen dem Potential des Pixelelektrodenabschnitts (12) und dem Potential der gemeinsamen Elektrode (17) größer oder gleich ist wie ein absoluter Wert einer Differenz zwischen dem Potential der Metallschicht (19) und dem Potential der gemeinsamen Elektrode (17).

25. Ein Verfahren zum Ansteuern einer Flüssigkristalltafel (2) wie in Anspruch 19 oder 20,
wobei das Verfahren Anlegen einer Spannung an die Flüssigkristallschicht (30) in einem der folgenden Potentialzustände umfasst: ein erster Potentialzustand, wo eine Potentialdifferenz, welche durch Subtrahieren eines Potentials der gemeinsamen Elektrode (17) von einem Potential der Metallschicht (19) erhalten wird, an Polarität entgegengesetzt ist zu einer Potentialdifferenz, welche durch Subtrahieren des Potentials der gemeinsamen Elektrode (17) von einem Potential des Pixelelektrodenabschnitts (12) erhalten wird; ein zweiter Potentialzustand, wo das Potential der Metallschicht (19) gleich ist zu dem Potential der gemeinsamen Elektrode (17); und ein dritter Potentialzustand, wo die Potentialdifferenz, welche durch Subtrahieren des Potentials der gemeinsamen Elektrode (17) von dem Potential der Metallschicht (19) erhalten wird, an Polarität gleich ist zu der Potentialdifferenz, welche durch Subtrahieren des Potentials der gemeinsamen Elektrode (17) von dem Potential des Pixelelektrodenabschnitts (12) erhalten wird und wo ein absoluter Wert einer Differenz zwischen dem Potential des Pixelelektrodenabschnitts (12) und dem Potential der gemeinsamen Elektrode (17) größer oder gleich ist wie ein absoluter Wert einer Differenz zwischen dem Potential der Metallschicht (19) und dem Potential der gemeinsamen Elektrode (17).

Revendications

1. Substrat de matrice active (10) comprenant :

plusieurs lignes de signaux de balayage (21) ;
plusieurs fils de signaux (22) disposés de manière à couper les lignes de signaux de balayage (21) ;
une section de pixels constituée par des sections d'électrodes de pixels (12) prévues chacune pour correspondre à une combinaison de chacune des lignes de signaux de balayage (21) et de chacun des fils de signaux (22), la section de pixels présentant une section d'espace de commande d'alignement (15) qui commande un état d'alignement de molécules de cristaux liquides ;
un élément de commutation (25) qui fait passer un fil de signaux (22), comme l'un des fils de signaux (22), et une section d'électrode de pixels (12), comme l'une des sections d'électrodes de pixels (12) à un état conducteur ou à un état non conducteur suivant un signal de balayage fourni à partir d'une ligne de signaux de balayage (21), comme l'une des lignes de signaux de balayage (21) ; et
un fil de métal (13), relié à l'élément de commutation (25), grâce auquel, quand l'élément de commutation (25) est dans un état conducteur, un signal de données provenant du fil de signaux (22) est fourni à la section d'électrode de pixels (12), **caractérisé en ce que**
dans une zone d'intersection entre la section d'espace de commande d'alignement (15) et la ligne de signaux de balayage (21), une couche de métal (19) est prévue entre une couche de la section de pixels et une couche de la ligne de signaux de balayage (21) de manière à couvrir au moins la ligne de signaux de balayage (21).

2. Substrat de matrice active (10) tel qu'il est présenté dans la revendication 1, comprenant par ailleurs une ligne de condensateur auxiliaire (14) qui forme un condensateur avec la section d'électrode de pixels (12), étant précisé
que dans une zone d'intersection entre la section d'espace de commande d'alignement (15) et la ligne de condensateur auxiliaire (14), la couche de métal (19) est prévue entre une couche de la section de pixels et une couche de la ligne de condensateur auxiliaire (14) de manière à couvrir au moins la ligne de condensateur auxiliaire.

3. Substrat de matrice active (10) tel qu'il est présenté dans la revendication 1 ou 2, étant précisé que la couche de métal (19) est constituée de manière à inclure au moins le fil de métal (13) ou le fil de signaux (22).

4. Substrat de matrice active (10) tel qu'il est présenté dans l'une quelconque des revendications 1 à 3, étant précisé que la section d'espace de commande d'alignement (15) est un long trou étroit qui est formé individuellement dans la section d'électrode de pixels (12).

5. Substrat de matrice active (10) tel qu'il est présenté dans l'une quelconque des revendications 1 à 3, étant précisé que la section d'espace de commande d'alignement (15) est un espace formé entre une section d'électrode de pixels (12) et une autre desdites sections (12) constituant la section de pixels.

6. Substrat de matrice active (10) tel qu'il est présenté dans l'une quelconque des revendications 1 à 3,

étant précisé que la section d'espace de commande d'alignement (15) est un long trou étroit formé grâce à une coupe dans la section d'électrode de pixels (12).

7. Substrat de matrice active (10) tel qu'il est présenté dans l'une quelconque des revendications 1 à 6, étant précisé que la section d'électrode de pixels (12) est une électrode multipixel comprenant plusieurs électrodes de sous-pixels et est commandée par un procédé de division de pixels.

8. Substrat de matrice active (10) tel qu'il est présenté dans la revendication 2, étant précisé que dans la zone d'intersection entre la section d'espace de commande d'alignement (15) et la ligne de condensateur auxiliaire (14), une ligne de drain servant de fil de métal (13) et s'étendant de l'élément de commutation (25) formé dans une partie de coin de la section d'électrode de pixels (12) jusqu'à la ligne de condensateur auxiliaire (14) disposée de manière à passer transversalement sur la section d'électrode de pixels (12) est pourvue d'une section de recouvrement (19) qui recouvre la ligne de condensateur auxiliaire (14).

9. Substrat de matrice active (10) tel qu'il est présenté dans la revendication 2, étant précisé :

que la ligne de signaux de balayage (21) est disposée de manière à passer transversalement sur la section d'électrode de pixels (12) ;
que la ligne de condensateur auxiliaire (14) est disposée de manière à passer transversalement sur la section d'électrode de pixels (12) globalement parallèlement à la ligne de signaux de balayage (21) ;
qu'une ligne de drainage servant de fil de métal (13) s'étend de l'élément de commutation (25) formé dans la section d'électrode de pixels (12) jusqu'à au moins la zone d'intersection entre la section d'espace de commande d'alignement (15) et la ligne de condensateur auxiliaire (14) disposée de manière à passer transversalement sur la section d'électrode de pixels (12), ou la zone d'intersection entre la section d'espace de commande d'alignement (15) et la ligne de signaux de balayage (21) ; et
qu'une section de recouvrement (19) qui recouvre au moins la ligne de condensateur auxiliaire (14) et la ligne de signaux de balayage (21) dans les zones respectives est prévue comme faisant partie de la ligne de drain (13).

10. Substrat de matrice active (10) tel qu'il est présenté dans la revendication 2, étant précisé :

que la ligne de signaux de balayage (21) est disposée de manière à passer transversalement le long d'un bord de la section d'électrode de pixels (12) ;
que la ligne de condensateur auxiliaire (14) est disposée de manière à passer transversalement sur un centre de la section d'électrode de pixels (12) globalement parallèlement à la ligne de signaux de balayage (21) ; et
qu'une ligne de drain servant de fil de métal (13) et s'étendant de l'élément de commutation (25) formé dans une partie de coin de la section d'électrode de pixels (12) jusqu'à au moins la zone d'intersection entre la section d'espace de commande d'alignement (15) et la ligne de condensateur auxiliaire (14) disposée de manière à passer transversalement sur la section d'électrode de pixels (12), ou la zone d'intersection entre la section d'espace de commande d'alignement (15) et la ligne de signaux de balayage (21) est pourvue d'une section de recouvrement (19) qui recouvre au moins la ligne de condensateur auxiliaire (14) et la ligne de signaux de balayage (21) dans les zones respectives.

11. Substrat de matrice active (10) tel qu'il est présenté dans la revendication 2, étant précisé :

que la ligne de signaux de balayage (21) est disposée de manière à passer transversalement sur un centre de la section d'électrode de pixels (12) ;
que la ligne de condensateur auxiliaire (14) est disposée de manière à passer transversalement le long d'un bord de la section d'électrode de pixels (12) globalement parallèlement à la ligne de signaux de balayage (21) ; et
qu'une ligne de drain servant de fil de métal (13) et s'étendant de l'élément de commutation (25) formé dans une partie de coin latérale de la section d'électrode de pixels (12) jusqu'à au moins la zone d'intersection entre la section d'espace de commande d'alignement (15) et la ligne de condensateur auxiliaire (14) disposée de manière à passer transversalement sur la section d'électrode de pixels (12), ou la zone d'intersection entre la section d'espace de commande d'alignement (15) et la ligne de signaux de balayage (21) est pourvue d'une section de recouvrement (19) qui recouvre au moins la ligne de condensateur auxiliaire (14) et la ligne de signaux de balayage (21) dans les zones respectives.

12. Substrat de matrice active (10) tel qu'il est présenté dans la revendication 10 ou 11, étant précisé que les côtés longs de la section d'électrode de pixels (12) s'étendent globalement parallèlement à la ligne de signaux de balayage (21).

13. Substrat de matrice active (10) tel qu'il est présenté dans la revendication 2, étant précisé :

que la ligne de condensateur auxiliaire (14) est prévue de manière à couvrir un endroit où une autre section d'espace de commande d'alignement voisine de la section d'espace d'alignement (15) à l'intérieur de chacune des sections d'électrodes de pixels (12) sont proches de la section d'espace de commande d'alignement (15) suivant un angle aigu ; et
que dans la zone d'intersection entre la ligne de condensateur auxiliaire (14), et l'autre section d'espace de commande d'alignement et la section d'espace de commande d'alignement (15), une ligne de drain servant de fil de métal (13) et s'étendant de l'élément de commutation (25) formé dans une partie de coin de la section d'électrode de pixels (12) jusqu'à la ligne de condensateur auxiliaire (14) est pourvue d'une section de recouvrement (19) qui recouvre au moins la ligne de condensateur auxiliaire (14).

14. Substrat de matrice active (10) tel qu'il est présenté dans la revendication 2, étant précisé :

que la ligne de condensateur auxiliaire (14) est prévue de manière à passer transversalement sur la section d'espace de commande d'alignement (15) formée sous la forme d'un espace entre plusieurs sections d'électrodes de pixels (12) ; et
que dans la zone d'intersection entre la section d'espace de commande d'alignement (15) et la ligne de condensateur auxiliaire (14), une ligne de drain servant de fil de métal (13) et s'étendant de l'élément de commutation (25) formé dans une partie de coin de la section d'électrode de pixels (12) jusqu'à la ligne de condensateur auxiliaire (14) est pourvue d'une section de recouvrement (19) qui recouvre au moins la ligne de condensateur auxiliaire (14).

15. Substrat de matrice active (10) tel qu'il est présenté dans la revendication 2, étant précisé :

que la ligne de condensateur auxiliaire (14) est prévue de manière à passer transversalement sur la section d'espace de commande d'alignement (15) formée sous la forme d'un espace entre les sections d'électrodes de pixels (12) ; et
que dans la zone d'intersection entre la section d'espace de commande d'alignement (15) et la ligne de condensateur auxiliaire (14), une ligne de signaux de données servant de ligne de signaux (22) et s'étendant à partir de l'élément de commutation (25) formé dans une partie de coin de la section d'électrode de pixels (12) de manière à couper la ligne de condensateur auxiliaire (14) est pourvue d'une section de recouvrement (19) qui recouvre au moins la ligne de condensateur auxiliaire (14).

16. Substrat de matrice active (10) tel qu'il est présenté dans la revendication 1, étant précisé que dans la zone d'intersection entre la section d'espace de commande d'alignement (15) et la ligne de signaux de balayage (21), une ligne de drain servant de fil de métal (13) et s'étendant de l'élément de commutation (25) formé dans la section d'électrode de pixels (12) jusqu'à la ligne de signaux de balayage (21) disposée de manière à passer transversalement sur la section d'électrode de pixels (12) est pourvue d'une section de recouvrement (19) qui recouvre au moins la lige de signaux de balayage (21).

17. Substrat de matrice active (10) tel qu'il est présenté dans la revendication 1 ou 2, étant précisé que la section d'espace de commande d'alignement (15) est formée dans la section d'électrode de pixels (12).

18. Substrat de matrice active (10) tel qu'il est présenté dans l'une quelconque des revendications 1 à 17, étant précisé qu'un potentiel de la couche de métal (19) est fixé de telle sorte que l'un quelconque des états de potentiel soit formé :

(1) un premier état de potentiel dans lequel une différence de potentiel obtenue en soustrayant un potentiel de l'électrode commune (17), qui est disposée sur un substrat opposé au substrat de matrice active, d'un potentiel de la couche de métal (19) est opposée en polarité à une différence de potentiel obtenue en soustrayant le potentiel de l'électrode commune (17) d'un potentiel de la section d'électrode de pixels (12) ;
(2) un deuxième état de potentiel dans lequel le potentiel de la couche de métal (19) est égal au potentiel de l'électrode commune (17) ; et
(3) un troisième état de potentiel dans lequel la différence de potentiel obtenue en soustrayant le potentiel de l'électrode commune (17) du potentiel de la couche de métal (19) est égale en polarité à la différence de potentiel obtenue en soustrayant le potentiel de l'électrode commune (17) du potentiel de la section d'électrode de pixels (12), et dans lequel une valeur absolue d'une différence entre le potentiel de la section d'électrode de pixels (12) et le potentiel de l'électrode commune (17) est supérieure ou égale à une valeur absolue d'une différence entre le potentiel de la couche de métal (19) et le potentiel de l'électrode commune (17).

19. Panneau d'affichage à cristaux liquides (2) comprenant :

un substrat de matrice active (10) tel qu'il est présenté dans l'une quelconque des revendications 1 à 18 ;
un contre-substrat (20) pourvu d'une électrode commune (17) ; et
une couche de cristaux liquides (30) placée en sandwich entre le substrat de matrice active (10) et le contre-substrat (20).

20. Panneau d'affichage à cristaux liquides (2) tel qu'il est présenté dans la revendication 19, étant précisé que le contre-substrat (20) contient une section de commande d'alignement (18) qui commande un état d'alignement de molécules de cristaux liquides.

21. Disposition d'affichage à cristaux liquides (1) comprenant :

un panneau d'affichage à cristaux liquides (2) tel qu'il est présenté dans la revendication 19 ou 20 ; et
un circuit d'attaque qui attaque le panneau d'affichage à cristaux liquides (2).

22. Procédé pour fabriquer un substrat de matrice active (10) comprenant (i) plusieurs lignes dé signaux de balayage (21), (ii) plusieurs fils de signaux (22) disposés de manière à couper les lignes de signaux de balayage (21) ; (iii) une section de pixels constituée par des sections d'électrodes de pixels (12) prévues chacune pour correspondre à une combinaison de chacune des lignes de signaux de balayage (21) et de chacun des fils de signaux (22), la section de pixels présentant une section d'espace de commande d'alignement (15) qui commande un état d'alignement de molécules de cristaux liquides, (iv) un élément de commutation (25) qui fait passer un fil de signaux (22), comme l'un des fils de signaux (22), et une section d'électrode de pixels (12), comme l'une des sections d'électrodes de pixels (12) à un état conducteur ou à un état non conducteur suivant un signal de balayage fourni à partir d'une ligne de signaux de balayage (21), comme l'une des lignes de signaux de balayage (21), et (v) un fil de métal (13), relié à l'élément de commutation (25), grâce auquel, quand l'élément de commutation (25) est dans un état conducteur, un signal de données provenant du fil de signaux (22) est fourni à la section d'électrode de pixels (12), **caractérisé en ce que** le procédé comprend l'étape de formation, dans une zone d'intersection entre la section d'espace de commande d'alignement (15) et la ligne de signaux de balayage (21), d'une couche de métal (19) entre une couche de la section de pixels et une couche de la ligne de signaux de balayage (21) de telle sorte que ladite couche de métal (19) couvre au moins la ligne de signaux de balayage (21).

23. Procédé tel qu'il est présenté dans la revendication 22, étant précisé que le substrat de matrice active (10) comprend par ailleurs une ligne de condensateur auxiliaire (14) qui forme un condensateur avec la section d'électrode de pixels (12),
le procédé comprenant l'étape de formation, dans une zone d'intersection entre la section d'espace de commande d'alignement (15) et la ligne de condensateur auxiliaire (14), d'une couche de métal (19) entre une couche de la section de pixels et une couche de la ligne de condensateur auxiliaire (14) de telle sorte que ladite couche de métal (19) couvre au moins la ligne de condensateur auxiliaire.

24. Procédé pour fabriquer un panneau d'affichage de cristaux liquides (2) tel qu'il est présenté dans la revendication 19 ou 20, le procédé comprenant une étape de renforcement d'alignement de polymère qui consiste à donner un angle de préinclinaison aux molécules de cristaux liquides de la couche de cristaux liquides (30) en polymérisant des monomères mélangés à l'avance à la couche de cristaux liquides (30), une tension étant appliquée à la couche de cristaux liquides (30) dans l'un quelconque des états de potentiel suivants : un premier état de potentiel dans lequel une différence de potentiel obtenue en soustrayant un potentiel de l'électrode commune (17) d'un potentiel de la couche de métal (19) est opposée en polarité à une différence de potentiel obtenue en soustrayant le potentiel de l'électrode commune (17) d'un potentiel de la section d'électrode de pixels (12) ; un deuxième état de potentiel dans lequel le potentiel de la couche de métal (19) est égal au potentiel de l'électrode commune (17) ; et un troisième état de potentiel dans lequel la différence de potentiel obtenue en soustrayant le potentiel de l'électrode commune (17) du potentiel de la couche de métal (19) est égale en polarité à la différence de potentiel obtenue en soustrayant le potentiel de l'électrode commune (17) du potentiel de la section d'électrode de pixels (12), et dans lequel une valeur absolue d'une différence entre le potentiel de la section d'électrode de pixels (12) et le potentiel de l'électrode commune (17) est supérieure ou égale à une valeur absolue d'une différence entre le potentiel de la couche de métal (19) et le potentiel de l'électrode commune (17).

25. Procédé pour commander un panneau d'affichage à cristaux liquides (2) tel qu'il est présenté dans la revendication 19 ou 20,
le procédé comprenant l'application d'une tension à la couche de cristaux liquides (30) dans l'un quelconque des états de potentiel suivants : un premier état de potentiel dans lequel une différence de potentiel obtenue en soustrayant un potentiel de l'électrode commune (17) d'un potentiel de la couche de métal (19) est opposée en polarité à une différence

de potentiel obtenue en soustrayant le potentiel de l'électrode commune (17) d'un potentiel de la section d'électrode de pixels (12) ; un deuxième état de potentiel dans lequel le potentiel de la couche de métal (19) est égal au potentiel de l'électrode commune (17) ; et un troisième état de potentiel dans lequel la différence de potentiel obtenue en soustrayant le potentiel de l'électrode commune (17) du potentiel de la couche de métal (19) est égale en polarité à la différence de potentiel obtenue en soustrayant le potentiel de l'électrode commune (17) du potentiel de la section d'électrode de pixels (12), et dans lequel une valeur absolue d'une différence entre le potentiel de la section d'électrode de pixels (12) et le potentiel de l'électrode commune (17) est supérieure ou égale à une valeur absolue d'une différence entre le potentiel de la couche de métal (19) et le potentiel de l'électrode commune (17).

FIG. 1

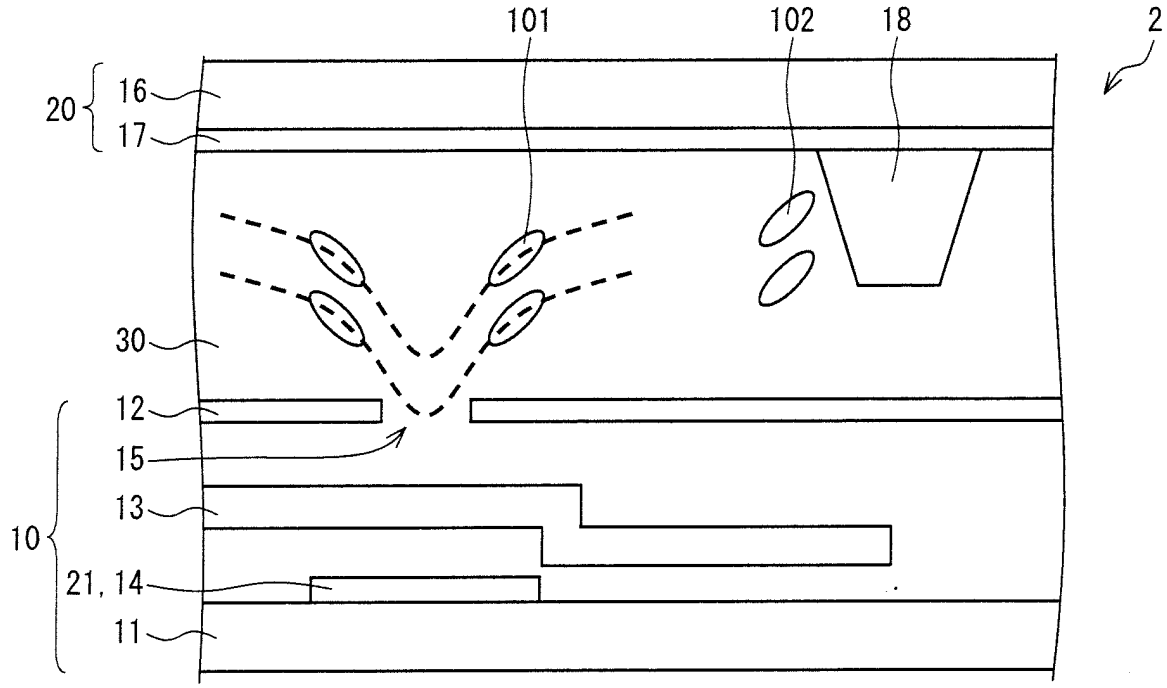


FIG. 2

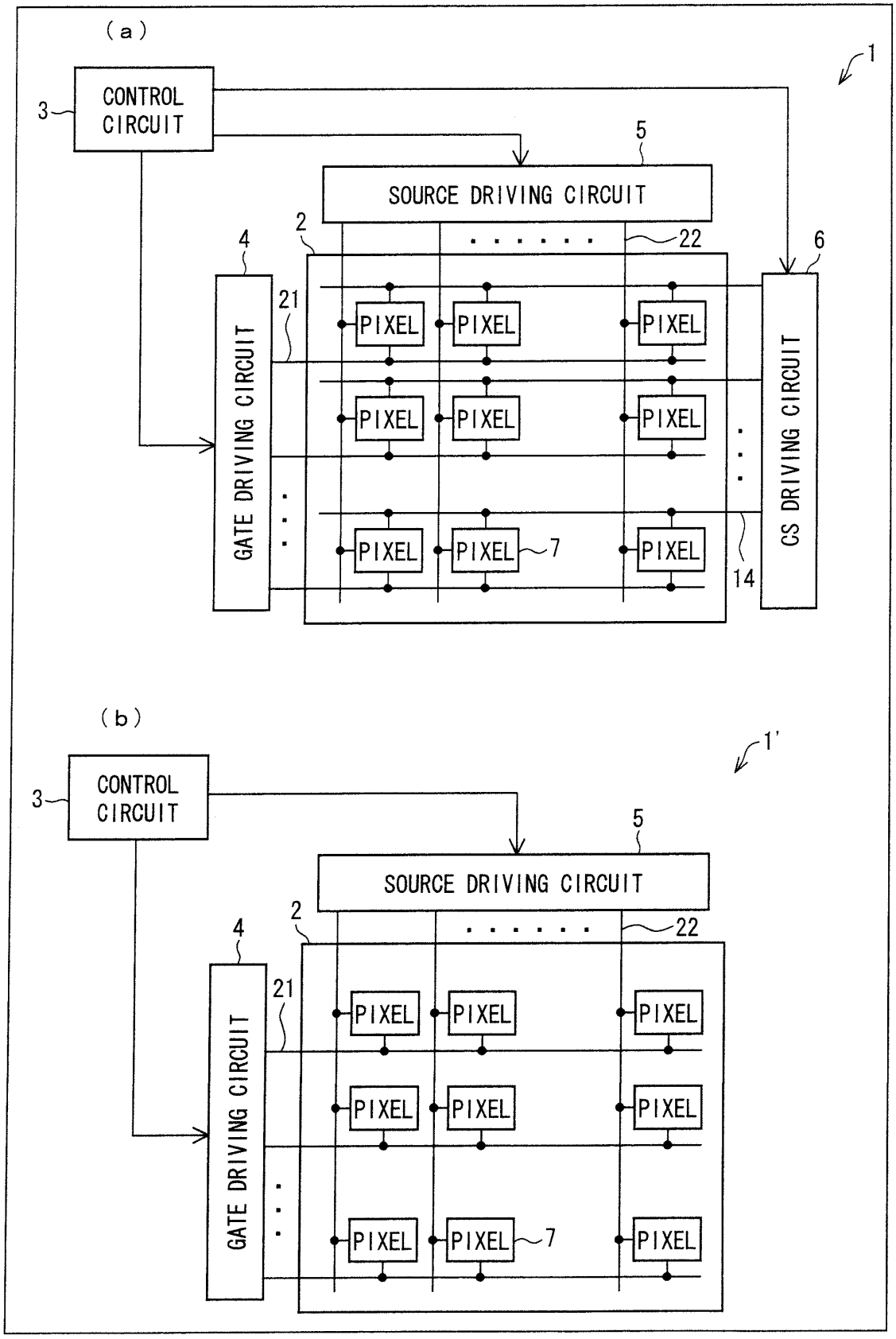

(a)
1
3
CONTROL CIRCUIT
5
SOURCE DRIVING CIRCUIT
2
4
22
6
21
PIXEL
GATE DRIVING CIRCUIT
CS DRIVING CIRCUIT
7
14
(b)
1'
3
CONTROL CIRCUIT
5
SOURCE DRIVING CIRCUIT
2
4
22
21
PIXEL
GATE DRIVING CIRCUIT
7

FIG. 3

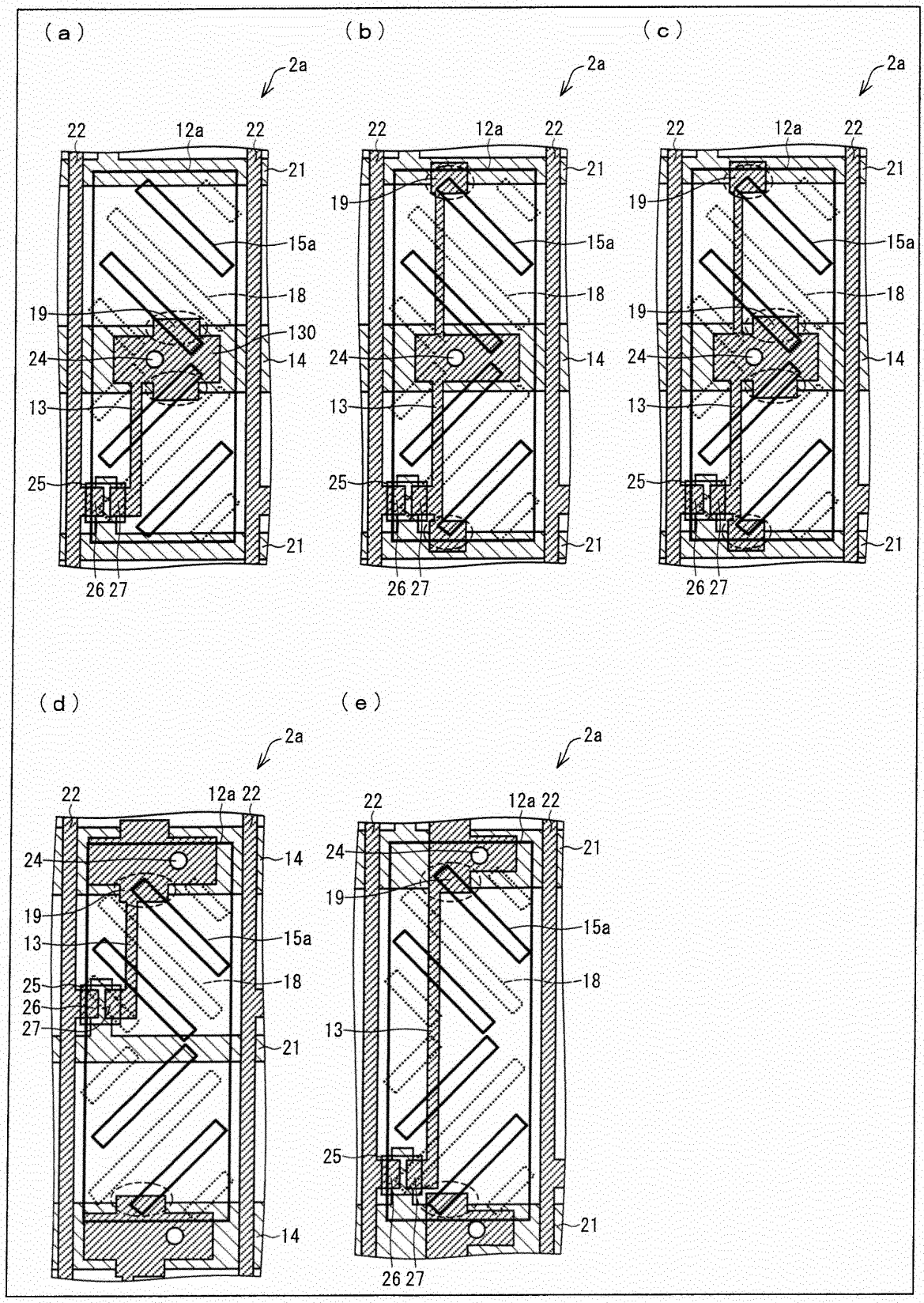


FIG. 4a

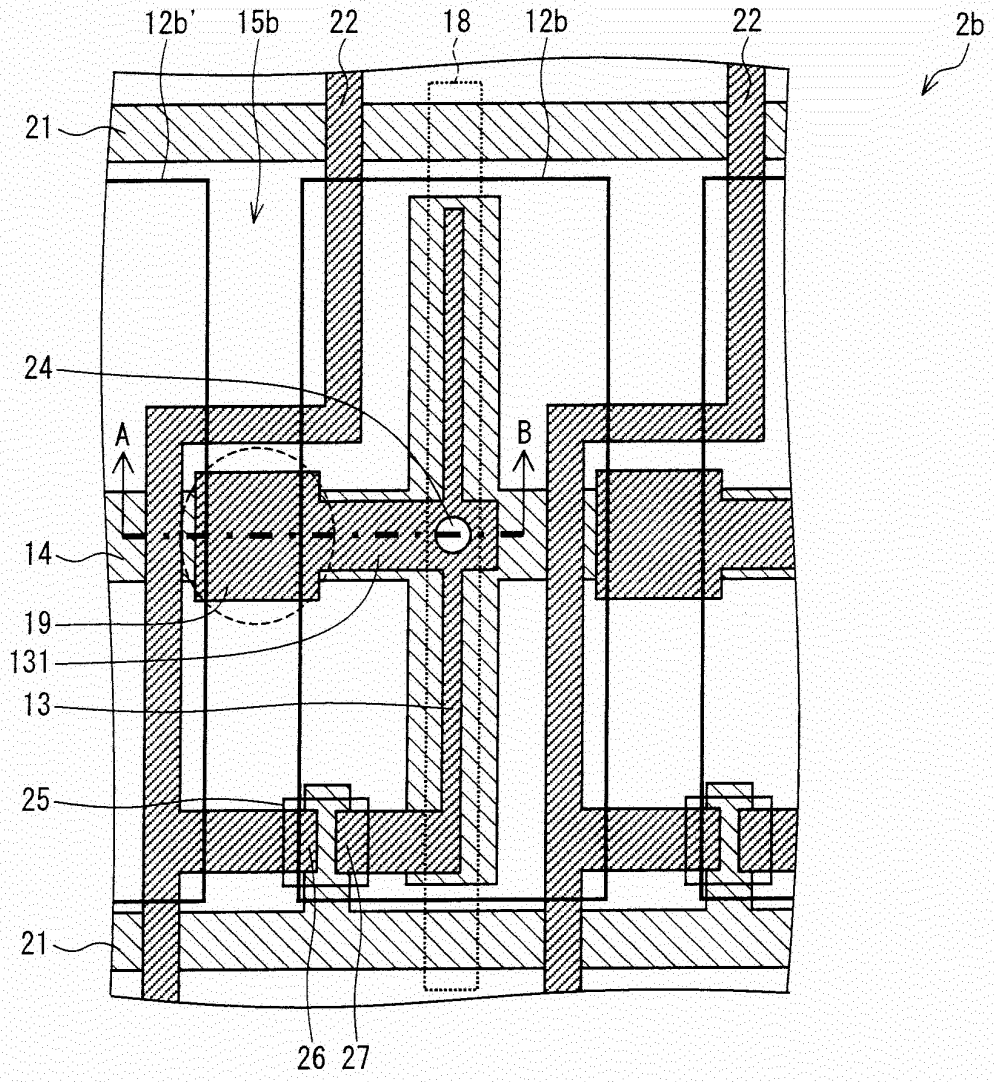

12b'
15b
22
18
12b
22
2b
21
24
A
B
14
19
131
13
25
21
26
27

FIG. 4b

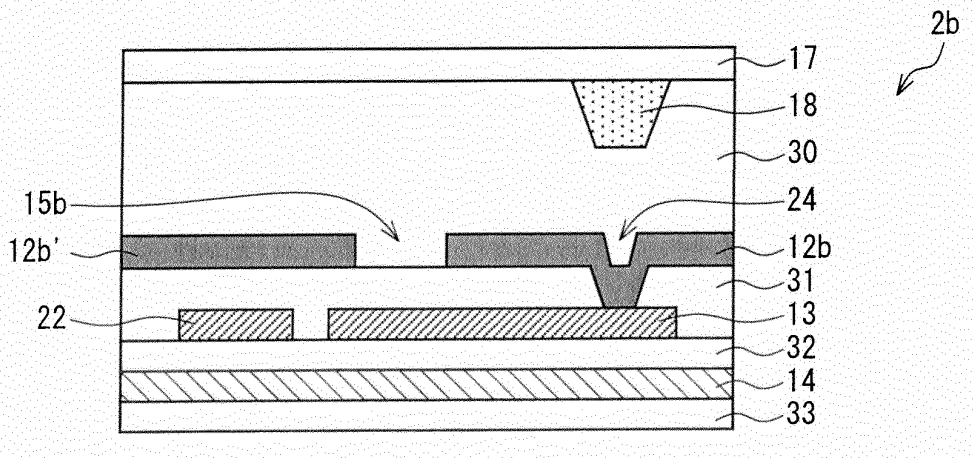

2b
17
18
30
15b
24
12b'
12b
31
22
13
32
14
33

FIG. 5

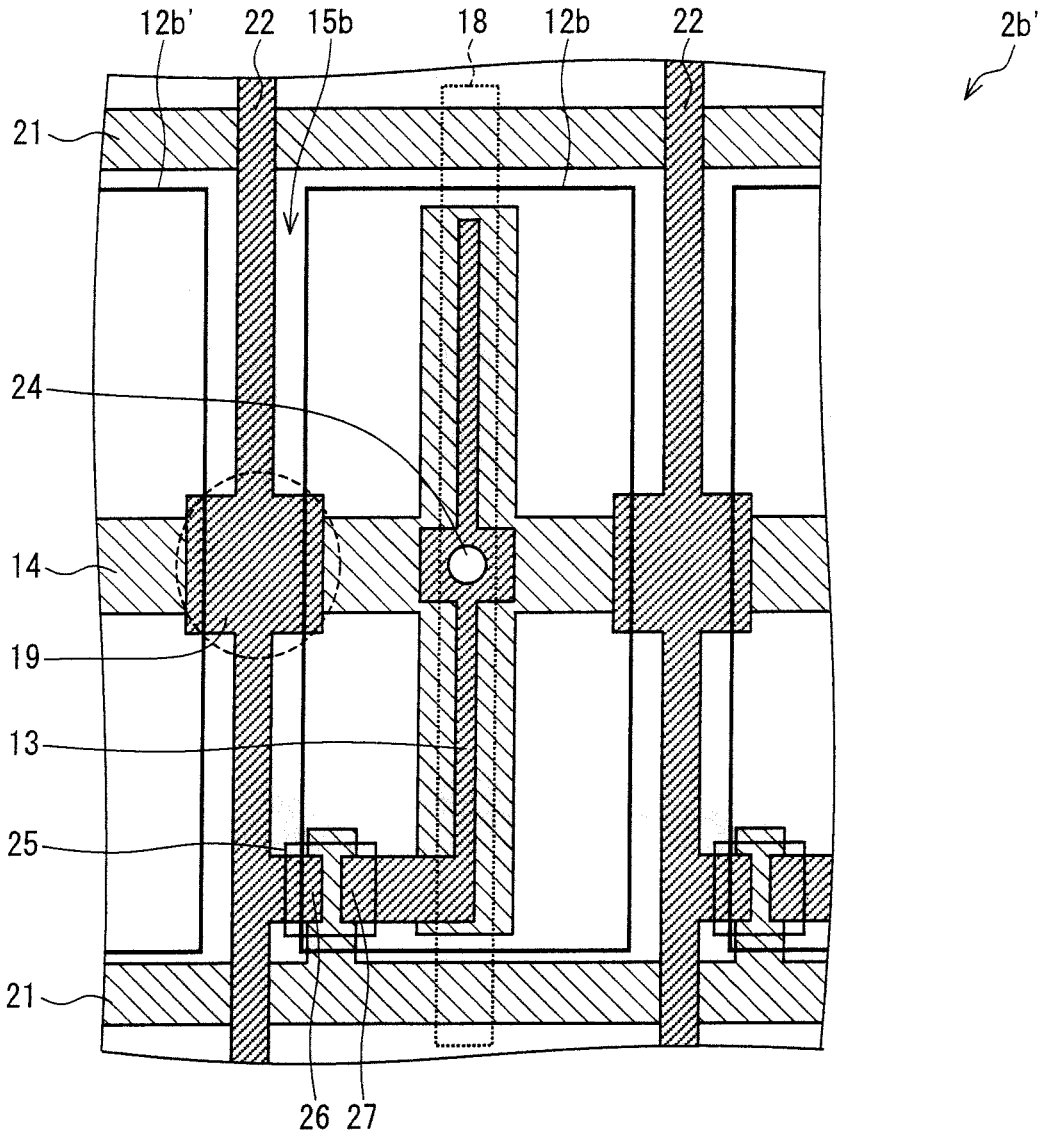


FIG. 6

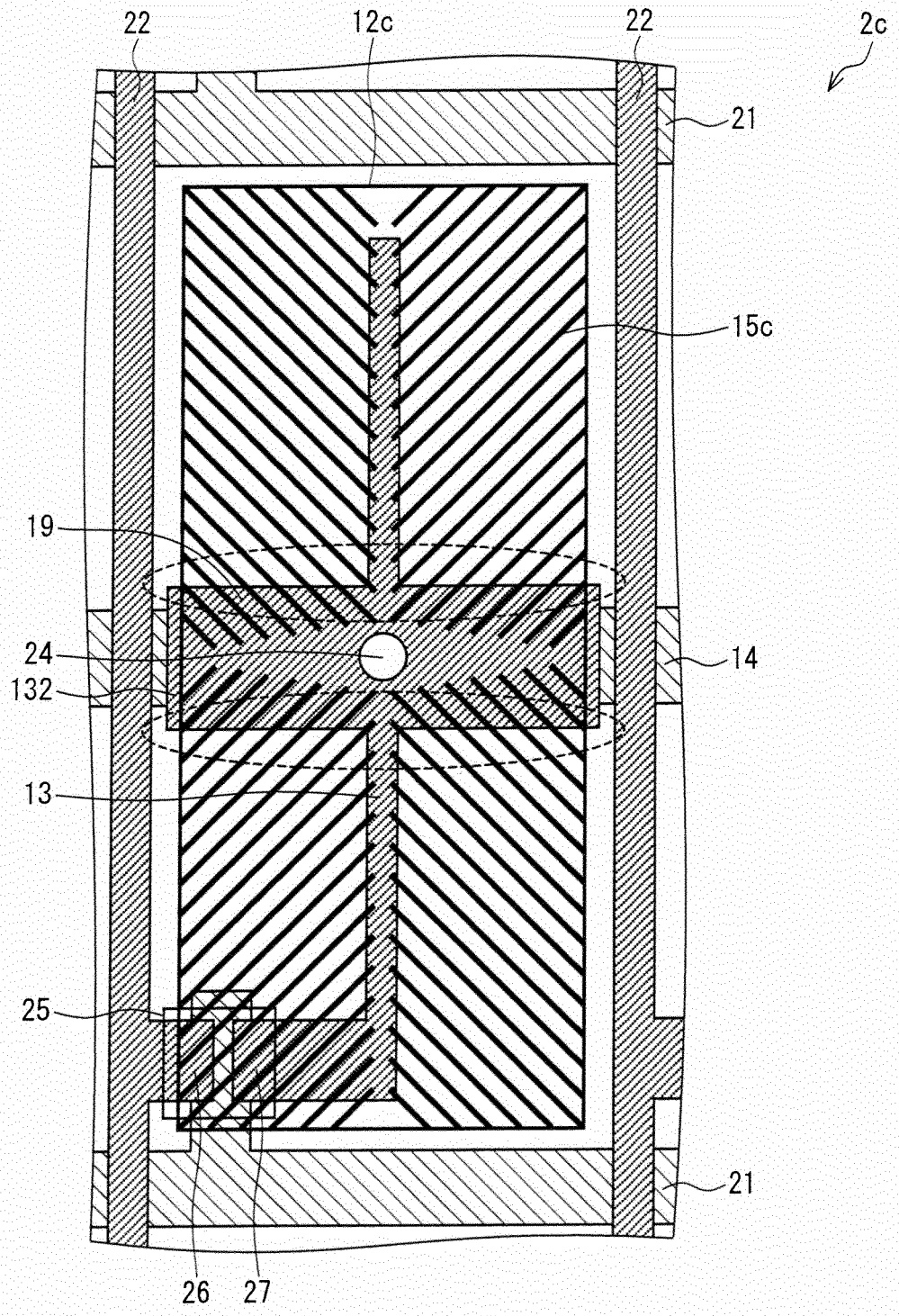


FIG. 7

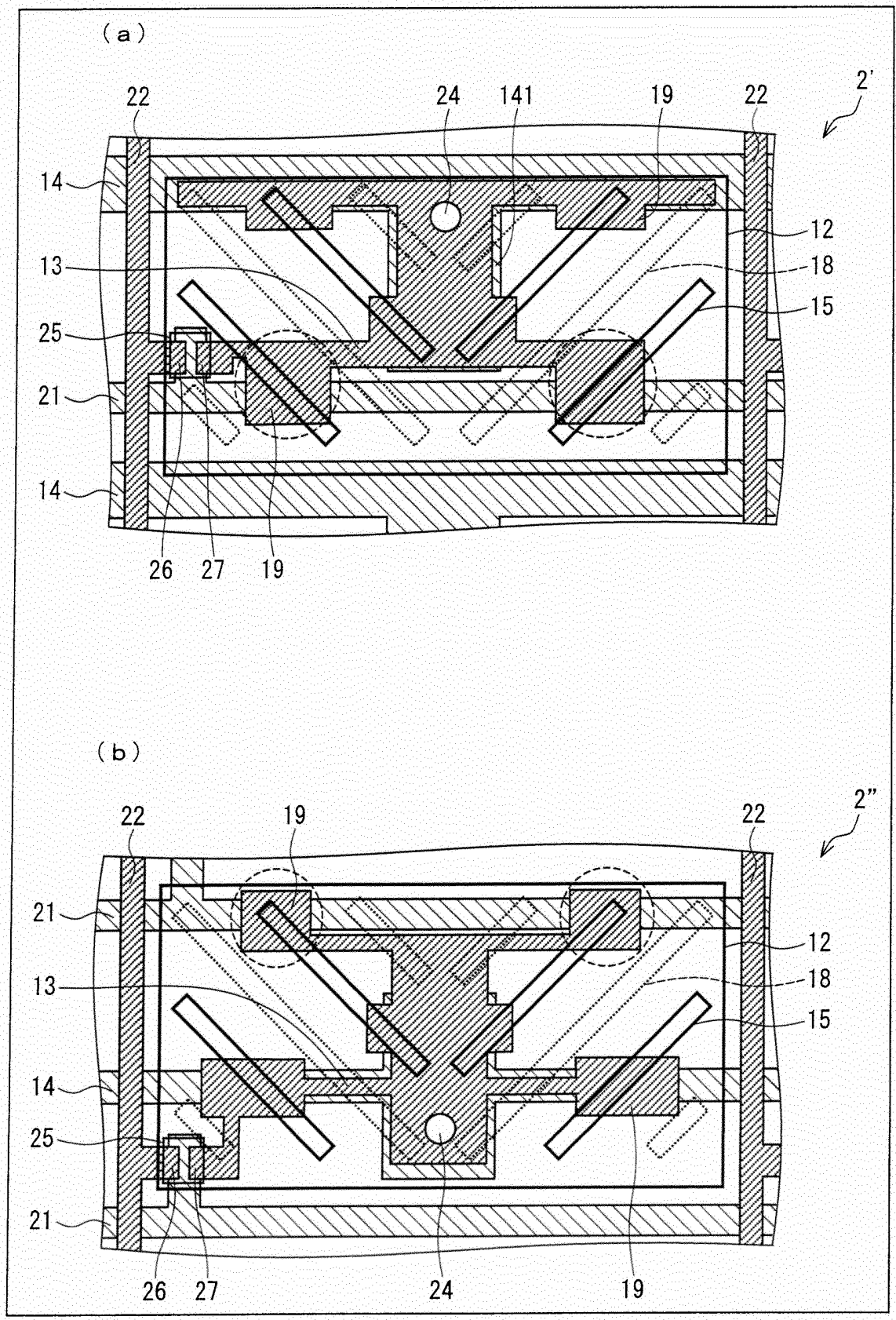

(a)
22
24
141
19
22
2'
14
12
13
18
15
25
21
14
26
27
19
(b)
22
19
22
2"
21
12
13
18
15
14
25
21
26
27
24
19

FIG. 8

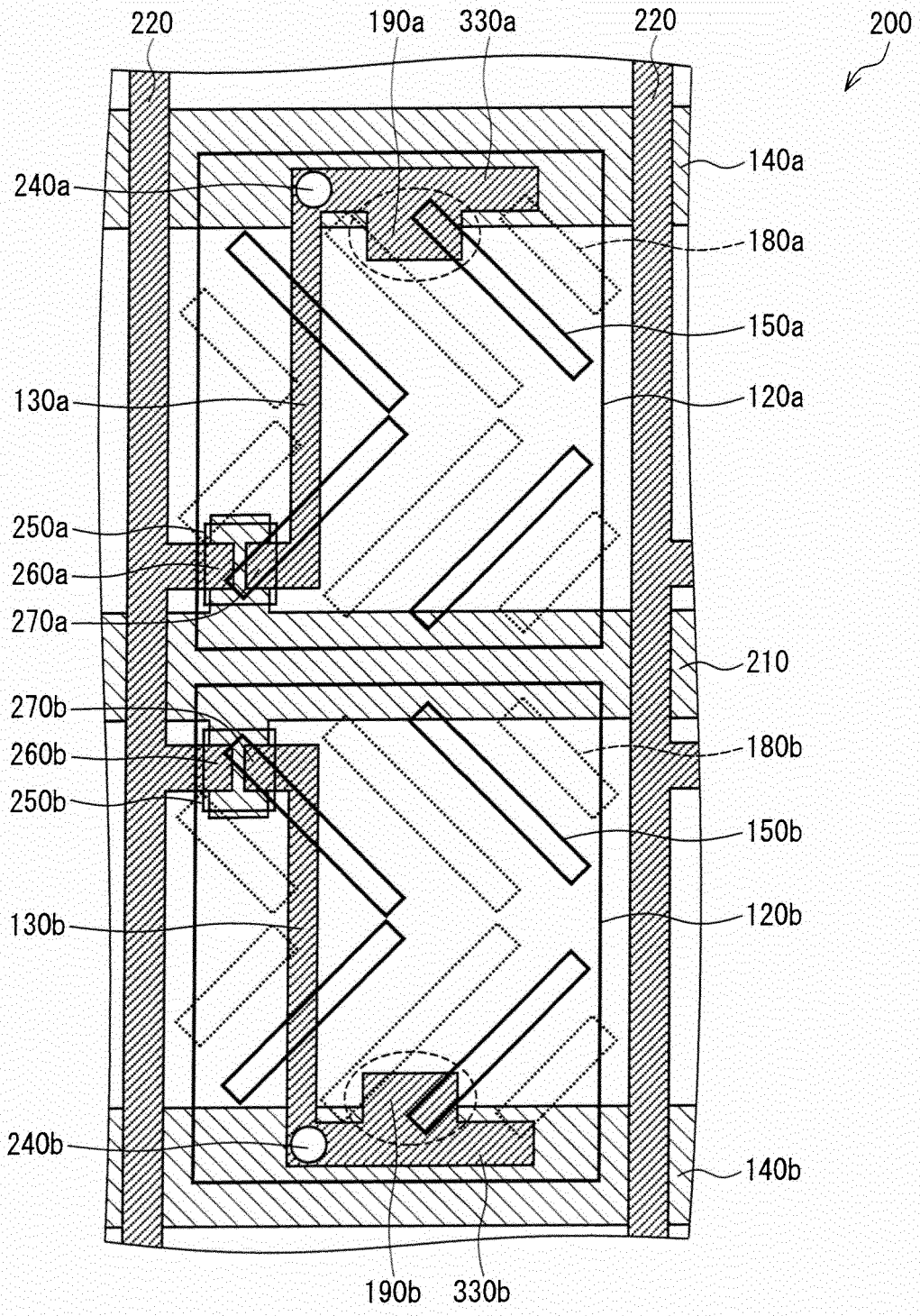

220
190a
330a
220
200
140a
240a
180a
150a
130a
120a
250a
260a
270a
210
270b
260b
180b
250b
150b
130b
120b
240b
140b
190b
330b

FIG. 9

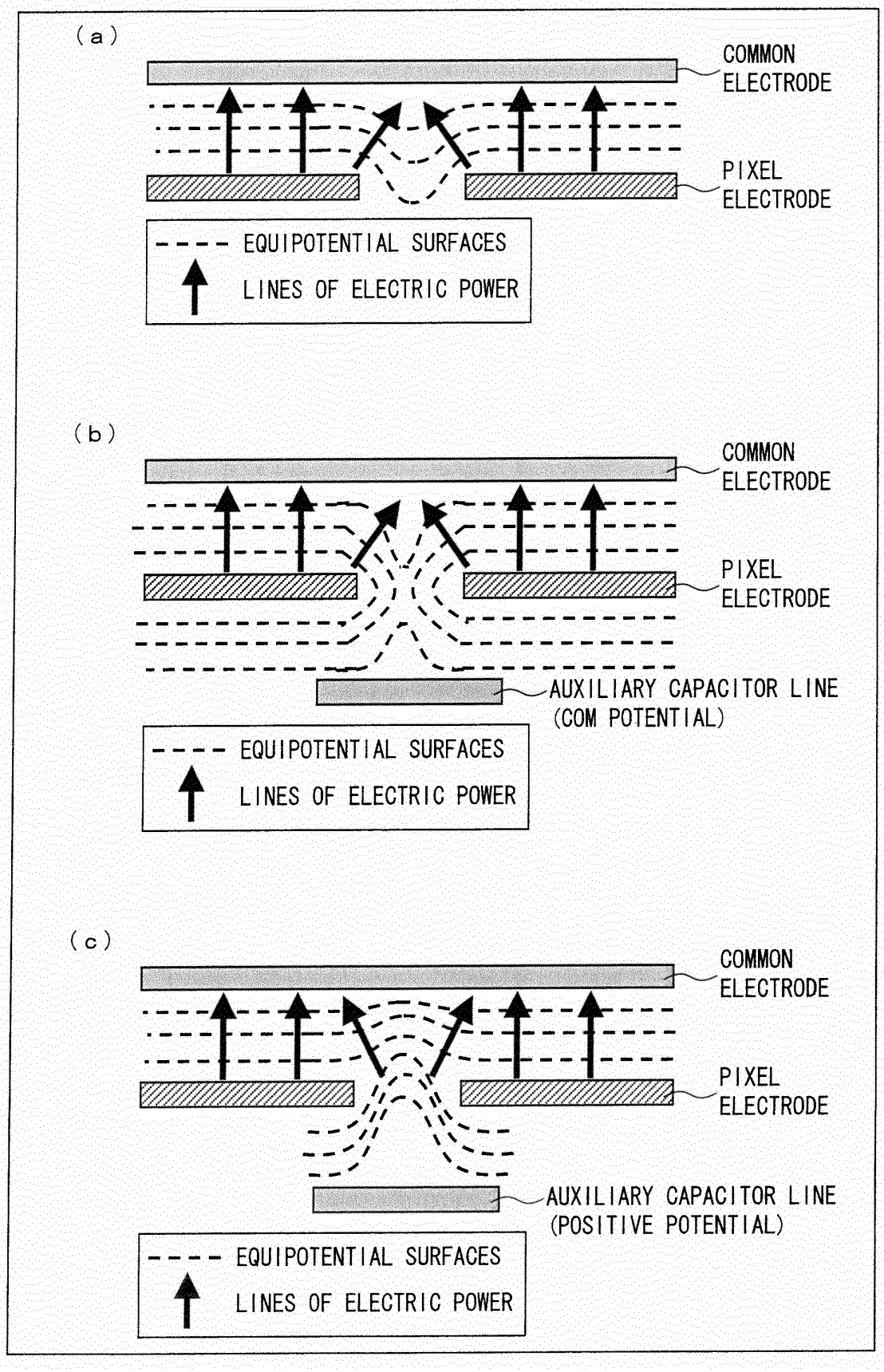

(a)
COMMON ELECTRODE
PIXEL ELECTRODE
EQUIPOTENTIAL SURFACES
LINES OF ELECTRIC POWER
(b)
COMMON ELECTRODE
PIXEL ELECTRODE
AUXILIARY CAPACITOR LINE (COM POTENTIAL)
EQUIPOTENTIAL SURFACES
LINES OF ELECTRIC POWER
(c)
COMMON ELECTRODE
PIXEL ELECTRODE
AUXILIARY CAPACITOR LINE (POSITIVE POTENTIAL)
EQUIPOTENTIAL SURFACES
LINES OF ELECTRIC POWER

FIG. 10

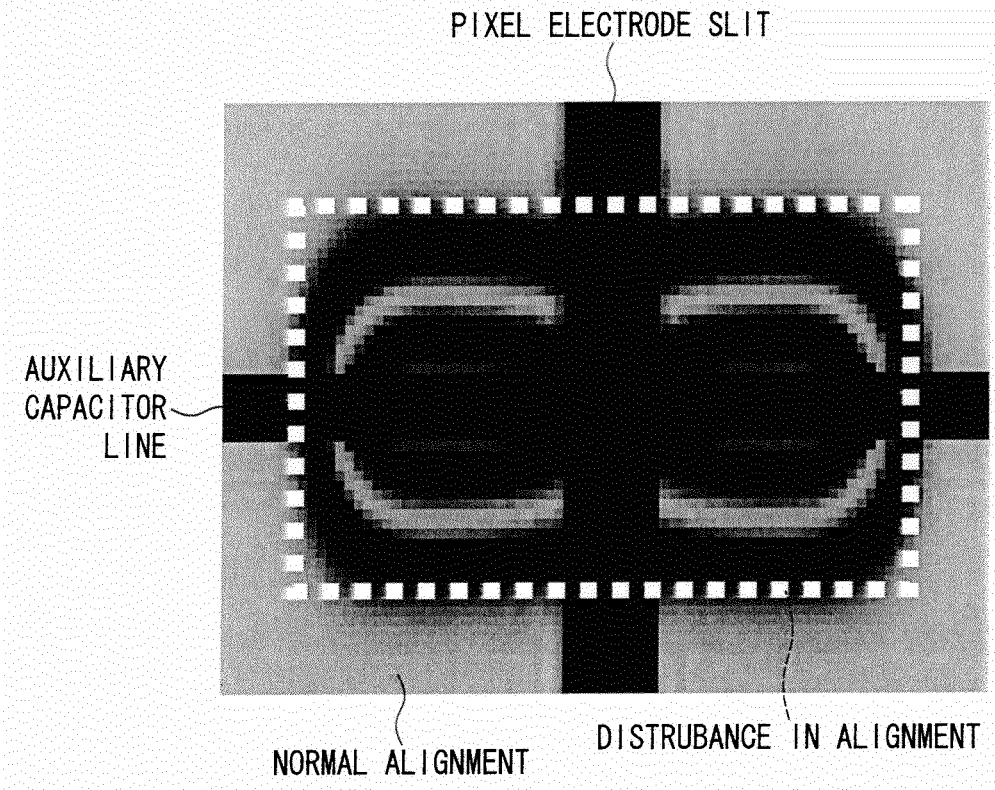

PIXEL ELECTRODE SLIT
AUXILIARY CAPACITOR LINE
NORMAL ALIGNMENT
DISTRUBANCE IN ALIGNMENT

FIG. 11

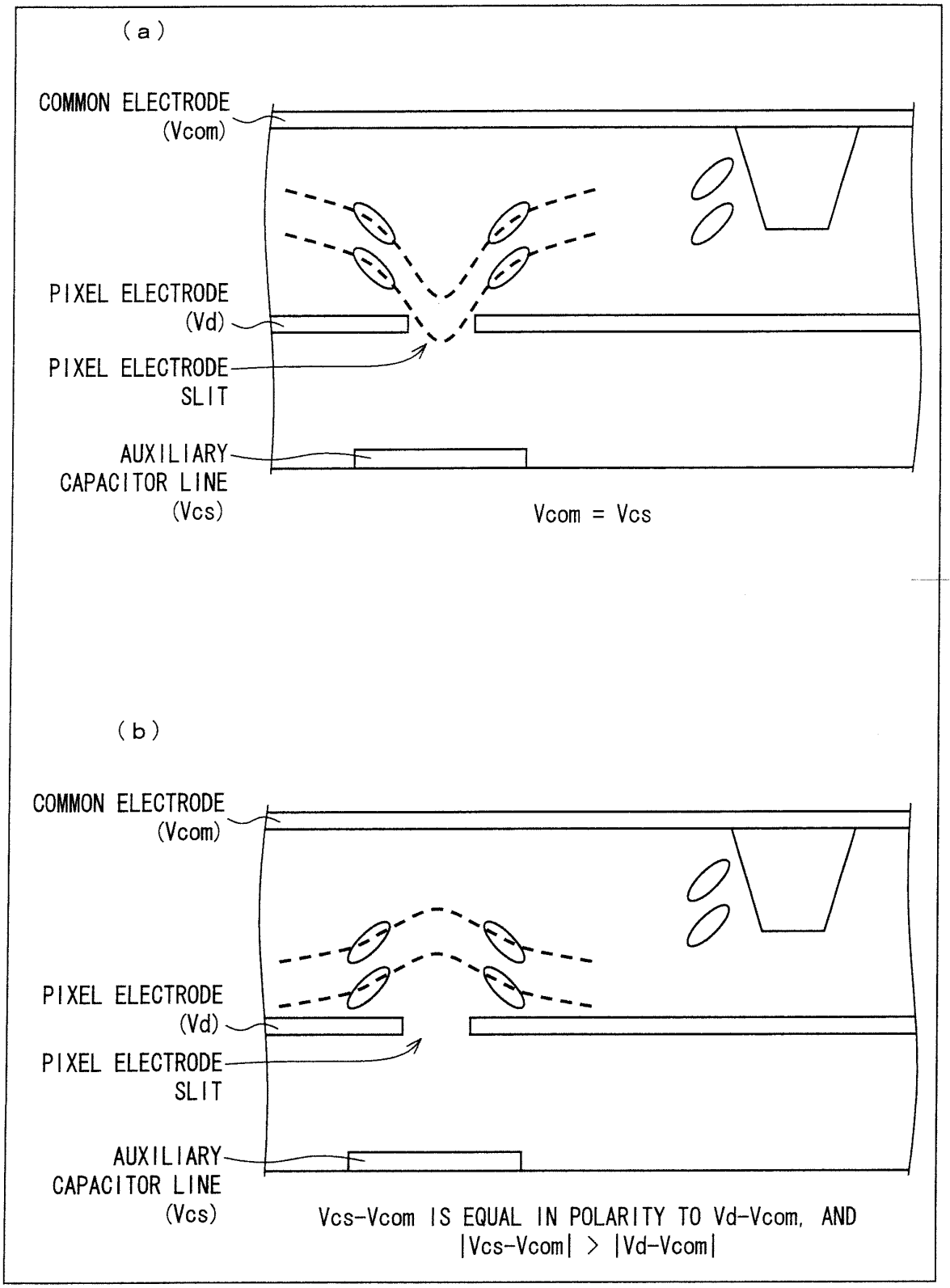
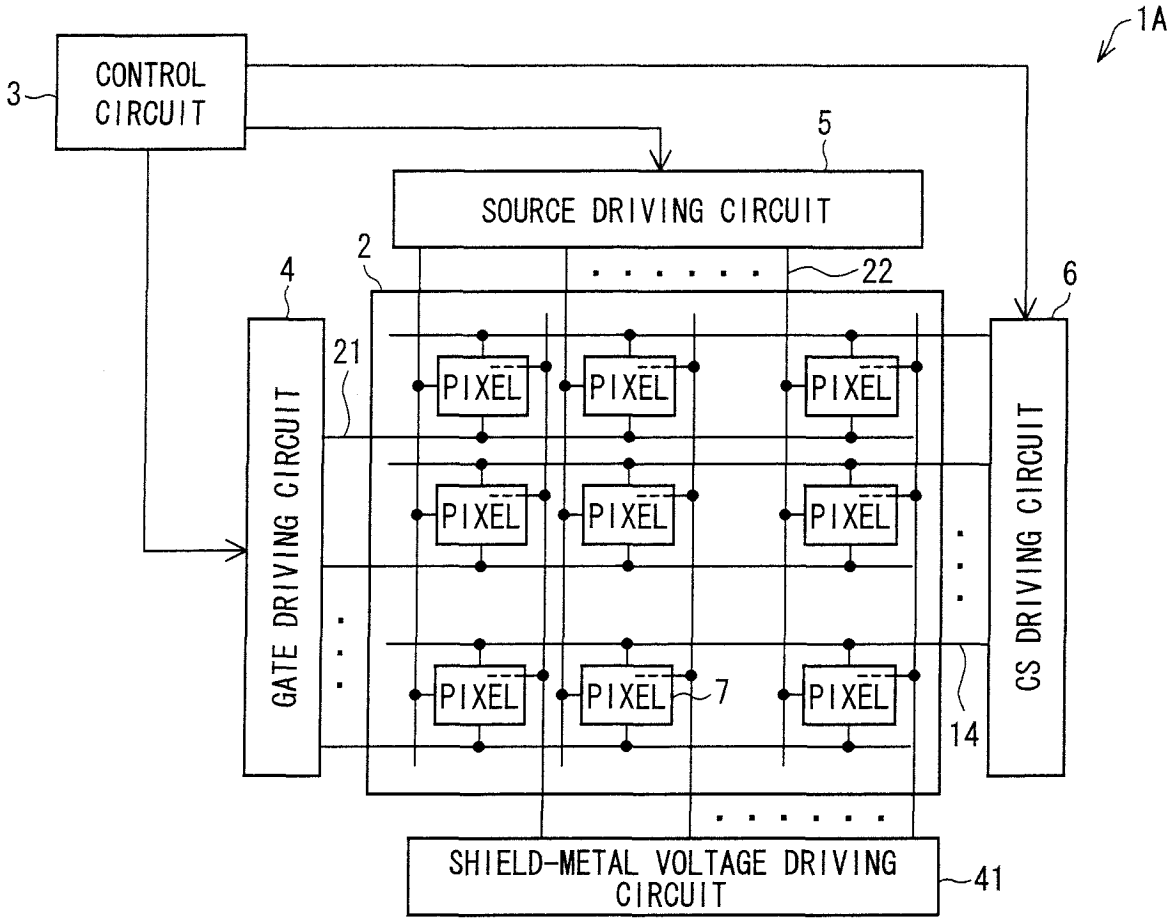

(a)
COMMON ELECTRODE
(Vcom)
PIXEL ELECTRODE
(Vd)
PIXEL ELECTRODE
SLIT
AUXILIARY
CAPACITOR LINE
(Vcs)
Vcom = Vcs
(b)
COMMON ELECTRODE
(Vcom)
PIXEL ELECTRODE
(Vd)
PIXEL ELECTRODE
SLIT
AUXILIARY
CAPACITOR LINE
(Vcs)
Vcs-Vcom IS EQUAL IN POLARITY TO Vd-Vcom, AND
|Vcs-Vcom| > |Vd-Vcom|

FIG. 12


1A
3
CONTROL CIRCUIT
5
SOURCE DRIVING CIRCUIT
2
4
22
6
21
PIXEL
GATE DRIVING CIRCUIT
CS DRIVING CIRCUIT
7
14
SHIELD-METAL VOLTAGE DRIVING CIRCUIT
41

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- US 2007211187 A1 **[0008]**
- JP 2003149647 A **[0009]**
- JP 2003177408 A **[0009]**

专利名称(译)	有源矩阵基板，液晶显示面板，液晶显示装置，有源矩阵基板的制造方法，液晶显示面板的制造方法以及液晶显示面板的驱动方法		
公开(公告)号	EP2390718B1	公开(公告)日	2014-11-05
申请号	EP2009827416	申请日	2009-08-07
[标]申请(专利权)人(译)	夏普株式会社		
申请(专利权)人(译)	夏普株式会社		
当前申请(专利权)人(译)	夏普株式会社		
[标]发明人	HORIUCHI SATOSHI YAMADA TAKAHARU HISADA YUHKO ITOH RYOHKI		
发明人	HORIUCHI, SATOSHI YAMADA, TAKAHARU HISADA, YUHKO ITOH, RYOHKI		
IPC分类号	G02F1/1343 G02F1/1368 G02F1/1337		
CPC分类号	G02F1/1337 G02F1/133707 G02F1/133788 G02F1/13624 G02F2001/133715 G02F2001/133769 G02F2001/134345 G02F2001/134372 G02F2001/13629 G02F2201/128 G02F2201/40 G02F2203/62 G09G3/3637 G09G3/3655 G09G2330/10		
优先权	2008295725 2008-11-19 JP		
其他公开文献	EP2390718A1 EP2390718A4		
外部链接	Espacenet		

摘要(译)

通过抑制包括基板的液晶显示板中的对准干扰来实现高质量显示，该基板被构造成使得像素电极中的狭缝与扫描信号线或辅助电容线相交。有源矩阵基板（10）包括：具有狭缝的像素电极（12）;和辅助电容线（14）。在狭缝（15）和辅助电容器线（14）或扫描信号线（21）之间的交叉区域中，至少一条漏极线（13）或数据信号线（22）设置在一层之间。像素电极（12）和辅助电容线（14）或扫描信号线（21）的层以覆盖辅助电容线（12）或扫描信号线（21）的方式。
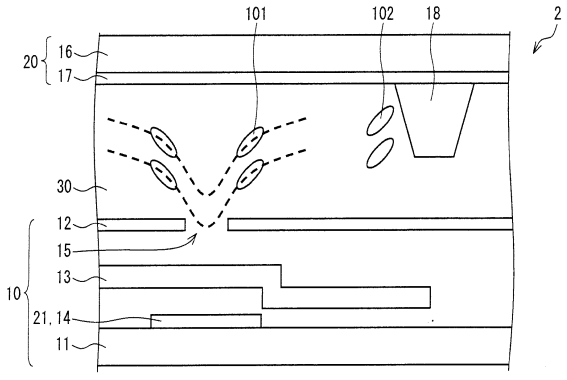
FIG. 1