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(54) **Liquid crystal display and methods of driving the same**

(57) A liquid crystal display (LCD) and methods of driving same. In one embodiment, the LCD includes a plurality of gate lines, $\{G_n\}$, spatially arranged along a row direction; a plurality of data lines, $\{D_m\}$, spatially arranged along a column direction perpendicular to the row direction, and a plurality of pixels, $\{P_{n,m}\}$, spatially arranged in the form of a matrix, where $m = 1, 2, \dots, M$, $n = 1, 2, \dots, N$, and M and N are positive integers. Each pixel $P_{n,m}$ is defined between two neighboring gate lines G_n and G_{n+1} and two neighboring data lines D_m and D_{m+1} , and comprises a first sub-pixel electrode, a second sub-pixel electrode, a first transistor (111) having a gate electrically coupled to the gate line G_{n+1} , a source and a drain electrically coupled to the first sub-pixel electrode, a second transistor (112) having a gate electrically coupled to the gate line G_n , a source electrically coupled to the source of the first transistor and a drain electrically coupled to the second sub-pixel electrode, and a third transistor (113) having a gate electrically coupled to the gate line G_{n+2} , a source electrically coupled to one of the two neighboring data lines D_m and D_{m+1} and a drain electrically coupled to the sources of the first and second transistors

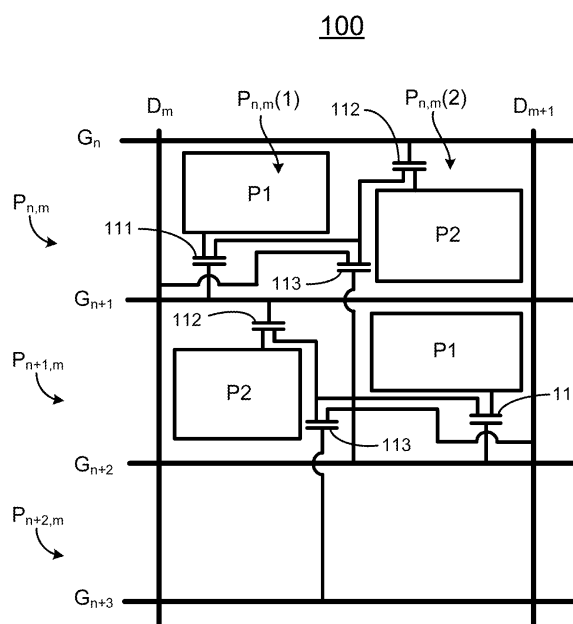


Fig. 1

Description**FIELD OF THE INVENTION**

5 **[0001]** The present invention relates generally to a liquid crystal display (LCD), and more particularly, to an LCD that utilizes an HSD3 driving scheme to reduce power consumption and improve performance and methods of driving same.

BACKGROUND OF THE INVENTION

10 **[0002]** A liquid crystal display (LCD) device includes an LCD panel formed with liquid crystal cells and pixel elements with each associating with a corresponding liquid crystal cell and having a liquid crystal (LC) capacitor and a storage capacitor, a thin film transistor (TFT) electrically coupled with the liquid crystal capacitor and the storage capacitor. These pixel elements are substantially arranged in the form of a matrix having a number of pixel rows and a number of pixel columns. Typically, gate signals are sequentially applied to the number of pixel rows for sequentially turning on the pixel elements row-by-row. When a gate signal is applied to a pixel row to turn on corresponding TFTs of the pixel elements of a pixel row, source signals (i.e., image signals) for the pixel row are simultaneously applied to the number of pixel columns so as to charge the corresponding liquid crystal capacitor and storage capacitor of the pixel row for aligning orientations of the corresponding liquid crystal cells associated with the pixel row to control light transmittance there-through. By repeating the procedure for all pixel rows, all pixel elements are supplied with corresponding source signals of the image signal, thereby displaying the image signal thereon.

15 **[0003]** It is known if a substantially high voltage potential is applied in the liquid crystal layer for a long period of time, the optical transmission characteristics of the liquid crystal molecules may change. This change may be permanent, causing an irreversible degradation in the display quality of the LCD. In order to prevent the LC molecules from being deteriorated, an LCD device is usually driven by using techniques that alternate the polarity of the voltages applied across a LC cell. These techniques may include inversion schemes such as frame inversion, row inversion, column inversion, and dot inversion. Typically, notwithstanding the inversion schemes, a higher image quality requires higher power consumption because of frequent polarity conversions. Such LCD devices, in particular thin film transistor (TFT) LCD devices, may consume significant amounts of power.

20 **[0004]** Approaches for reducing the power consumption of an LCD exist, such as a half source driving configuration of pixels, as shown in Fig. 6, which is referred to HSD2 in the disclosure. Fig. 6(a) shows waveforms of gate signals g_1 and g_2 sequentially applied to gate lines G1 and G2 of the LCD, respectively. Figs. 6(b)-(f) show corresponding charging and holding processes of two sub-pixels P1 and P2 defined by two gate lines G1 and G2 and two data lines D1 and D2. For such an approach, during the timing sequences (states), t_0 , t_1 , ..., and t_4 , the sub-pixel P2 has twice feed-throughs but the sub-pixel P1 has only one feed-through. Accordingly, the potential voltages charged in the sub-pixels P1 and P2 are different. The non-uniformity of the potential voltages in the sub-pixels P1 and P2 cause the mura effect, a defect in intensity in displayed images.

25 **[0005]** Therefore, a heretofore unaddressed need exists in the art to address the aforementioned deficiencies and inadequacies.

SUMMARY OF THE INVENTION

30 **[0006]** The present invention, in one aspect, relates to an LCD. In one embodiment, the LCD includes a plurality of gate lines, $\{G_n\}$, $n = 1, 2, \dots, N$, N being an integer greater than zero, spatially arranged along a row direction, a plurality of data lines, $\{D_m\}$, $m = 1, 2, \dots, M$, M being an integer greater than zero, spatially arranged crossing the plurality of gate lines $\{G_n\}$ along a column direction perpendicular to the row direction, and a plurality of pixels, $\{P_{n,m}\}$, spatially arranged in the form of a matrix.

35 **[0007]** Each pixel $P_{n,m}$ is defined between two neighboring gate lines G_n and G_{n+1} and two neighboring data lines D_m and D_{m+1} , and comprises a first sub-pixel electrode, a second sub-pixel electrode, a first transistor having a gate electrically coupled to the gate line G_{n+1} , a source and a drain electrically coupled to the first sub-pixel electrode, a second transistor having a gate electrically coupled to the gate line G_n , a source electrically coupled to the source of the first transistor and a drain electrically coupled to the second sub-pixel electrode, and a third transistor having a gate electrically coupled to the gate line G_{n+2} , a source electrically coupled to one of the two neighboring data lines D_m and D_{m+1} and a drain electrically coupled to the sources of the first and second transistors. In one embodiment, the source of the third transistor of the pixel $P_{n,m}$ is electrically coupled to the data line D_m . In another embodiment, the source of the third transistor of the pixel $P_{n,m}$ is electrically coupled to the data line D_m when n is an odd positive integer, or electrically coupled to the data line D_{m+1} when n is an even positive integer.

40 **[0008]** Additionally, the LCD also includes a gate driver for generating a plurality of gate signals respectively applied to the plurality of gate lines $\{G_n\}$, wherein the plurality of gate signals is configured to turn on the transistors connected

to the plurality of gate lines $\{G_n\}$ in a predefined sequence, and a data driver for generating a plurality of data signals respectively applied to the plurality of data lines $\{D_m\}$, wherein the plurality of data signals is configured such that any two neighboring data signals have inverted polarities. Each of the plurality of gate signals is configured to have a waveform. The waveform has a first voltage potential V_1 in a first duration, Γ_1 , a second voltage potential V_2 in a second duration, Γ_2 , a third voltage potential V_3 in a third duration, Γ_3 , a fourth voltage potential V_4 in a fourth duration, Γ_4 , and a fifth voltage potential V_5 in a fifth duration, Γ_5 , where the $(j+1)$ -th duration Γ_{j+1} is immediately after the j -th duration Γ_j , $j = 1, 2, 3$ and 4 , $V_1 = V_3 = V_5 > V_2 = V_4$, $\Gamma_2 = \Gamma_1/2$, $\Gamma_3 = (\Gamma_1 - t)/2$, $\Gamma_4 = t$, $\Gamma_5 = \Gamma_3$, and $\Gamma_1 \gg t$. In one embodiment, the waveform of each of the gate signals is sequentially shifted from one another by the duration of Γ_1 .

[0009] In one embodiment, the LCD further includes at least one common electrode formed in relation to the first and second sub-pixel electrodes of each pixel $P_{n,m}$.

[0010] In one embodiment, each pixel $P_{n,m}$ further comprises a liquid crystal (LC) capacitor, a second LC capacitor, a first storage capacitor and a second storage capacitor. The first LC capacitor and the first storage capacitor are electrically coupled between the first sub-pixel electrode and the at least one common electrode in parallel. The second LC capacitor and the second storage capacitor are electrically coupled between the second sub-pixel electrode and the at least one common electrode in parallel.

[0011] In one embodiment, the first sub-pixel electrode, the first transistor, the first LC capacitor, and the first storage capacitor of each pixel $P_{n,m}$ define a first sub-pixel, $P_{n,m}(1)$, of the pixel $P_{n,m}$. The second sub-pixel electrode, the second transistor, the second LC capacitor, and the second storage capacitor of each pixel $P_{n,m}$ define a second sub-pixel, $P_{n,m}(2)$, of the pixel $P_{n,m}$.

[0012] In another aspect, the present invention relates to a method of driving an LCD. In one embodiment, the method includes the step of providing an LCD comprising a plurality of gate lines, $\{G_n\}$, $n = 1, 2, \dots, N$, N being an integer greater than zero, spatially arranged along a row direction, a plurality of data lines, $\{D_m\}$, $m = 1, 2, \dots, M$, M being an integer greater than zero, spatially arranged crossing the plurality of gate lines $\{G_n\}$ along a column direction perpendicular to the row direction, and a plurality of pixels, $\{P_{n,m}\}$, spatially arranged in the form of a matrix.

[0013] Each pixel $P_{n,m}$ is defined between two neighboring gate lines G_n and G_{n+1} and two neighboring data lines D_m and D_{m+1} , and comprises a first sub-pixel electrode, a second sub-pixel electrode, a first transistor having a gate electrically coupled to the gate line G_{n+1} , a source and a drain electrically coupled to the first sub-pixel electrode, a second transistor having a gate electrically coupled to the gate line G_n , a source electrically coupled to the source of the first transistor and a drain electrically coupled to the second sub-pixel electrode, and a third transistor having a gate electrically coupled to the gate line G_{n+2} , a source electrically coupled to one of the two neighboring data lines D_m and D_{m+1} and a drain electrically coupled to the sources of the first and second transistors. In one embodiment, the source of the third transistor of the pixel $P_{n,m}$ is electrically coupled to the data line D_m . In another embodiment, the source of the third transistor of the pixel $P_{n,m}$ is electrically coupled to the data line D_m when n is an odd positive integer, or electrically coupled to the data line D_{m+1} when n is an even positive integer.

[0014] The method also includes the step of applying a plurality of gate signals to the plurality of gate lines $\{G_n\}$ and a plurality of data signals to the plurality of data lines $\{D_m\}$, respectively, wherein the plurality of gate signals is configured to turn on the transistors connected to the plurality of gate lines $\{G_n\}$ in a predefined sequence, and the plurality of data signals is configured such that any two neighboring data signals have inverted polarities.

[0015] In one embodiment, each of the plurality of gate signals is configured to have a waveform. The waveform has a first voltage potential V_1 in a first duration, Γ_1 , a second voltage potential V_2 in a second duration, Γ_2 , a third voltage potential V_3 in a third duration, Γ_3 , a fourth voltage potential V_4 in a fourth duration, Γ_4 , and a fifth voltage potential V_5 in a fifth duration, Γ_5 , where the $(j+1)$ -th duration Γ_{j+1} is immediately after the j -th duration Γ_j , $j = 1, 2, 3$ and 4 , $V_1 = V_3 = V_5 > V_2 = V_4$, $\Gamma_2 = \Gamma_1/2$, $\Gamma_3 = (\Gamma_1 - t)/2$, $\Gamma_4 = t$, $\Gamma_5 = \Gamma_3$, and $\Gamma_1 \gg t$. In one embodiment, the waveform of each of the gate signals is sequentially shifted from one another by the duration of Γ_1 .

[0016] In yet another aspect, the present invention relates to an LCD. In one embodiment, the LCD panel comprises a plurality of pixels, $\{P_{n,m}\}$, spatially arranged in the form of a matrix, $n = 1, 2, \dots, N$, and $m = 1, 2, \dots, M$, and N, M being an integer greater than zero. Each pixel $P_{n,m}$ includes a first sub-pixel electrode, a second sub-pixel electrode, a first switching element electrically coupled to the first sub-pixel electrode, a second switching element electrically coupled to the second sub-pixel electrode, and a third switching element electrically coupled to the first and second switching elements.

[0017] The LCD further comprises a plurality of gate lines, $\{G_n\}$, spatially arranged along a row direction. Each pair of two neighboring gate lines G_n and G_{n+1} defines a pixel row $P_{n,\{m\}}$ of the pixel matrix $\{P_{n,m}\}$ therebetween and is electrically coupled to the first and second switching elements of each pixel in the pixel row $P_{n,\{m\}}$, respectively.

[0018] The LCD also comprises a plurality of data lines, $\{D_m\}$, spatially arranged crossing the plurality of gate lines $\{G_n\}$ along a column direction perpendicular to the row direction. Each pair of two neighboring data lines D_m and D_{m+1} defines a pixel column, $P_{\{n\},m}$, of the pixel matrix $\{P_{n,m}\}$ therebetween, and is electrically coupled to the third switching element of each pixel $P_{n,m}$ in the pixel column, $P_{\{n\},m}$.

[0019] Moreover, the LCD includes a gate driver for generating a plurality of gate signals respectively applied to the

plurality of gate lines $\{G_n\}$, wherein the plurality of gate signals is configured to turn on the switching elements connected to the plurality of gate lines $\{G_n\}$ in a predefined sequence, and a data driver for generating a plurality of data signals respectively applied to the plurality of data lines $\{D_m\}$, wherein the plurality of data signals is configured such that any two neighboring data signals have inverted polarities.

[0020] In one embodiment, the first sub-pixel electrode and the first switching element of each pixel $P_{n,m}$ define a first sub-pixel, $P_{n,m}(1)$, of the pixel $P_{n,m}$. The second sub-pixel electrode and the second switching element of each pixel $P_{n,m}$ define a second sub-pixel, $P_{n,m}(2)$, of the pixel $P_{n,m}$.

[0021] In one embodiment, each of the first, second and third switching elements of the pixel $P_{n,m}$ of the pixel matrix $\{P_{n,m}\}$ is a field-effect thin film transistor having a gate, a source and a drain. The gate, the source and the drain of the first switching element of the pixel $P_{n,m}$ are electrically coupled to the gate line G_{n+1} , the source of the second switching element of the pixel $P_{n,m}$, and the first sub-pixel electrode of the pixel $P_{n,m}$, respectively. The gate, the source and the drain of the second switching element of the pixel $P_{n,m}$ are electrically coupled to the gate line G_n , the source of the first switching element of the pixel $P_{n,m}$, and the second sub-pixel electrode of the pixel $P_{n,m}$, respectively. In one embodiment, the gate, the source and the drain of the third switching element of the pixel $P_{n,m}$ are electrically coupled to the gate line G_{n+2} , the data line D_m , and the sources of the first and second switching elements of the pixel $P_{n,m}$, respectively. In another embodiment, the gate and the drain of the third switching element of the pixel $P_{n,m}$ are electrically coupled to the gate line G_{n+2} and the sources of the first and second switching elements of the pixel $P_{n,m}$, respectively, while the source of the third transistor of the pixel $P_{n,m}$ is electrically coupled to the data line D_m when n is an odd positive integer, or electrically coupled to the data line D_{m+1} when n is an even positive integer.

[0022] In a further aspect, the present invention relates to a method of driving an LCD. In one embodiment, the method includes the step of providing an LCD comprising (a) a plurality of pixels, $\{P_{n,m}\}$, spatially arranged in the form of a matrix, $n = 1, 2, \dots, N$, and $m = 1, 2, \dots, M$, and N, M being an integer greater than zero, each pixel $P_{n,m}$ comprising a first sub-pixel electrode, a second sub-pixel electrode, a first switching element electrically coupled to the first sub-pixel electrode, a second switching element electrically coupled to the second sub-pixel electrode, and a third switching element electrically coupled to the first and second switching elements, (b) a plurality of gate lines, $\{G_n\}$, spatially arranged along a row direction, wherein each pair of two neighboring gate lines G_n and G_{n+1} defines a pixel row $P_{n,\{m\}}$ of the pixel matrix $\{P_{n,m}\}$ therebetween and is electrically coupled to the first and second switching elements of each pixel in the pixel row $P_{n,\{m\}}$, respectively, and (c) a plurality of data lines, $\{D_m\}$, spatially arranged crossing the plurality of gate lines $\{G_n\}$ along a column direction perpendicular to the row direction. Each pair of two neighboring data lines D_m and D_{m+1} defines a pixel column, $P_{\{n\},m}$, of the pixel matrix $\{P_{n,m}\}$ therebetween, and is electrically coupled to the third switching element of each pixel $P_{n,m}$ in the pixel column, $P_{\{n\},m}$.

[0023] In one embodiment, each of the first, second and third switching elements of the pixel $P_{n,m}$ of the pixel matrix $\{P_{n,m}\}$ is a field-effect thin film transistor having a gate, a source and a drain. The gate, the source and the drain of the first switching element of the pixel $P_{n,m}$ are electrically coupled to the gate line G_{n+1} , the source of the second switching element of the pixel $P_{n,m}$, and the first sub-pixel electrode of the pixel $P_{n,m}$, respectively. The gate, the source and the drain of the second switching element of the pixel $P_{n,m}$ are electrically coupled to the gate line G_n , the source of the first switching element of the pixel $P_{n,m}$, and the second sub-pixel electrode of the pixel $P_{n,m}$, respectively. The gate, the source and the drain of the third switching element of the pixel $P_{n,m}$ are electrically coupled to the gate line G_{n+2} , the data line D_m , and the sources of the first and second switching elements of the pixel $P_{n,m}$, respectively. The gate, the source and the drain of the third switching element of the pixel $P_{n+1,m}$ are electrically coupled to the gate line G_{n+3} , the data line D_{m+1} , and the sources of the first and second switching elements of the pixel $P_{n+1,m}$, respectively.

[0024] The method also includes the step of applying a plurality of gate signals to the plurality of gate lines $\{G_n\}$ and a plurality of data signals to the plurality of data lines $\{D_m\}$, respectively, wherein the plurality of gate signals is configured to turn on the switching elements connected to the plurality of gate lines $\{G_n\}$ in a predefined sequence, and the plurality of data signals is configured such that any two neighboring data signals have inverted polarities.

[0025] In one embodiment, each of the plurality of gate signals is configured to have a waveform. The waveform has a first voltage potential V_1 in a first duration, Γ_1 , a second voltage potential V_2 in a second duration, Γ_2 , a third voltage potential V_3 in a third duration, Γ_3 , a fourth voltage potential V_4 in a fourth duration, Γ_4 , and a fifth voltage potential V_5 in a fifth duration, Γ_5 , where the $(j+1)$ -th duration Γ_{j+1} is immediately after the j -th duration Γ_j , $j = 1, 2, 3$ and 4 , $V_1 = V_3 = V_5 > V_2 = V_4$, $\Gamma_2 = \Gamma_1/2$, $\Gamma_3 = (\Gamma_1 - t)/2$, $\Gamma_4 = t$, $\Gamma_5 = \Gamma_3$, and $\Gamma_1 \gg t$. The waveform of each of the gate signals is sequentially shifted from one another by the duration of Γ_1 .

[0026] These and other aspects of the present invention will become apparent from the following description of the preferred embodiment taken in conjunction with the following drawings, although variations and modifications therein may be affected without departing from the spirit and scope of the novel concepts of the disclosure.

BRIEF DESCRIPTION OF THE DRAWINGS

[0027] The accompanying drawings illustrate one or more embodiments of the invention and, together with the written

description, serve to explain the principles of the invention. Wherever possible, the same reference numbers are used throughout the drawings to refer to the same or like elements of an embodiment, wherein:

Fig. 1 shows schematically a partial layout view of an LCD according to one embodiment of the present invention;
 Fig. 2 shows time charts of driving signals applied to the LCD shown in Fig. 1;
 Fig. 3 shows schematically pixel charging and holding processes (a)-(d) of the LCD shown in Fig. 1;
 Fig. 4 shows simulation results of the pixel voltage potentials of the LCD for the gate signals shown in Fig. 1;
 Fig. 5 shows schematically an LCD according to another embodiment of the present invention, (a) an equivalent circuit diagram, and (b) time charts of driving signals;
 Fig. 6 shows schematically pixel charging and holding processes (a) and (b) of the LCD shown in Fig. 5; and
 Fig. 7 shows time charts of driving signals (a) and pixel charging and holding processes (b)-(f) of a conventional LCD.

DETAILED DESCRIPTION OF THE INVENTION

[0028] The present disclosure is more particularly described in the following examples that are intended as illustrative only since numerous modifications and variations therein will be apparent to those skilled in the art. Various embodiments of the disclosure are now described in detail. Referring to the drawings, like numbers indicate like components throughout the views. As used in the description herein and throughout the claims that follow, the meaning of "a", "an", and "the" includes plural reference unless the context clearly dictates otherwise. Also, as used in the description herein and throughout the claims that follow, the meaning of "in" includes "in" and "on" unless the context clearly dictates otherwise.

[0029] The terms used in this specification generally have their ordinary meanings in the art, within the context of the disclosure, and in the specific context where each term is used. Certain terms that are used to describe the disclosure are discussed below, or elsewhere in the specification, to provide additional guidance to the practitioner regarding the description of the disclosure. The use of examples anywhere in this specification, including examples of any terms discussed herein, is illustrative only, and in no way limits the scope and meaning of the disclosure or of any exemplified term. Likewise, the disclosure is not limited to various embodiments given in this specification.

[0030] As used herein, "around", "about" or "approximately" shall generally mean within 20 percent, preferably within 10 percent, and more preferably within 5 percent of a given value or range. Numerical quantities given herein are approximate, meaning that the term "around", "about" or "approximately" can be inferred if not expressly stated.

[0031] As used herein, the terms "comprising," "including," "having," "containing," "involving," and the like are to be understood to be open-ended, i.e., to mean including but not limited to.

[0032] The term "HSD2", as used herein, refers to a pixel arrangement and driving scheme of an LCD in which each pixel defined two neighboring gate lines is configured to have first and second switches electrically coupled to the two neighboring gate lines, respectively. The term "HSD3", as used herein, refers to a pixel arrangement and driving scheme of an LCD in which each pixel defined two neighboring gate lines is configured to have first, second and third switches. The first and second switches are electrically coupled to the two neighboring gate lines, respectively, while the third switch is electrically coupled to the first and second switches and a third gate line that is immediately next to the two neighboring gate lines.

[0033] The description will be made as to the embodiments of the present invention in conjunction with the accompanying drawings in Figs. 1-6. In accordance with the purposes of this invention, as embodied and broadly described herein, this invention, in one aspect, relates to an LCD that utilizes an HSD3 driving scheme to reduce power consumption and improve performance and methods of driving same.

[0034] Referring to Fig. 1, an LCD panel 100 according to one embodiment of the present invention is partially and schematically shown. The LCD panel 100 includes a plurality of gate lines, $G_1, G_2, \dots, G_n, G_{n+1}, G_{n+2}, G_{n+3}, \dots, G_N$, that are spatially arranged along a row (horizontal) direction, and a plurality of data lines, $D_1, D_2, \dots, D_m, D_{m+1}, D_{m+2}, D_{m+3}, \dots, D_M$, that are spatially arranged crossing the plurality of gate lines $G_1, G_2, \dots, G_n, G_{n+1}, G_{n+2}, G_{n+3}, \dots, G_N$ along a column (vertical) direction that is perpendicular to the row direction. N and M are integers greater than one. The LCD panel 100 further has a plurality of pixels, $\{P_{n,m}\}$, that is spatially arranged in the form of a matrix. Each pixel $P_{n,m}$ is defined between two neighboring gate lines G_n and G_{n+1} and two neighboring data lines D_m and D_{m+1} . For the purpose of illustration of embodiments of the present invention, Fig. 1 schematically shows only four gate lines G_n, G_{n+1}, G_{n+2} and G_{n+3} , two data lines D_m and D_{m+1} , and three corresponding pixels of the LCD panel 100.

[0035] The pixel $P_{n,m}$ located, for example, between two neighboring gate lines G_n and G_{n+1} and two neighboring data lines D_m and D_{m+1} crossing the two neighboring gate lines G_n and G_{n+1} , has a first sub-pixel electrode P1, a second sub-pixel electrode P2, a first transistor 111, a second transistor 112 and a third transistor 113.

[0036] The first transistor 111 has a gate electrically coupled to the gate line G_{n+1} , a source and a drain electrically coupled to the first sub-pixel electrode P1. The second transistor 112 has a gate electrically coupled to the gate line G_n , a source electrically coupled to the source of the first transistor 111 and a drain electrically coupled to the second sub-pixel electrode P2. The third transistor 113 has a gate electrically coupled to the gate line G_{n+2} , a source electrically

coupled to one of the two neighboring data lines D_m and D_{m+1} and a drain electrically coupled to the sources of the first and second transistors 111 and 112. In the exemplary embodiment shown in Fig. 1, the source of the third transistor 113 of the pixel $P_{n,m}$ is electrically coupled to the data line D_m when n is an odd positive integer, or electrically coupled to the data line D_{m+1} when n is an even positive integer. In another embodiment as shown in Fig. 5 below, the source of the third transistor 113 of the pixel $P_{n,m}$ is electrically coupled to the data line D_m .

[0037] Additionally, the LCD 100 also includes at least one common electrode (not shown) formed in relation to the first and second sub-pixel electrodes P1 and P2 of each pixel $P_{n,m}$. As shown in Fig. 5 below, each pixel $P_{n,m}$ may further include a first LC capacitor, C_{L1} , a second LC capacitor, C_{L2} , a first storage capacitor, C_{S1} , and a second storage capacitor, C_{S2} . The first LC capacitor C_{L1} and the first storage capacitor C_{S1} are electrically coupled between the first sub-pixel electrode P1 and the at least one common electrode in parallel. The second LC capacitor C_{L2} and the second storage capacitor C_{S2} are electrically coupled between the second sub-pixel electrode P2 and the at least one common electrode in parallel.

[0038] Alternatively, each pixel $P_{n,m}$ is configured to have two or more sub-pixels. The first sub-pixel electrode P1, the first transistor 111, the first LC capacitor C_{L1} and the first storage capacitor C_{S1} of each pixel $P_{n,m}$ define a first sub-pixel, $P_{n,m}(1)$, of the pixel $P_{n,m}$, while the second sub-pixel electrode P2, the second transistor 112, the second LC capacitor C_{L2} and the second storage capacitor C_{S2} of each pixel $P_{n,m}$ define a second sub-pixel, $P_{n,m}(2)$, of the pixel $P_{n,m}$. The first, second and third transistors 111, 112 and 113 in one embodiment are field-effect TFTs and adapted for activating the first sub-pixel $P_{n,m}(1)$ and the second sub-pixel $P_{n,m}(2)$, respectively. Other types of transistors may also be utilized to practice the present invention.

[0039] In one embodiment, the sub-pixel electrodes P1/P2 of the first sub-pixel $P_{n,m}(1)$ and the second sub-pixel $P_{n,m}(2)$ of each pixel $P_{n,m}$ are deposited on a first substrate (not shown), while the common electrode is deposited on a second substrate (not shown) that is spatially apart from the first substrate. The LC molecules are filled into cells between the first and second substrates. Each cell is associated with a pixel $P_{n,m}$ of the LCD 100. Voltages (potentials) applied to the sub-pixel electrodes P1 and P2 control orientation alignments of the LC molecules in the LC cells associated with the corresponding sub-pixels.

[0040] The LCD 100 further has a gate driver and a data driver (not shown). The gate driver is adapted for generating a plurality of gate signals, $\{g_n\}$, respectively applied to the plurality of gate lines $\{G_n\}$. The plurality of gate signals $\{g_n\}$ is configured to turn on the first, second and third transistors 111, 112 and 113 connected to the plurality of gate lines $\{G_n\}$ in a predefined sequence. The data driver is adapted for generating a plurality of data signals, $\{d_m\}$, respectively applied to the plurality of data lines $\{D_m\}$.

[0041] Referring to Fig. 2, waveform/time charts of the gate signals g_1 , g_2 , g_3 and g_4 applied to the LCD shown in Fig. 1 and charging in the corresponding sub-pixel electrodes P1 and P2 of the LCD are shown according to one embodiment of the present invention. Each of the gate signals g_1 , g_2 , g_3 and g_4 is configured to have a waveform. The waveform has a first voltage potential V_1 in a first duration, Γ_1 , a second voltage potential V_2 in a second duration, Γ_2 , a third voltage potential V_3 in a third duration, Γ_3 , a fourth voltage potential V_4 in a fourth duration, Γ_4 , and a fifth voltage potential V_5 in a fifth duration, Γ_5 , where the $(j+1)$ -th duration Γ_{j+1} is immediately after the j -th duration Γ_j , $j = 1, 2, 3$ and 4 , $V_1 = V_3 = V_5 > V_2 = V_4$, $\Gamma_2 = \Gamma_1/2$, $\Gamma_3 = (\Gamma_1 - t)/2$, $\Gamma_4 = t$, $\Gamma_5 = \Gamma_3$, and $\Gamma_1 \gg t \geq \Gamma_1/40$. In this embodiment, V_1 (V_3 , V_5) and V_2 (V_4) are corresponding to a high voltage potential and a low voltage potential, respectively, for effectively turning on and off the corresponding transistors of a corresponding pixel row. The waveform of each of the gate signals g_1 , g_2 , g_3 and g_4 is sequentially shifted from one another so as to activate the three pixel rows in a predetermined order (sequence). In this exemplary embodiment, the gate signal g_2 is shifted by the duration of Γ_1 from the gate signal g_1 ; the gate signal g_3 is shifted by the duration of Γ_1 from the gate signal g_2 ; and the gate signal g_4 is shifted by the duration of Γ_1 from the gate signal g_3 , respectively. Usually, the waveform of each gate signal is characterized with a plurality of pulses, for example, pulses 201, 202 and 203. Each pulse has a pulse width and height. Specifically, the pulse width and height of the pulse 201 define the first duration Γ_1 and the first voltage potential V_1 , respectively; the pulse width and height of the pulse 202 define the third duration Γ_3 and the third voltage potential V_3 , respectively; and the pulse width and height of the pulse 203 define the fifth duration Γ_5 and the fifth voltage potential V_5 , respectively. The separation between the pulses 201 and 202 defines the second duration Γ_2 , while the separation between the pulses 202 and 203 defines the fourth duration Γ_4 . In one embodiment, $\Gamma_1 \gg \Gamma_4 (=t) \geq \Gamma_1/40$.

[0042] As shown in Fig. 3, when such gate signals g_1 , g_2 , g_3 and g_4 are applied to the gate lines G_1 , G_2 , G_3 , and G_4 , respectively, of the LCD shown in Fig. 1, the second feed-through effect on the first sub-pixel or the second sub-pixel will be avoided in operation.

[0043] For example, in the time period of T0, the gates G_1 and G_2 are turned on, while the gates G_3 and G_4 are turned off. Accordingly, the third transistors 113 of both the pixels $P_{1,1}$ and $P_{2,1}$ are turned off. Thus, no data signals are applied to the first and second sub-pixels of the pixels $P_{1,1}$ and $P_{2,1}$ through the data line D_1 or D_2 . This is corresponding to State T0, as shown in Fig. 3(a).

[0044] In the time period of T1, the gates G_1 and G_3 are turned on, while the gates G_2 and G_4 are turned off. Accordingly, the second transistor 112 and the third transistor 113 of the pixel $P_{1,1}$ are turned on, whereby the data signal is applied

to the second sub-pixel of the pixel $P_{1,1}$ through the data line D_1 , and the second sub-pixel electrode P2 of the pixel $P_{1,1}$ is charged. This is corresponding to State T1, as shown in Fig. 3(b).

[0045] In the time period of T2, the gates G_2 and G_3 are turned on, while the gates G_1 and G_4 are turned off. Accordingly, the first transistor 111 and the third transistor 113 of the pixel $P_{1,1}$ are turned on, whereby the data signal is applied to the first sub-pixel of the pixel $P_{1,1}$ through the data line D_1 , and the first sub-pixel electrode P1 of the pixel $P_{1,1}$ is charged and the second sub-pixel electrode P2 of the pixel $P_{1,1}$ is held. This is corresponding to State T2, as shown in Fig. 3(c).

[0046] In the time period of T3, the gates G_2 and G_4 are turned on, while the gates G_1 and G_3 are turned off. Accordingly, the second transistor 112 and the third transistor 113 of the pixel $P_{2,1}$ are turned on, whereby the data signal is applied to the second sub-pixel of the pixel $P_{2,1}$ through the data line D_2 , and the second sub-pixel electrode P2 of the pixel $P_{2,1}$ is charged, and the first and second sub-pixel electrodes P1 and P2 of the pixel $P_{1,1}$ are held. This is corresponding to State T3, as shown in Fig. 3(d).

[0047] Fig. 4 and Table 1 show simulation results for the gate signals g_1 , g_2 , g_3 and g_4 having a waveform same as that shown in Fig. 2. The final voltages charged in the sub-pixels P1 and P2 are almost identical. Thus, The HSD3 driving scheme according to the present invention has more uniform charging and better holding performance comparing to the HSD2 driving scheme.

Table 1: Simulation Results of the LCD at Frame Rate = 50Hz. (T_{ch} is the pixel charging time; W/L represents the sub-pixel width and length; V_p and V_{p'} are the sub-pixel voltages; Thold is the holding time; V_{hold} is the holding voltages; and ΔV represents the voltage difference between V_{p'} and V_{hold}.)

Driving Method	Sub-Pixel	Charging Check			After Feed-Through	Holding Check (Leakage Current)		
		T _{ch}	W/L	V _p (Charging Ratio)	V _{p'}	Thold	V _{hold}	ΔV
HSD2	P1	33us	210um /5um	14.76V (99.2%)	12.78V	19.96ms	11.77V	-1.02V
	P2			11.19V (87.3%)	9.05V		9.31V	+0.26V
HSD3	P1	33us	210um /5um	12.44V (91.5%)	10.11V	19.96ms	9.804V	-0.185V
	P2			12.44V (91.5%)	10.15V		9.848V	-0.181V

[0048] Fig. 5(a) shows partially and schematically an LCD 200 according to another embodiment of the present invention. The configuration of the LCD 200 is same as that of the LCD 100 shown in Fig. 1, except that the source of the third transistor 213 of each pixel $P_{n,m}$ is electrically coupled to the data line D_m . Fig. 5(b) shows time charts of the gate signals g_1 , g_2 , ..., and g_6 sequentially applied to the gate line G1, G2, ..., and G6, respectively, of the LCD. Each of the gate signals g_1 , g_2 , ..., and g_6 has a waveform same as that shown in Fig. 2. Accordingly, the pixel charging sequence is from sub-pixel (1) to sub-pixel (2) to sub-pixel (3), ..., to sub-pixel (n).

[0049] Fig. 6(a) shows pixel discharging processes of the LCD 200, indicated by the current leakage path 223, while Fig. 6(b) pixel charging processes of the LCD 200, indicated by the charging path 221 for the sub-pixel P1 and the charging path 222 for the sub-pixel P2.

[0050] According to the embodiments of the present invention as disclosed above, a half source channel amount is reduced and the aperture ratio is improved in the LCD with the HSD3 driving scheme, comparing to a conventional LCD. Further, the LCD of the present invention has good uniformity in charging and holding performance.

[0051] The foregoing description of the exemplary embodiments of the invention has been presented only for the purposes of illustration and description and is not intended to be exhaustive or to limit the invention to the precise forms disclosed. Many modifications and variations are possible in light of the above teaching.

[0052] The embodiments were chosen and described in order to explain the principles of the invention and their practical application so as to activate others skilled in the art to utilize the invention and various embodiments and with various modifications as are suited to the particular use contemplated. Alternative embodiments will become apparent to those skilled in the art to which the present invention pertains without departing from its spirit and scope. Accordingly,

the scope of the present invention is defined by the appended claims rather than the foregoing description and the exemplary embodiments described therein.

Claims

1. A liquid crystal display (LCD), comprising:

(a) a plurality of pixels, $\{P_{n,m}\}$, spatially arranged in the form of a matrix, $n = 1, 2, \dots, N$, and $m = 1, 2, \dots, M$, and N, M being an integer greater than zero, each pixel $P_{n,m}$ comprising a first sub-pixel electrode, a second subpixel electrode, a first switching element electrically coupled to the first sub-pixel electrode, a second switching element electrically coupled to the second sub-pixel electrode, and a third switching element electrically coupled to the first and second switching elements;

(b) a plurality of gate lines, $\{G_n\}$, spatially arranged along a row direction, wherein each pair of two neighboring gate lines G_n and G_{n+1} defines a pixel row $P_{n,\{m\}}$ of the pixel matrix $\{P_{n,m}\}$ therebetween and is electrically coupled to the first and second switching elements of each pixel $P_{n,m}$ in the pixel row $P_{n,\{m\}}$, respectively; and

(c) a plurality of data lines, $\{D_m\}$, spatially arranged crossing the plurality of gate lines $\{G_n\}$ along a column direction perpendicular to the row direction, wherein each pair of two neighboring data lines D_m and D_{m+1} defines a pixel column, $P_{\{n\},m}$, of the pixel matrix $\{P_{n,m}\}$ therebetween, and is electrically coupled to the third switching element of each pixel $P_{n,m}$ in the pixel column, $P_{\{n\},m}$.

2. The LCD of claim 1, wherein the first sub-pixel electrode and the first switching element of the pixel $P_{n,m}$ define a first sub-pixel, $P_{n,m}(1)$, of the pixel $P_{n,m}$, while the second sub-pixel electrode and the second switching element of the pixel $P_{n,m}$ define a second sub-pixel, $P_{n,m}(2)$, of the pixel $P_{n,m}$.

3. The LCD of claim 1, wherein each of the first, second and third switching elements of the pixel $P_{n,m}$ of the pixel matrix $\{P_{n,m}\}$ is a field-effect thin film transistor having a gate, a source and a drain.

4. The LCD of claim 3, wherein the gate, the source and the drain of the first switching element of the pixel $P_{n,m}$ are electrically coupled to the gate line G_{n+1} , the source of the second switching element of the pixel $P_{n,m}$, and the first subpixel electrode of the pixel $P_{n,m}$, respectively; and wherein the gate, the source and the drain of the second switching element of the pixel $P_{n,m}$ are electrically coupled to the gate line G_n , the source of the first switching element of the pixel $P_{n,m}$, and the second sub-pixel electrode of the pixel $P_{n,m}$, respectively.

5. The LCD of claim 4, wherein the gate, the source and the drain of the third switching element of the pixel $P_{n,m}$ are electrically coupled to the gate line G_{n+2} , the data line D_m , and the sources of the first and second switching elements of the pixel $P_{n,m}$, respectively.

6. The LCD of claim 4, wherein the gate and the drain of the third switching element of the pixel $P_{n,m}$ are electrically coupled to the gate line G_{n+2} and the sources of the first and second switching elements of the pixel $P_{n,m}$, respectively, while the source of the third transistor of the pixel $P_{n,m}$ is electrically coupled to the data line D_m when n is an odd positive integer, or electrically coupled to the data line D_{m+1} when n is an even positive integer.

7. The LCD of claim 1, further comprising:

(a) a gate driver for generating a plurality of gate signals respectively applied to the plurality of gate lines $\{G_n\}$, wherein the plurality of gate signals is configured to turn on the switching elements connected to the plurality of gate lines $\{G_n\}$ in a predefined sequence; and

(b) a data driver for generating a plurality of data signals respectively applied to the plurality of data lines $\{D_m\}$, wherein the plurality of data signals is configured such that any two neighboring data signals have inverted polarities.

8. A method of driving a liquid crystal display (LCD), comprising the steps of:

(a) providing an LCD panel comprising:

(i) a plurality of pixels, $\{P_{n,m}\}$, spatially arranged in the form of a matrix, $n = 1, 2, \dots, N$, and $m = 1, 2, \dots, M$, and N, M being an integer greater than zero, each pixel $P_{n,m}$ comprising a first subpixel electrode, a

second sub-pixel electrode, a first switching element electrically coupled to the first sub-pixel electrode, a second switching element electrically coupled to the second subpixel electrode, and a third switching element electrically coupled to the first and second switching elements;

(ii) a plurality of gate lines, $\{G_n\}$, spatially arranged along a row direction, wherein each pair of two neighboring gate lines G_n and G_{n+1} defines a pixel row $P_{n,\{m\}}$ of the pixel matrix $\{P_{n,m}\}$ therebetween and is electrically coupled to the first and second switching elements of each pixel $P_{n,m}$ in the pixel row $P_{n,\{m\}}$, respectively; and

(iii) a plurality of data lines, $\{D_m\}$, spatially arranged crossing the plurality of gate lines $\{G_n\}$ along a column direction perpendicular to the row direction, wherein each pair of two neighboring data lines D_m and D_{m+1} defines a pixel column, $P_{\{n\},m}$, of the pixel matrix $\{P_{n,m}\}$ therebetween, and is electrically coupled to the third switching element of each pixel $P_{n,m}$ in the pixel column, $P_{\{n\},m}$; and

(b) applying a plurality of gate signals to the plurality of gate lines $\{G_n\}$ and a plurality of data signals to the plurality of data lines $\{D_m\}$, respectively, wherein the plurality of gate signals is configured to turn on the switching elements connected to the plurality of gate lines $\{G_n\}$ in a predefined sequence, and the plurality of data signals is configured such that any two neighboring data signals have inverted polarities.

9. The method of claim 8, wherein each of the first, second and third switching elements of the pixel $P_{n,m}$ of the pixel matrix $\{P_{n,m}\}$ is a field-effect thin film transistor having a gate, a source and a drain.

10. The method of claim 9, wherein the gate, the source and the drain of the first switching element of the pixel $P_{n,m}$ are electrically coupled to the gate line G_{n+1} , the source of the second switching element of the pixel $P_{n,m}$, and the first subpixel electrode of the pixel $P_{n,m}$, respectively; and wherein the gate, the source and the drain of the second switching element of the pixel $P_{n,m}$ are electrically coupled to the gate line G_n , the source of the first switching element of the pixel $P_{n,m}$, and the second sub-pixel electrode of the pixel $P_{n,m}$, respectively.

11. The method of claim 10, wherein the gate, the source and the drain of the third switching element of the pixel $P_{n,m}$ are electrically coupled to the gate line G_{n+2} , the data line D_m , and the sources of the first and second switching elements of the pixel $P_{n,m}$, respectively.

12. The method of claim 11, wherein the gate and the drain of the third switching element of the pixel $P_{n,m}$ are electrically coupled to the gate line G_{n+2} and the sources of the first and second switching elements of the pixel $P_{n,m}$, respectively, while the source of the third transistor of the pixel $P_{n,m}$ is electrically coupled to the data line D_m when n is an odd positive integer, or electrically coupled to the data line D_{m+1} when n is an even positive integer.

13. The method of claim 8, wherein each of the plurality of gate signals is configured to have a waveform, wherein the waveform has a first voltage potential V_1 in a first duration, Γ_1 , a second voltage potential V_2 in a second duration, Γ_2 , a third voltage potential V_3 in a third duration, Γ_3 , a fourth voltage potential V_4 in a fourth duration, Γ_4 , and a fifth voltage potential V_5 in a fifth duration, Γ_5 , wherein the $(j+1)$ -th duration Γ_{j+1} is immediately after the j -th duration Γ_j , $j = 1, 2, 3$ and 4 , and wherein $V_1 = V_3 = V_5 > V_2 = V_4$, $\Gamma_2 = \Gamma_1/2$, $\Gamma_3 = (\Gamma_1 - t)/2$, $\Gamma_4 = t$, $\Gamma_5 = \Gamma_3$, and $\Gamma_1 \gg t$.

14. The method of claim 13, wherein the waveform of each of the gate signals is sequentially shifted from one another by the duration of Γ_1 .

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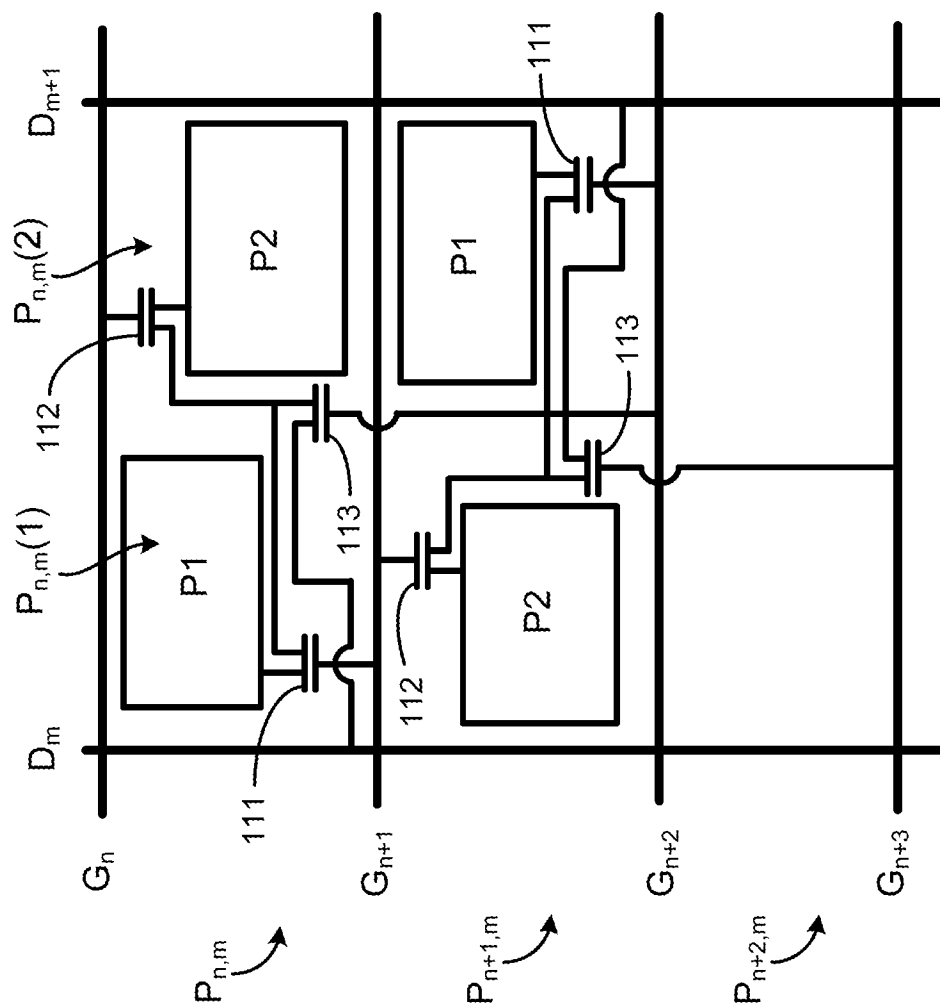


Fig. 1

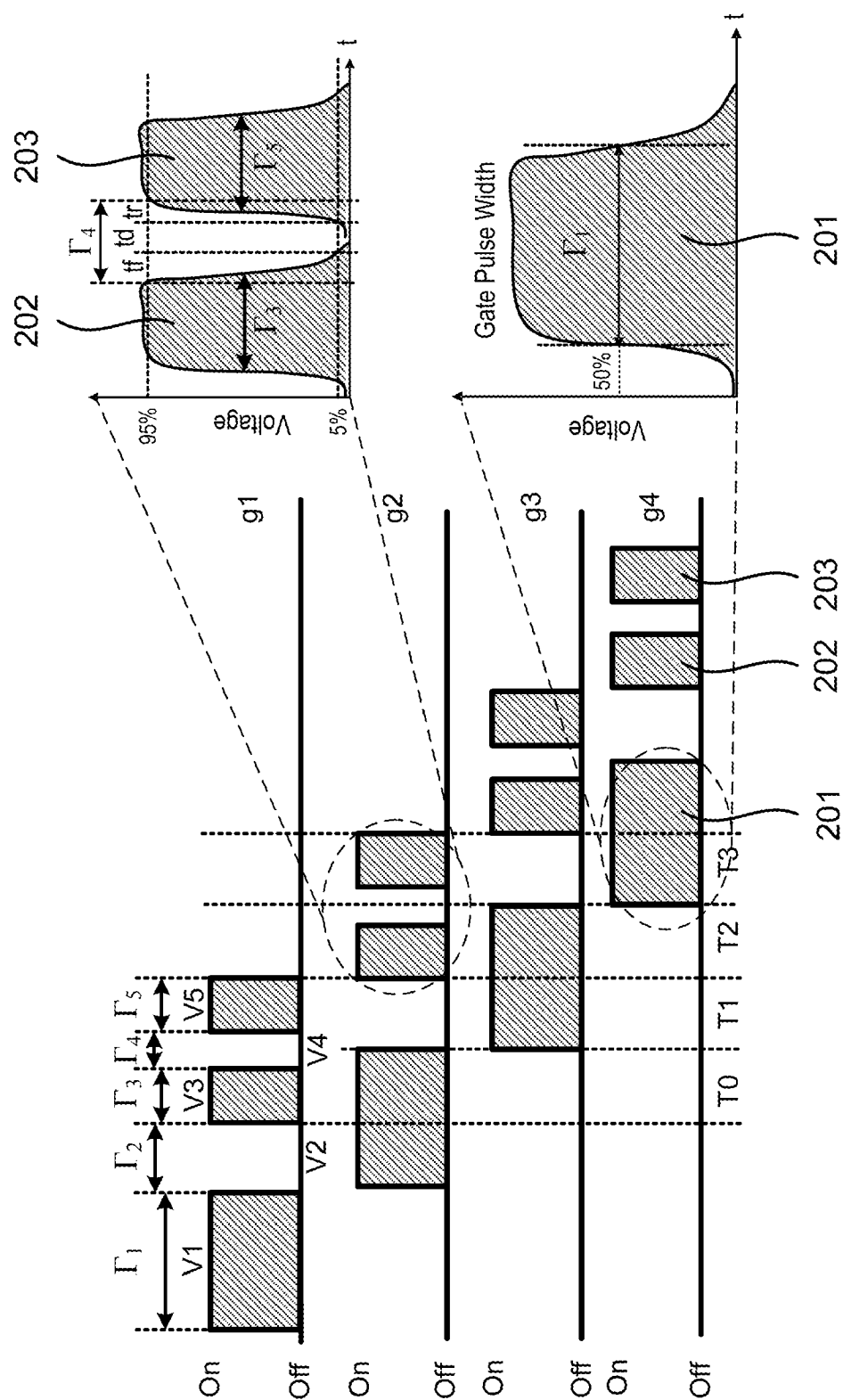


Fig. 2

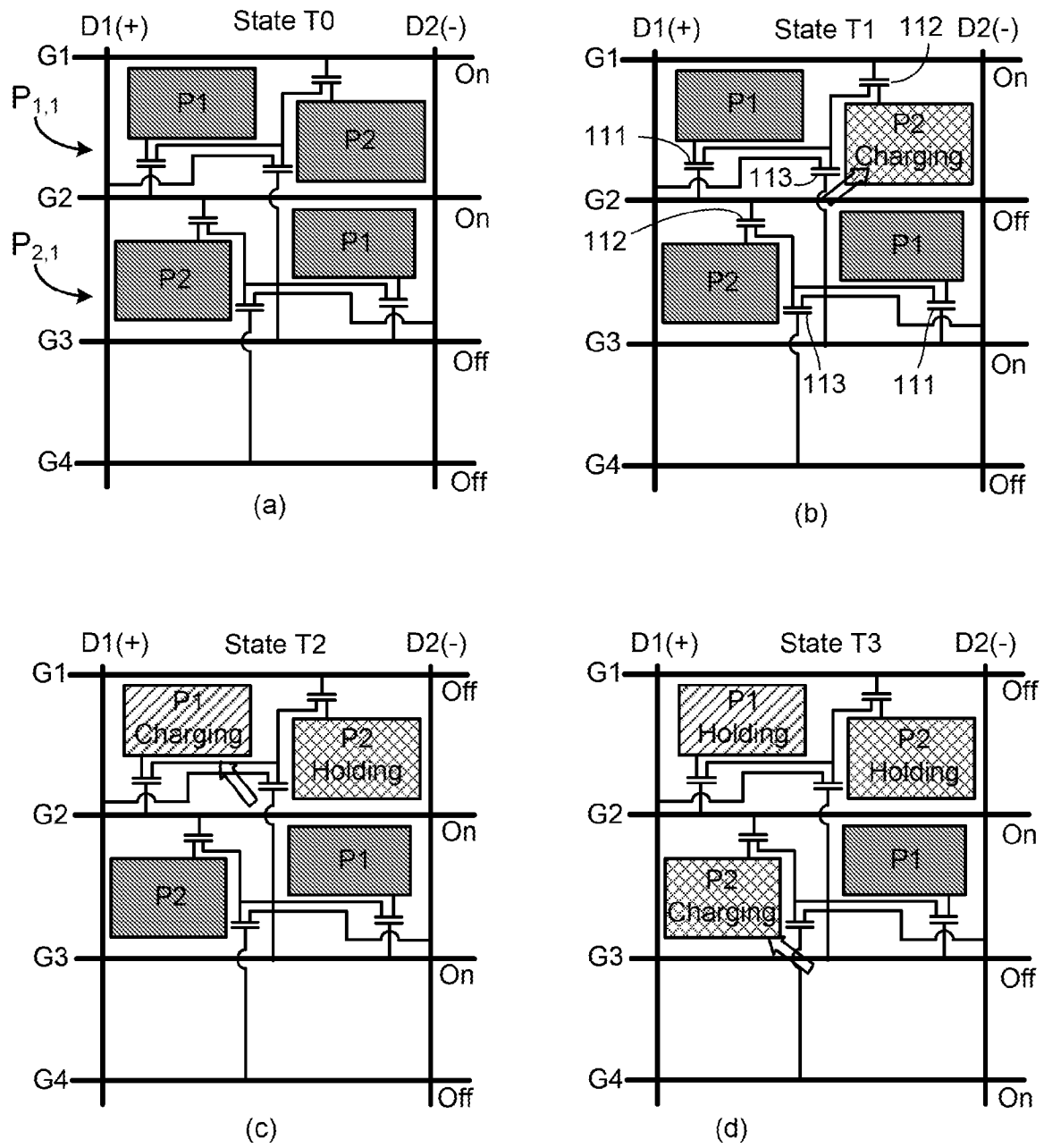


Fig. 3

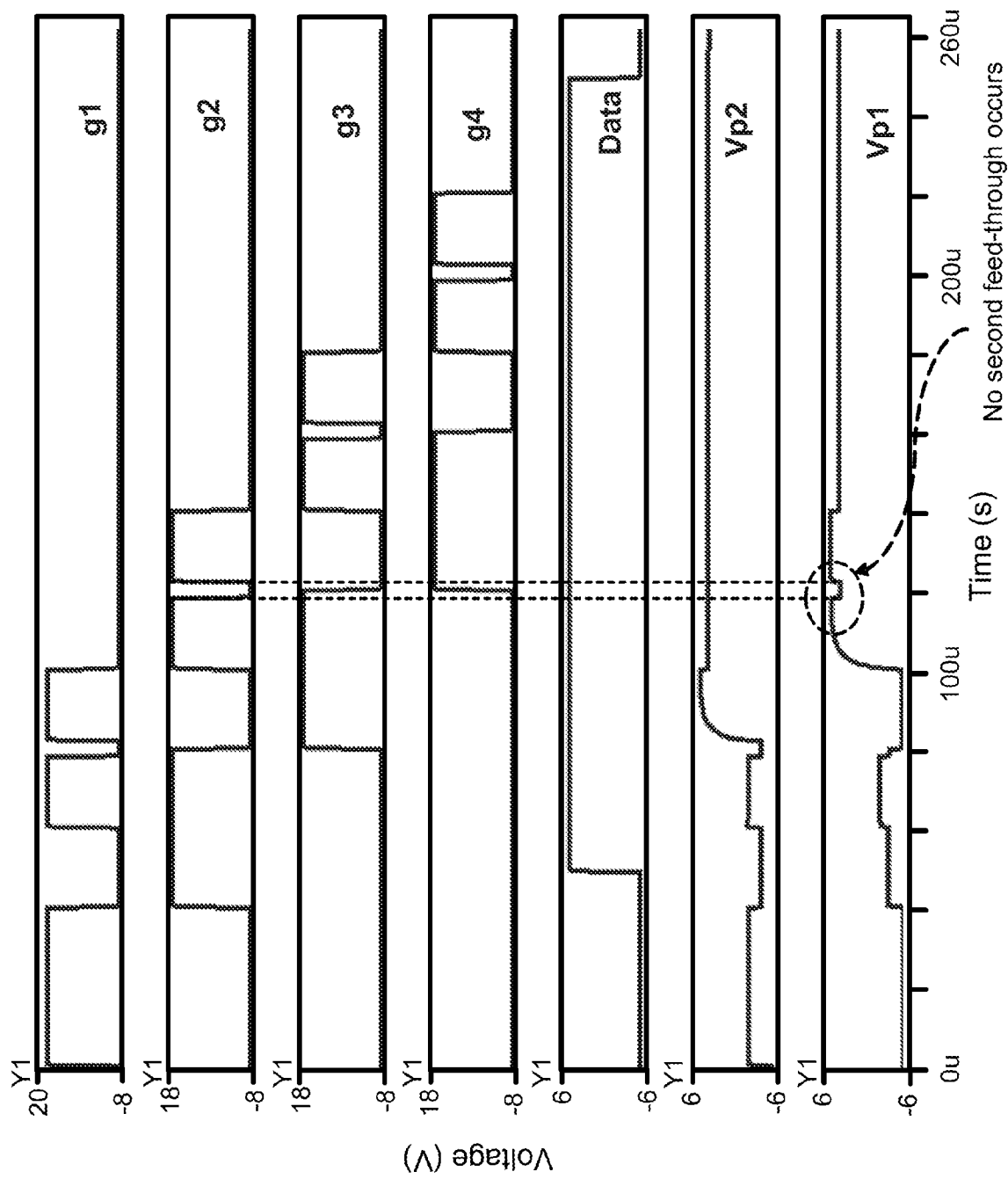


Fig. 4

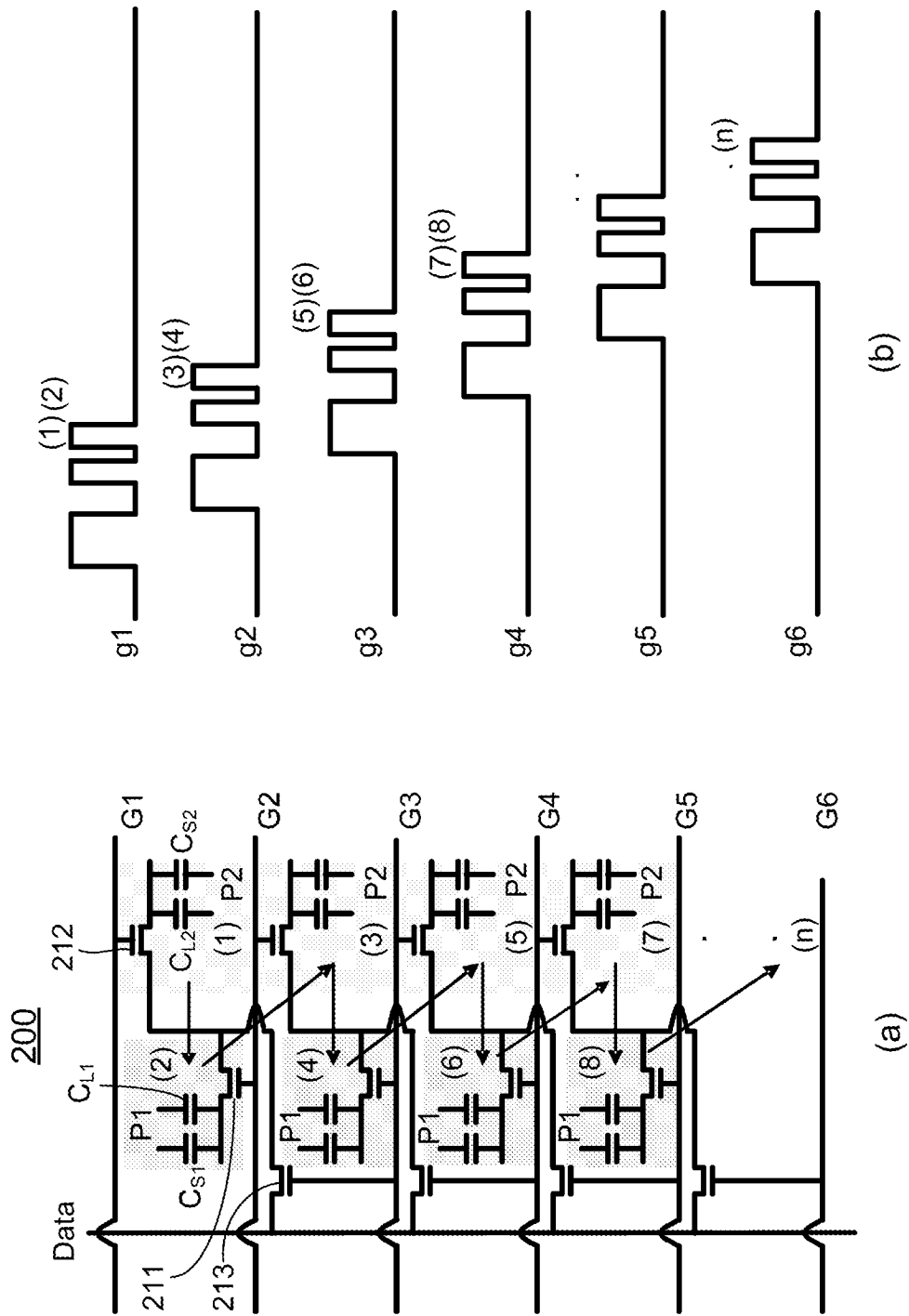


Fig. 5

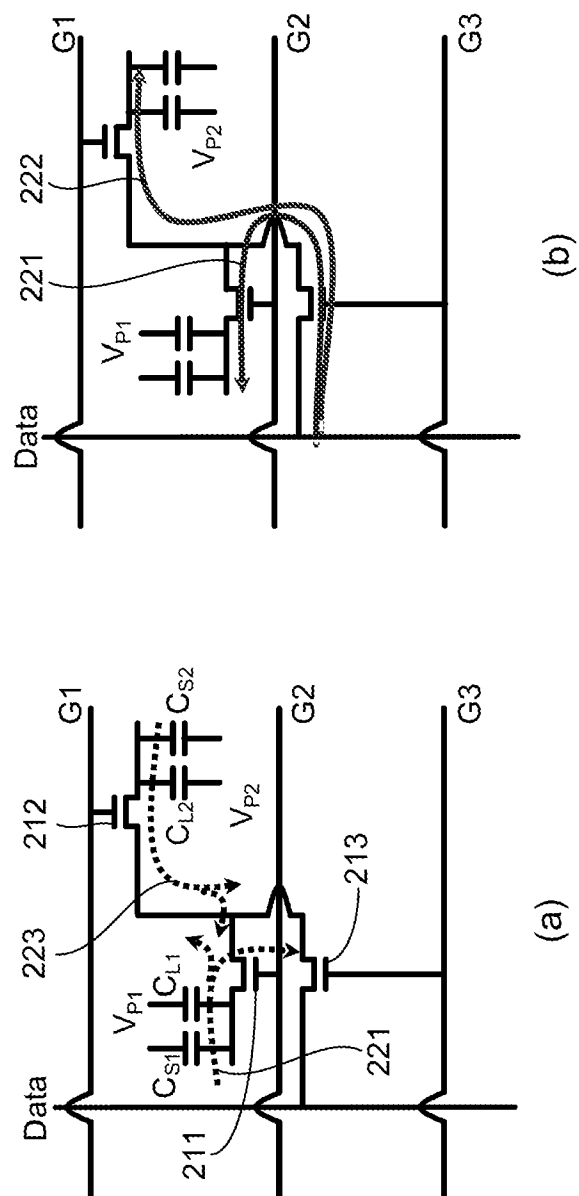


Fig. 6

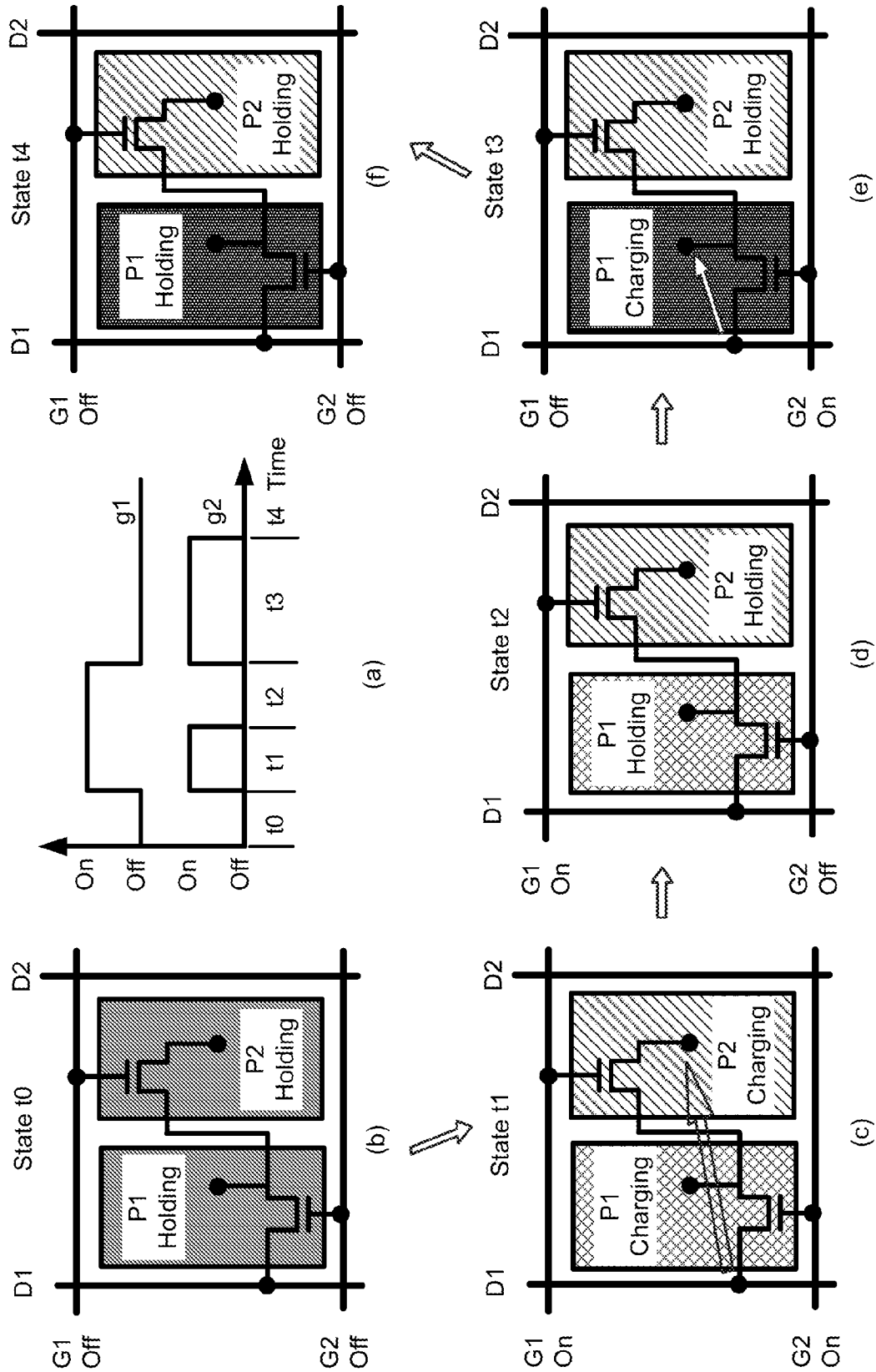


Fig. 7 (Related Art)



EUROPEAN SEARCH REPORT

Application Number
EP 10 16 5588

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
X	US 2001/045925 A1 (LIBSCH FRANK R [US] ET AL) 29 November 2001 (2001-11-29) * paragraphs [0005] - [0007], [0033] - [0035], [0044]; figures 5,7,8,9,16 *	1-14	INV. G09G3/36
X	US 2008/048957 A1 (CHIANG MIN-FENG [TW] ET AL) 28 February 2008 (2008-02-28) * paragraphs [0007], [0008], [0024] - [0030], [0058]; figure 3 *	1-4,7-10	
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The present search report has been drawn up for all claims			TECHNICAL FIELDS SEARCHED (IPC)
			G09G
Place of search		Date of completion of the search	Examiner
The Hague		15 March 2011	Pichon, Jean-Michel
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document			

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**ANNEX TO THE EUROPEAN SEARCH REPORT
ON EUROPEAN PATENT APPLICATION NO.**

EP 10 16 5588

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15-03-2011

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CN 101404134 A	08-04-2009	NONE	

专利名称(译)	液晶显示器及其驱动方法		
公开(公告)号	EP2360670A1	公开(公告)日	2011-08-24
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[标]申请(专利权)人(译)	友达光电股份有限公司		
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[标]发明人	TSAI YU CHENG LEE KUO HSIEN LU CHAO LIANG KUO JING TIN		
发明人	TSAI, YU-CHENG LEE, KUO-HSIEN LU, CHAO-LIANG KUO, JING-TIN		
IPC分类号	G09G3/36		
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代理机构(译)	LANG , CHRISTIAN		
优先权	12/703896 2010-02-11 US		
外部链接	Espacenet		

摘要(译)

液晶显示器 (LCD) 及其驱动方法。在一个实施例中, LCD包括沿行方向空间排列的多条栅极线{Gn};多个数据线{Dm}, 沿垂直于行方向的列方向在空间上排列, 和多个像素{Pn, m}, 以矩阵的形式在空间上排列, 其中 $m = 1, 2, \dots, M$, $n = 1, 2, \dots, N$, M和N是正整数。每个像素 $P_{n, m}$ 限定在两条相邻的栅极线 G_n 和 G_{n+1} 与两条相邻的数据线 D_m 和 D_{m+1} 之间, 并包括第一子像素电极, 第二子像素电极, 第一晶体管 (111) 具有电耦合到栅极线 G_{n+1} 的栅极, 电耦合到第一子像素电极的源极和漏极, 具有电耦合到栅极线 G_n 的栅极的第二晶体管 (112), 电耦合到栅极线 G_n 的源极第一晶体管的源极和漏极电耦合到第二子像素电极, 第三晶体管 (113) 具有电耦合到栅极线 G_{n+2} 的栅极, 源极电耦合到两个相邻数据之一线 D_m 和 D_{m+1} 以及电耦合到第一和第二晶体管的源极的漏极

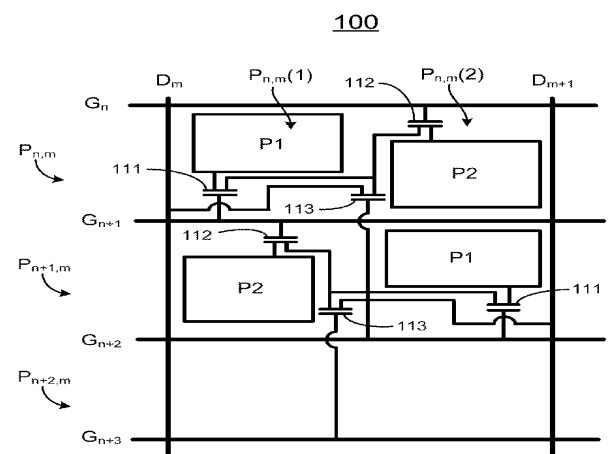


Fig. 1