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(54) **Array substrate, methods of manufacturing the array substrate, and liquid crystal display device having the array substrate**

Array-Substrat, Verfahren zur Herstellung des Array-Substrats, Substrat und Flüssigkristallanzeigevorrichtung mit dem Array-Substrat

Substrat de réseau, procédé de fabrication du substrat de réseau, et dispositif d'affichage à cristaux liquides disposant du substrat de réseau

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Description

BACKGROUND OF THE INVENTION

[0001] FIELD OF THE INVENTION

[0002] The present invention relates to an array substrate, a method of manufacturing the array substrate, and a liquid crystal display (LCD) device having the array substrate. More particularly, exemplary embodiments of the present invention relate to array substrate having an improved display quality, a method of manufacturing the array substrate, and an LCD device having the array substrate.

[0003] DISCUSSION OF THE BACKGROUND

[0004] An LCD device of a mobile patterned vertical alignment (mPVA) mode (hereinafter, an mPVA LCD device) may have an optical mode, in which circular polarization is applied, and in which the transmissivity is relatively superior to other modes.

[0005] The mPVA LCD device having the circular polarization optical mode may have disadvantages related to viewing properties or contrast ratio compared to a PVA mode in which to linear polarization is applied. However, the transmissivity of the linear polarization PVA mode may be lower than the transmissivity of the circular polarization PVA mode.

[0006] Thus, when a linear polarization optical mode is applicable to an mPVA mode, the aperture ratio of a pixel may be large, and a liquid crystal director may form an angle of about 45 degrees with respect to the polarization axis of a polarizer, in order to improve transmissivity.

[0007] However, the linear polarization mPVA mode liquid crystal is controlled by a fringe field when a slit portion is formed on a common electrode of a color filter substrate. Accordingly, the linear polarization mPVA mode is disadvantageous in that transmissivity may be reduced.

[0008] To overcome these problems, a micro-slit mode, in which a slit is formed on a pixel electrode of an array substrate, rather than on the common electrode, may be used. However, the micro-slit mode is disadvantageous in that controlling the liquid crystal at edges of micro-slits or between the micro-slits formed on the pixel electrode is difficult, and the LCD device display quality may be deteriorated thereby.

[0009] The following documents represent background art which can be useful to understand the invention.

[0010] US2006061722 discloses a multi-domain vertical alignment liquid crystal display having a pixel electrode which contains micro-slits and wherein circular polarization is used to increase the transmission of the cell.

[0011] US2004100607 discloses a liquid crystal display having a transparent shielding electrode (fig. 4, item 88) however the shielding electrode is placed at the same level than the pixel electrode.

SUMMARY OF THE INVENTION

[0012] The present invention provides an array substrate according to claim 1.

[0013] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention, and together with the description serve to explain the principles of the invention.

[0015] FIG. 1 is a plan view showing a liquid crystal display (LCD) device according to an exemplary embodiment of the present invention.

[0016] FIG. 2 is an enlarged plan view showing an example of a pixel area shown as FIG. 1.

[0017] FIG. 3 is a cross-sectional view taken along line I-I' in FIG. 2.

[0018] FIG. 4A, FIG. 4B, FIG. 4C, FIG. 4D, FIG. 4E, FIG. 4F, FIG. 4G, FIG. 4H, and FIG. 4I are cross-sectional views showing a process for manufacturing the array substrate shown in FIG. 1, FIG. 2, and FIG. 3.

[0019] FIG. 5A is a cross-sectional view taken along line II-II' in FIG. 2.

[0020] FIG. 5B is a cross-sectional view taken along line III-III' in FIG. 2.

[0021] FIG. 6 is a cross-sectional view showing movements of a liquid crystal layer between the shielding electrode and the outline portion of a pixel electrode in FIG. 5A and FIG. 5B.

[0022] FIG. 7A is an image observing light transmissivity of the LCD device in which slit portions are formed in a diagonal direction.

[0023] FIG. 7B is an image observing light transmissivity of the LCD device shown as FIG. 1, FIG. 2, FIG. 3, FIG. 4, FIG. 5A, and FIG. 5B.

[0024] FIG. 8 is a graph representing response time of LCD devices shown as FIG. 7A and FIG. 7B;

[0025] FIG. 9 is an enlarged plan view showing a pixel area of the array substrate of the LCD device according to an example.

[0026] FIG. 10 is a cross-sectional view taken along line IV-IV' in FIG. 9.

[0027] FIG. 11A, FIG. 11B, FIG. 11C, and FIG. 11D are cross-sectional views showing a process for manufacturing the array substrate shown in FIG. 9 and FIG. 10.

[0028] FIG. 12A is an image showing light transmissivity of the LCD device having an array substrate identical to the array substrate shown as FIG. 9 and FIG. 10 except that a pixel electrode does not have an outline portion.

[0029] FIG. 12B is an image showing light transmis-

sivity of the LCD device having the array substrate shown in FIG. 9 and FIG. 10.

[0030] FIG. 13 is a graph showing a response time of the LCD devices shown in FIG. 12A and FIG. 12B.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

[0031] Hereinafter, the present invention will be explained in detail with reference to the accompanying drawings.

[0032] FIG. 1 is a plan view showing a liquid crystal display (LCD) device 100 according to an exemplary embodiment of the present invention.

[0033] Referring to FIG. 1, the LCD device 100 according to an exemplary embodiment of the present invention includes a display panel 10 and a driving part 5.

[0034] The display panel 10 includes an array substrate 101, an opposite substrate 105, and a liquid crystal layer. The array substrate 101 and the opposite substrate 105 opposite to each other are joined by a sealing member 102 having a frame shape. Liquid crystals are disposed in the space between the array substrate 101, the opposite substrate 105, and the sealing member 102 to form the liquid crystal layer.

[0035] The opposite substrate 105 is disposed in a direction from the ground, and the array substrate 101 is disposed in a direction toward the ground in FIG. 1.

[0036] The opposite substrate 105 may be a color filter substrate having an RGB color filter. The array substrate 101 is an element substrate being driven through an active matrix driving process using a thin-film transistor (TFT) element.

[0037] In addition, the array substrate 101 includes a pixel electrode having a micro-slit pattern formed therethrough in the LCD device 100, and the opposite substrate 105 includes a common electrode having a plane shape formed therethrough.

[0038] The array substrate 101 may have a substantially rectangular shape. In this embodiment, a horizontal direction of the array substrate 101 is defined as 'x', and a vertical direction of the array substrate 101 is defined as 'y'.

[0039] FIG. 2 is an enlarged plan view showing an example of a pixel area shown as FIG. 1. FIG. 3 is a cross-sectional view taken along line I-I' in FIG. 2.

[0040] Referring to FIG. 1, FIG. 2, FIG. 3, a display device 100 includes an array substrate 101, an opposite substrate 105, and a liquid crystal layer 107.

[0041] A plan view of the array substrate 101 is shown in FIG. 2, and a cross-sectional view of the array substrate 101, the opposite substrate 105, and the liquid crystal layer 107 is shown in FIG. 3.

[0042] Referring to FIG. 1, FIG. 2, and FIG. 3, the array substrate 101 according to the present invention includes a lower substrate 102, a plurality of gate lines 111, a plurality of data lines 115, a switching element 108, a shielding electrode 160, and a pixel electrode 170.

[0043] FIG. 4A, FIG. 4B, FIG. 4C, FIG. 4D, FIG. 4E, FIG. 4F, FIG. 4G, FIG. 4H, and FIG. 4I are cross-sectional views showing a process for manufacturing the array substrate 101 as shown in FIG. 1, FIG. 2, and FIG. 3.

[0044] According to a process for manufacturing an array substrate in this exemplary embodiment, a gate metal, which may be a two-layer structure formed of aluminum (Al) and molybdenum (Mo), is deposited to a thickness of about 3,000 Å via a sputtering process on the lower substrate 102, an etching process is performed as shown in FIG. 4A to form the gate lines 111 and the gate electrode 112 protruded from the gate line 111. The gate lines 111 are parallel with the horizontal direction to be extended on the lower substrate 102.

[0045] Then, a gate insulation layer 113 and a semiconductor pattern 114 are formed as shown in FIG. 3 and FIG. 4B. The gate insulation layer 113, which may be formed of silicon nitride (SiNx), is deposited to have a thickness of about 4,500 Å on the gate lines 111. A semiconductor layer, which may be made of amorphous silicon (n+ a-Si), is deposited to a thickness of about 2,000 Å on the gate insulation layer 113, and an amorphous silicon (n+ a-Si) layer doped at a high concentration is deposited to a thickness of about 500 Å on the gate insulation layer 113. The amorphous silicon (n+ a-Si) layers are etched to form a semiconductor pattern 114. The semiconductor pattern 114 is formed on the gate insulation layer 113 on a location corresponding to the gate electrode 112.

[0046] As shown in FIG. 3 and FIG. 4C, a data metal, which may be a three-layer structure formed of molybdenum-aluminum-molybdenum, is deposited to a thickness of about 300 Å, 2,500 Å, and 1,000 Å, respectively, on the gate insulation layer 113, and is patterned to form the data line 115, the source electrode 121, and the drain electrode 123.

[0047] The data lines 115 extend in the vertical direction 'y' on the gate insulation layer 113. The source electrode 121 protrudes from the data line 11 near the point where the gate line 111 crosses the data line 115, to extend on the semiconductor pattern 114 on the gate electrode 112. The drain electrode 123 is disposed on the semiconductor pattern 114 opposite to the source electrode 121, and extends on the gate insulation layer 113 in a portion of a pixel area PA.

[0048] In this exemplary embodiment, the pixel area PA has a substantially rectangular shape that extends in the vertical direction. Alternatively, the pixel area PA may have a Z-shape, such that the gate line 111 is arranged in the horizontal direction around the pixel area PA, and the data line 115 is arranged in the vertical direction around the pixel area PA.

[0049] When the semiconductor layer and the data metal layer are etched by a single etching process, the semiconductor pattern 114 is formed below the data line 115, the source electrode 121, and the drain electrode 123, and is formed on the gate line 112 on the gate insulation layer 113. A channel region, which is disposed

between the source electrode 121 and the drain electrode 123, is formed semiconductor pattern 114 using an etch-back process.

[0050] The gate electrode 112, the gate insulation layer 113, the semiconductor pattern 114, the source electrode 121, and the drain electrode 123 compose a switching element 108.

[0051] Then, as shown in FIG. 4D, a first passivation layer 130 covering the lower substrate 102 having the data line 115 formed thereon is formed. The first passivation layer 130, which may be made of silicon nitride (SiNx), may be deposited to a thickness of about 2,000 Å. A contact hole may be formed in the first passivation layer 130 to expose a portion of the drain electrode 123.

[0052] As shown in FIG. 4E, an organic insulation layer 140 is formed to a thickness of about 2.0 μm on the first passivation layer 130. A contact hole 143 exposing a portion of the drain electrode 123 may be formed in the organic insulation layer 140 and the first passivation layer 130. The organic insulation layer 140 reduces a parasitic capacitance between a pixel electrode 170, which will be described below, and the data line 115. When the pixel electrode 170 is formed to not overlap with the data line 115, the organic insulation layer 140 may be omitted.

[0053] As shown in FIG. 4F, the shielding electrode 160 is formed on the organic insulation layer 140. The shielding electrode 160 prevents parasitic capacitance from forming between the data line 115, the gate line 111, and the pixel electrode 170. Alternatively, the shielding electrode 160 may form a storage capacitor with the pixel electrode 170 to store a pixel voltage applied to the pixel electrode 170 for one frame.

[0054] An optically transparent and electrically conductive material such as indium tin oxide (ITO) or indium zinc oxide (IZO) is deposited to a thickness of about 900 Å on the organic insulation layer 140, and is patterned to form the shielding electrode 160.

[0055] FIG. 5A is a cross-sectional view taken along line II-II' in FIG. 2. FIG. 5B is a cross-sectional view taken along line III-III' in FIG. 2.

[0056] Referring to FIG. 2, FIG. 5A, and FIG. 5B, the shielding electrode 160 is formed on the gate line 111 and the data line 115 to shield in the width direction. That is, the shielding electrode 160 is formed on the gate line 111 between the pixel areas PA and the data line 115, and a line width of the shielding electrode 160 is wider than that of the gate line 111 and the data line 115, respectively. Thus, the shielding electrode 160 extends to an edge of the pixel area PA. In this exemplary embodiment, the shielding electrode 160 is formed from the optically transparent and electrically conductive material so that an aperture ratio of the pixel area PA is not reduced even if the shielding electrode 160 overlaps with an edge of the pixel area PA.

[0057] As shown in FIG. 4G, a second passivation layer 165 is formed on the shielding electrode 160. The second passivation 165 layer may be formed of a material and a thickness substantially identical to the first passivation layer 130. A contact hole may be formed in the second passivation layer 165, in which the contact hole is connected to a contact hole 143 formed in the organic insulation layer 140.

[0058] As shown in FIG. 4H, an optically transparent and electrically conductive material such as ITO or IZO is deposited to a thickness of about 900 Å on the second passivation layer 165, and is patterned to form the pixel electrode 170. The pixel electrode 170 is connected to the drain electrode 123 through the contact hole 143.

[0059] Referring to FIG. 2, FIG. 5A, and FIG. 5B, the pixel electrode 170 includes a frame portion 175, a connection portion 171, and a strip portion 173. The frame portion 175 is formed on the second passivation layer 165 and corresponds to the edge of the pixel area PA along the gate line 111 and the data line 115. A portion of the frame portion 175 may be formed to overlap with the shielding electrode 160 that extends to the edge of the pixel area PA in the width direction. As shown in FIG. 5A and FIG. 5B, a portion of the frame portion 175 may be formed to overlap with the gate line 111 and the data line 115 in the width direction.

[0060] The connection portions 171 divide the pixel area PA into a plurality of domains to connect to the frame portion 175. The connection portions 171 are disposed in a direction crossing an extending direction of the gate line 111 and the data line 115, respectively.

[0061] In this exemplary embodiment, as shown in FIG. 2, the pixel electrode 170 includes two of the connection portions 171. One connection portion 171 is disposed in a direction at an angle of 45 degrees with respect to the gate line 111, and another connection portion 171 is disposed in a direction at an angle of 135 degrees with respect to the gate line 111.

[0062] Two of the connection portions 171 extend to diagonal directions of the pixel electrode 170, respectively. Thus, the connection portions 171 are disposed in an X-shape. Accordingly, the pixel area PA is divided into eight domains by the connection portions 171.

[0063] The strip portions 173 are parallel with each other on the pixel area PA domains, respectively. The strip portions 173 protrude from side surfaces of the connection portion 171 to connect to the frame portion 175. The strip portions 173 are substantially parallel with the data line 115 on a domain contacting the gate line 111, and the strip portions 173 are substantially parallel with the gate line 111 on a domain contacting the data line 115.

[0064] In this exemplary embodiment, two frame portions are disposed on one pixel area PA adjacent to each other in the data line 115 direction to connect to each other thus forming the pixel electrode 170. Thus, the length of the horizontal direction and the length of the vertical direction of the pixel electrode 170 are almost identical to each other. Accordingly, the length of the horizontal direction and the length of the vertical direction of the strip portions 173 are almost identical to each other.

[0065] When a data signal is applied from the driving part 5 to the data line 115, and a gate signal is applied

to the gate line 111, the data signal is applied to the pixel electrode 170 via the switching element 108 as a pixel voltage.

[0066] In this exemplary embodiment, a portion of the frame portion 175 of the pixel electrode 170 overlaps with the data line 115 and the gate 111, but the shielding electrode 160 forms a parasitic capacitance with the data line 115 and prevents a parasitic capacitance from being formed between the pixel electrode 170 and the data line 115, thus preventing a distorted data signal.

[0067] Finally, as shown in FIG. 4I, a lower alignment layer 168 covering the pixel electrode 170 is formed.

[0068] The lower alignment layer 168 and the opposite substrate 105, which will be described below, make liquid crystal molecules of the liquid crystal layer 107 align in a perpendicular direction. That is, the liquid crystal molecules are aligned in the direction from the array substrate 101 toward the opposite substrate 105 in a first stage.

[0069] The array substrate may further include a lower polarizer 30. As shown in FIG. 4I, the lower polarizer 30 is attached on the lower substrate 102 to be manufactured in the array substrate 101.

[0070] The lower polarization axis of the lower polarizer 30 is parallel with extending directions of the connection portions 171, that is, diagonal directions. Accordingly, the lower polarization axis is disposed in a direction at an angle of about 45 degrees or about 135 degrees with respect to the extending direction of the slit portion 173.

[0071] Referring to FIG. 1, FIG. 2, and FIG. 3, the opposite substrate 105 may include an upper substrate 104, a light-blocking pattern 181, a color filter pattern 185, an overcoating layer 187, a common electrode 190, an upper alignment layer 60, and an upper polarizer 70.

[0072] The light-blocking pattern 181 is formed below the upper substrate 104 in correspondence with the gate line 111, the data line 115, and the switching element 108. Thus, a color filter pattern 185 is formed on the upper substrate corresponding to the pixel area PA. A color filter pattern 185 may include, for example, a red filter, a green filter, and a blue filter. The red filter, the green filter, and the blue filter may be disposed in order on each pixel area PA in the horizontal direction x.

[0073] The overcoating layer 187 covers the color pattern 185 and the light-blocking pattern 181, and the common electrode 190 is formed on the overcoating layer 187.

[0074] The upper alignment layer 60 is formed on the common electrode 190 to vertically align a liquid crystal layer 107.

[0075] The upper polarizer 70 is attached on the upper substrate 104, and a polarization axis of the upper polarizer 70 may be substantially perpendicular to a polarization axis of the lower polarizer 30.

[0076] In this exemplary embodiment, where micro-slit patterns are formed between the strip portions 173 in the pixel electrode 170, a vertically aligned liquid crystal is used. Thus, a plurality of domains may be formed in the pixel area PA so that side viewing properties of the LCD device 100 may be improved.

[0077] FIG. 6 is a cross-sectional view showing movements of liquid crystal layer between the shielding electrode and the frame portion of a pixel electrode in FIG. 5A or FIG. 5B.

[0078] Referring to FIG. 6, when the pixel voltage is applied to the pixel electrode 170, an electric field boundary is formed between the shielding electrode 160 and the frame portion 175. An edge of the frame portion 175 overlaps with an upper portion of the shielding electrode 160 so that a horizontal component of the electric field boundary is formed stronger than that of an electric field boundary of the other portion. Thus, as shown in FIG. 6, it is recognized that a direction of liquid crystal molecules on the shielding electrode 160 is close to a horizontal direction.

[0079] That is, a second efficiency of liquid crystal molecules is increased in a condition where an electric field is applied, in which the liquid crystal molecules are placed at an edge of the pixel area PA. The second efficiency means a movement efficiency in which the liquid crystal molecules are rotated from a vertical direction to a horizontal direction.

[0080] Alternatively, a horizontal component of the electric field boundary may be substantially parallel with a vertical direction at an upper portion of the gate line 111, and may be substantially parallel with a horizontal direction at an upper portion of the data line 115. Also, a director of the liquid crystal molecules may be arranged in parallel with a length direction of the strip portions 173. The strip portions 173 are extended to the horizontal direction or the vertical direction depending on the domain.

[0081] That is, a horizontal component direction of the electric field boundary in which the liquid crystal molecules move is substantially the same as a length direction of the strip portion 173, which guides the director of the liquid crystal molecules. Thus, the liquid crystal molecules do not need to rotate in a horizontal direction. Accordingly, a third efficiency of the liquid crystal molecules is increased. The third efficiency means a rotation efficiency of the liquid crystal molecules in the horizontal direction.

[0082] Accordingly, the liquid crystal molecules may be effectively controlled at the edge of the pixel area PA so that texture generation is prevented, and the aperture ratio and response time of the liquid crystal molecules may be improved.

[0083] FIG. 7A is an image showing light transmissivity of the LCD device in which strip portions 173 are formed in diagonal directions. FIG. 7B is an image showing light transmissivity of the LCD device 100 shown as FIG. 1, FIG. 2, FIG. 3, FIG. 4A, FIG. 4B, FIG. 4C, FIG. 4D, FIG. 4E, FIG. 4F, FIG. 4G, FIG. 4H, FIG. 4I, FIG. 5A, and FIG. 5B.

[0084] FIG. 7A and FIG. 7B are images showing light transmissivity after an identical time from that when the

pixel voltage is applied. A dark portion of the images represents that light transmissivity is lower than other portions due to a slow response of liquid crystal molecules.

[0085] As shown in FIG. 7A, the strip portion 173 of the LCD device is extended to one of the diagonal directions unlike in the present exemplary embodiment. In addition, the frame portion 175 connecting to edge portions of the strip portion 173 is removed, a shielding electrode 160 as light-blocking metal is formed on a portion of the pixel area PA unlike in the present exemplary embodiment. The LCD device is substantially identical to the LCD device 100 of the present exemplary embodiment except in the-above mentioned manner.

[0086] The image in FIG. 7B is brighter than the image in FIG. 7A, and has a uniform luminance. A portion between an edge of the pixel area PA and the strip portions 173 is relatively darker than the other portion in FIG. 7B.

[0087] FIG. 8 is a graph showing a response time of the LCD device shown as FIG. 7A and FIG. 7B.

[0088] A horizontal axis represents an elapsed time after applying a pixel voltage, and a vertical axis represents a light transmissivity of a pixel area PA in FIG. 8. Referring to FIG. 8, it is recognized that a light transmissivity of the LCD device described in FIG. 7A, which is represented by the dashed line, is substantially lower than light transmissivity of the LCD device 100 of the present exemplary embodiment described in FIG. 7B, which is represented by the solid line, for a substantially identical time.

[0089] That is, the LCD device described in FIG. 7A and FIG. 8 does not include the light transmissivity improving effect by the frame portion 175 and the shielding electrode 160 unlike the present exemplary embodiment, and a direction of the slit portion 173 and a direction of horizontal electric field is different from each other in an angle of 45 degrees so that the second and third efficiency of the liquid crystal molecules is low.

[0090] The second and third efficiency of the liquid crystal molecules in the LCD device 100 of the present exemplary embodiment may be improved by the frame portion 175, the shielding electrode 160, and a direction of the strip portion 173 more than the LCD device described in FIG. 7A and FIG. 8, so that the display quality of the LCD device 100 may be improved.

[0091] FIG. 9 is an enlarged plan view showing a pixel area of the array substrate of the LCD device according to an example. FIG. 10 is a cross-sectional view taken along line IV-IV' in FIG. 9.

[0092] Referring to FIG. 9 and FIG. 10, an array substrate and a process for manufacturing the array substrate of this example is substantially identical to the array substrate and the process for manufacturing the array substrate described in FIG. 1 and FIG. 6, except a size of the pixel electrode 370 and an omitted organic insulation layer 140. Accordingly, the same reference numerals will be used to refer to the same elements as those described, and any detailed explanation will be omitted.

[0093] In this example, wherein the one pixel electrode 370 is disposed in the pixel area PA, and a long side of the pixel electrode 370 is substantially parallel with the direction in which the data line 315 extends. The pixel electrode is substantially identical to the pixel electrode 170 described in FIG. 1, FIG. 2, FIG. 3, FIG. 4A, FIG. 4B, FIG. 4C, FIG. 4D, FIG. 4E, FIG. 4F, FIG. 4G, FIG. 4H, FIG. 4I, FIG. 5A, FIG. 5B, and FIG. 6. Thus, the strip portions 373 of the vertical direction are longer than the strip portions 373 of the horizontal direction.

[0094] FIG. 11A, FIG. 11B, FIG. 11C, and FIG. 11D are cross-sectional views showing a process for manufacturing the array substrate shown as FIG. 9 and FIG. 10.

[0095] in a process for forming the array substrate according to this example, the organic insulation layer 140 is omitted, and a first passivation layer 330 is formed as shown in FIG. 11A, and a shielding electrode 360 is formed on the first passivation layer 330 as shown in FIG. 11B.. Then, a second passivation layer 365 covering the shielding electrode 360 is formed as shown in FIG. 11C. Then, the pixel electrode 370 is formed on the second passivation layer 365 and an alignment layer 368 is formed as shown in FIG. 11D.

[0096] A process for forming an organic insulation layer 140 is omitted to reduce a process step in this exemplary embodiment.

[0097] The LCD device in this example is substantially identical to the LCD device described in FIG. 1, FIG. 2, FIG. 3, FIG. 4A, FIG. 4B, FIG. 4C, FIG. 4D, FIG. 4E, FIG. 4F, FIG. 4G, FIG. 4H, FIG. 4I, FIG. 5A, FIG. 5B, and FIG. 6 except having the array substrate in FIG. 9 and FIG. 10. Accordingly, any detailed explanation will be omitted.

[0098] FIG. 12A is an image showing light transmissivity of the LCD device having an array substrate identical to the array substrate shown as FIG. 9 and FIG. 10, except that a pixel electrode does not have an outline portion. FIG. 12B is an image showing light transmissivity of the LCD device having the array substrate shown as FIG. 9 and FIG. 10.

[0099] An frame portion 375 connecting to edge portions of the slit portion 373 is removed, and a shielding electrode 360 as light-blocking metal is formed on a portion of the pixel area PA, unlike in the present example. The LCD device is substantially identical to the LCD device 100 of the present example except in the-above mentioned manner. The image in FIG. 12B is brighter than the image in FIG. 12A, and has a uniform luminance. A portion between an edge of the pixel area PA and the slit portions 373 is relatively darker than the other portion in FIG. 12A.

[0100] FIG. 13 is a graph representing response time of LCD devices shown as FIG. 12A and FIG. 12B.

[0101] A horizontal axis represents an elapsed time after applying a pixel voltage, and a vertical axis represents a light transmissivity of a pixel area PA in FIG. 13. Referring to FIG. 13, it is recognized that after 40 msec from applying a pixel voltage a light transmissivity of the LCD device described in FIG. 12A, which is represented

by the dashed line, is substantially lower than light transmissivity of the LCD device of the present example described in FIG. 12B, which is represented by the solid line, for a substantially identical time.

[0102] That is, the second and third efficiency of the liquid crystal molecules in the LCD device of the present example is remarkably improved by the outline portion 375 and the shielding electrode 360 over the LCD device described in FIG. 12A, thus the display quality of the LCD device may be improved.

[0103] It will be apparent to those skilled in the art that various modifications and variation can be made in the present invention within the scope of the appended claims

Claims

1. An array substrate (101) comprising:

a substrate (102) comprising a plurality of gate lines (111) and a plurality of data lines (115) that cross each other and that are insulated from each other, and a plurality of switching elements (108), each switching element (108) connected to one of the gate lines (111) and one of the data lines (115) ;
a plurality of pixel electrodes (170) each arranged in a pixel area (PA), each pixel electrode (170) comprising:

a first and a second frame portion (175) arranged on the substrate (102) at the edges of the corresponding pixel area (PA) along the data lines (115) and the gate lines (111) and disposed adjacent to each other in the data line direction and connected to each other in the pixel area (PA),

a plurality of connection portions (171) that extend in a direction crossing the data lines (115) and the gate lines (111), and connect to the first or second frame portions (175), the connection portions (171) dividing the corresponding pixel area (PA) into a plurality of domains, wherein the connection portion (171) extends in crossing directions inside each frame portion (175) to form an X-shape, and
a plurality of strip portions (173) that protrude from side surfaces of the connection portions (171) in each of the domains, the strip portions (173) being connected to the frame portion (175) which contains the connection portions from which the strip portions (173) protrude, wherein the strip portions (173) are parallel with the gate lines (111) at domains that contact the data lines (175), and the strip portions (173) are parallel with the data lines (115) at domains that contact the gate lines (111);
characterized in that each pixel area (PA) comprises
a shielding electrode (160) arranged along the outline of the pixel area (PA) on the data lines (115) and along the gate lines (111), and shielding the pixel electrode (170) from the data lines (115) and gate lines (111), respectively, and a passivation layer (165) is formed on the shielding electrode (160) wherein trhe first and the second frame portions (175) are arranged on the passivation layer (165).

2. The array substrate of claim 1, further comprising:

a first insulation layer (130) arranged between the data lines (115) and the shielding electrode (160);

3. The array substrate of claim 2, further comprising:

an organic insulation layer (140) arranged between the first insulation layer (130) and the shielding electrode (160).

4. The array substrate of claim 1, wherein the shielding electrode (160) comprises an optically transparent and electrically conductive material, and the width of the shielding electrode (160) is wider than that of the data lines (115) to overlap with a portion of the first and second frame portions (175).

5. The array substrate of claim 4, wherein the portion of the first frame portion (175) overlaps with a portion of the data lines (115) and the gate lines (111).

6. The array substrate of claim 1, further comprising:

a polarizer (30) disposed below the substrate (102), wherein the polarizer (30) has a polarization axis parallel with one of the diagonal directions.

Patentansprüche

1. Array-Substrat (101), umfassend
ein Substrat (102) mit einer Vielzahl von Gate-Leitungen (111) und einer Vielzahl von Datenleitungen (115), die einander kreuzen und voneinander isoliert sind, und einer Vielzahl von Schaltelementen (108), wobei jedes Schaltelement (108) mit einer der Gate-Leitungen (111) und einer der Datenleitungen (115) verbunden ist,
eine Vielzahl von Pixelelektroden (170), die jeweils in einem Pixelbereich (PA) angeordnet sind, wobei jede Pixelelektrode (170) folgendes umfasst:

einen ersten und einen zweiten Rahmenabschnitt (175), die auf dem Substrat (102) an den Rändern des entsprechenden Pixelbereichs (PA) entlang der Datenleitungen (115) und der Gate-Leitungen (111) und in Richtung der Datenleitungen einander benachbart angeordnet sowie im Pixelbereich (PA) miteinander verbunden sind,

eine Vielzahl von Verbindungsabschnitten (171), die in einer die Datenleitungen (115) und die Gate-Leitungen (111) kreuzenden Richtung verlaufen und mit dem ersten oder zweiten Rahmenabschnitt (175) in Verbindung stehen, wobei die Verbindungsabschnitte (171) den entsprechenden Pixelbereich (PA) in eine Vielzahl von Gebieten unterteilen, wobei der Verbindungsabschnitt (171) innerhalb jedes Rahmenabschnitts (175) in sich kreuzenden Richtungen verläuft, um eine X-Form zu bilden, und

eine Vielzahl von Streifenabschnitten (173), die von Seitenflächen der Verbindungsabschnitte (171) in jedem der Gebiete vorstehen, wobei die Streifenabschnitte (173) mit dem Rahmenabschnitt (175) verbunden sind, der die Verbindungsabschnitte enthält, von denen die Streifenabschnitte (173) vorstehen, wobei die Streifenabschnitte (173) in Gebieten, die mit den Datenleitungen (175) in Kontakt stehen, parallel zu den Gate-Leitungen (111) verlaufen, und in Gebieten, die mit den Gate-Leitungen (111) in Kontakt stehen, parallel zu den Datenleitungen (115) verlaufen, **dadurch gekennzeichnet, dass**

jeder Pixelbereich (PA) eine Abschirmelektrode (160) umfasst, die entlang dem Umriss des Pixelbereichs (PA) auf den Datenleitungen (115) und entlang der Gate-Leitungen (111) verläuft und die Pixelelektrode (170) gegenüber den Datenleitungen (115) und Gate-Leitungen (111) abschirmt, und

auf der Abschirmelektrode (160) eine Passivierungsschicht (165) ausgebildet ist, wobei der erste und zweite Rahmenabschnitt (175) auf der Passivierungsschicht (165) liegen.

2. Array-Substrat nach Anspruch 1, ferner umfassend eine erste Isolierschicht (130), die zwischen den Datenleitungen (115) und der Abschirmelektrode (160) angeordnet ist.

3. Array-Substrat nach Anspruch 2, ferner umfassend eine organische Isolierschicht (140), die zwischen der ersten Isolierschicht (130) und der Abschirmelektrode (160) angeordnet ist.

4. Array-Substrat nach Anspruch 1, wobei die Abschirmelektrode (160) ein optisch transparentes und elektrisch leitfähiges Material umfasst und die Breite der Abschirmelektrode (160) größer als die der Datenleitungen (115) ist, um den ersten und zweiten Rahmenabschnitt (175) teilweise zu überlappen.

5. Array-Substrat nach Anspruch 4, wobei der erste Rahmenabschnitt (175) einen Abschnitt der Datenleitungen (115) und der Gate-Leitungen (111) überlappt.

6. Array-Substrat nach Anspruch 1, ferner umfassend einen Polarisator (30), der unterhalb des Substrats (102) angeordnet ist, wobei der Polarisator (30) eine Polarisationsachse parallel zu einer der diagonalen Richtungen aufweist.

Revendications

1. Un substrat de matrice (101) comprenant :

un substrat (102) comprenant une pluralité de lignes de barrière (111) et une pluralité de lignes de données (115) qui se croisent et qui sont isolées l'une de l'autre, et une pluralité d'éléments de commutation (108), chaque élément de commutation (108) étant connecté à une des lignes de barrière (111) et une des lignes de données (115) ;

une pluralité d'électrodes de pixel (170), chacune disposée dans une zone de pixel (PA), chaque électrode de pixel (170) comprenant :

une première et une deuxième portions de cadre (175) disposées sur le substrat (102) sur les bords de la zone de pixel (PA) correspondante, le long des lignes de données (115) et des lignes de barrière (111), et disposées de façon adjacente l'une à l'autre dans le sens de la ligne de données et connectées l'une à l'autre dans la zone de pixel (PA),

une pluralité de portions de connexion (171) qui s'étend dans un sens traversant les lignes de données (115) et les lignes de barrière (111), et se connecte à la première ou la deuxième portions de cadre (175), les portions de connexion (171) divisant la zone de pixel (PA) correspondante en une pluralité de domaines, où la portion de connexion (171) s'étend dans le sens de la traversée à l'intérieur de chaque portion de cadre (175) pour former une croix, et

une pluralité de portions de bande (173) qui dépasse des surfaces latérales des portions de connexion (171) dans chacun des domaines, les portions de bande (173) étant connectées à la portion de cadre (175) qui contient les portions de connexion à partir

desquelles les portions de bande (173) dépassent, où les portions de bande (173) sont parallèles aux lignes de barrière (111) à des domaines qui font contact avec les lignes de données (175), et les portions de bande (173) sont parallèles aux lignes de données (115) aux domaines qui font contact avec les lignes de barrière (111) ;

caractérisé en ce que chaque zone de pixel (PA) comprend une électrode de protection (160) disposée le long du contour de la zone de pixel (PA) sur les lignes de données (115) et le long des lignes de barrière (111), et protégeant l'électrode de pixel (170) des lignes de données (115) et des lignes de barrière (111), respectivement,
et une couche de passivation (165) est formée sur l'électrode de protection (160), où la première et la deuxième portions de cadre (175) sont sur la couche de passivation (165).

2. Le substrat de matrice de la revendication 1, comprenant également :

une première couche d'isolation (130) disposée entre les lignes de données (115) et l'électrode de protection (160).

3. Le substrat de matrice de la revendication 2, comprenant également :une couche d'isolation organique (140) disposée entre la première couche d'isolation (130) et l'électrode de protection (160).

4. Le substrat de matrice de la revendication 1, où l'électrode de protection (160) comprend un matériau électriquement conducteur et optiquement transparent, et la largeur de l'électrode de protection (160) est plus large que celle des lignes de données (115) pour chevaucher une portion des première et deuxième portions de cadre (175).

5. Le substrat de matrice de la revendication 4, où la portion de la première portion de cadre (175) chevauche une portion des lignes de données (115) et des lignes de barrière (111).

6. Le substrat de matrice de la revendication 1, comprenant également :

un polariseur (30) disposé sous le substrat (102), où le polariseur (30) possède un axe de polarisation parallèle à un des sens en diagonal.

FIG. 1

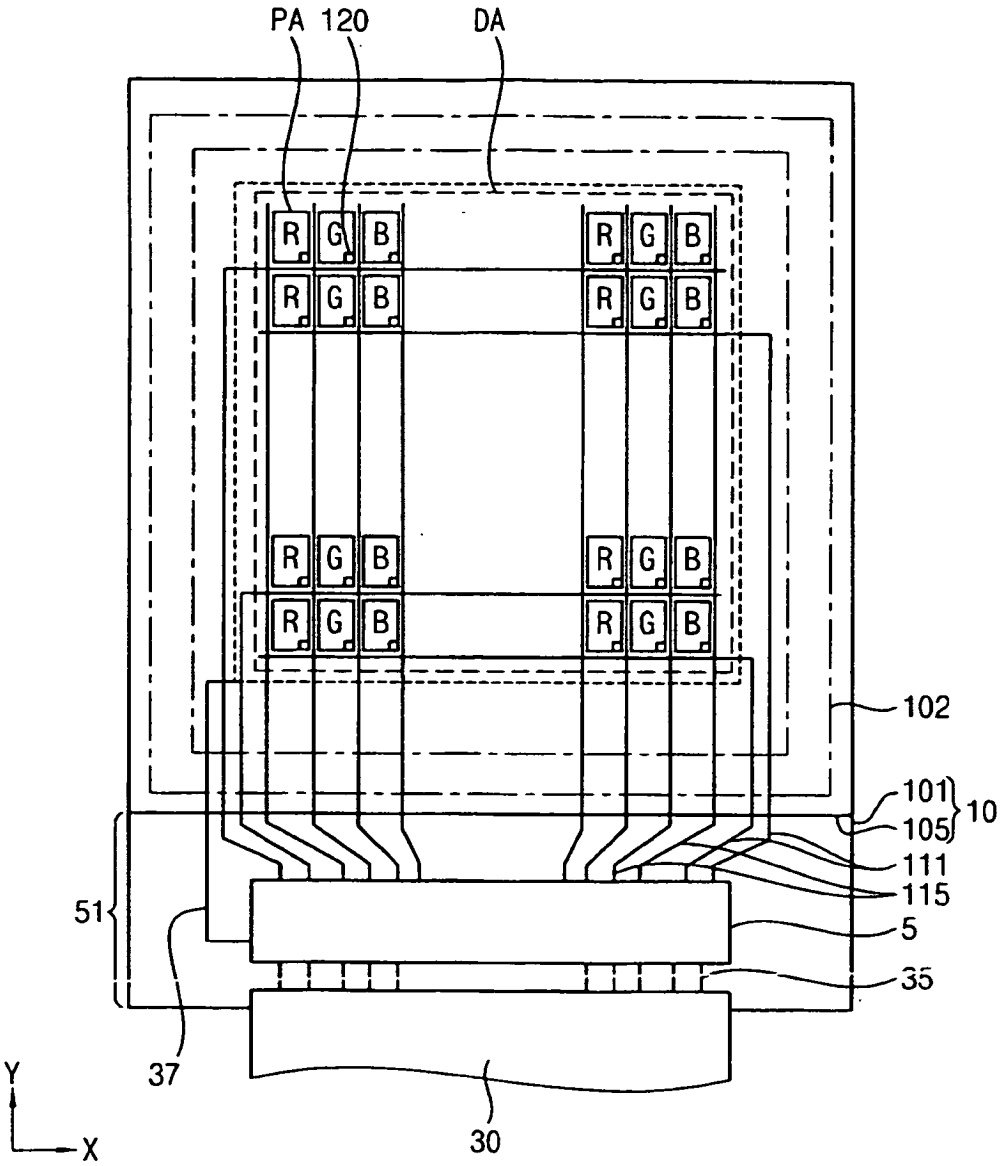


FIG. 2

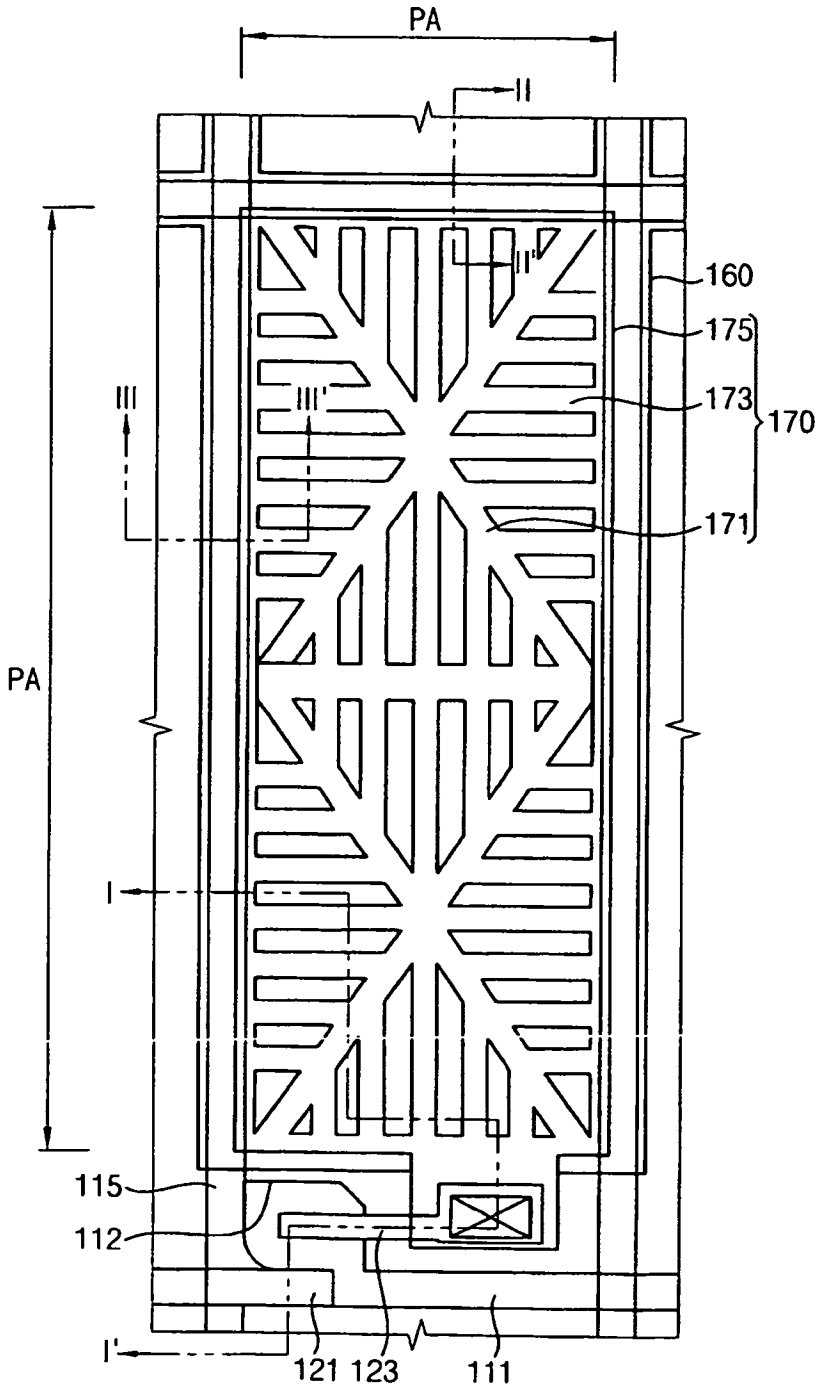


FIG. 3

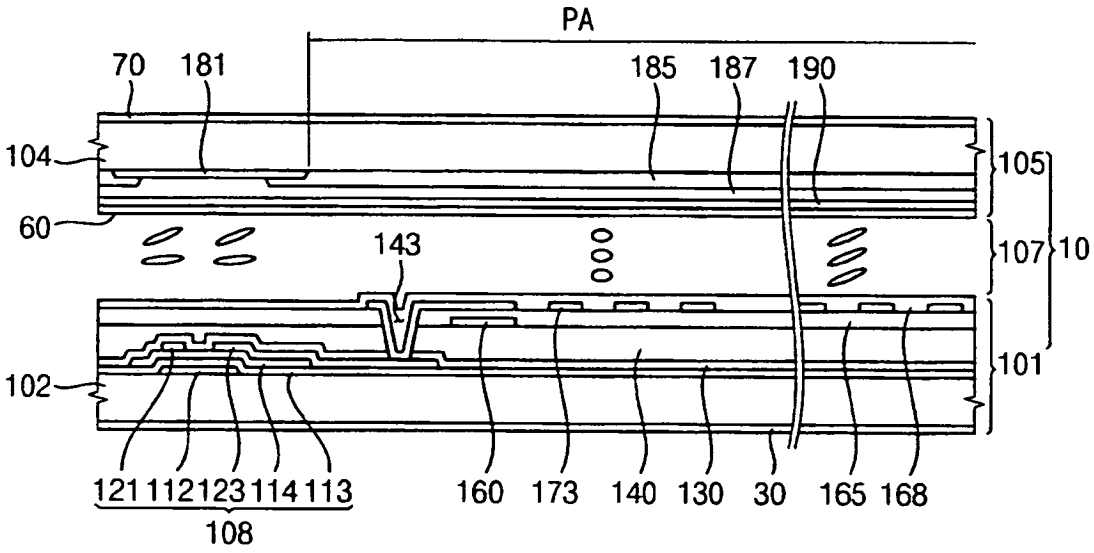

PA
70
181
185
187
190
104
105
60
143
107
10
101
102
121
112
123
114
113
108
160
173
140
130
30
165
168

FIG. 4A

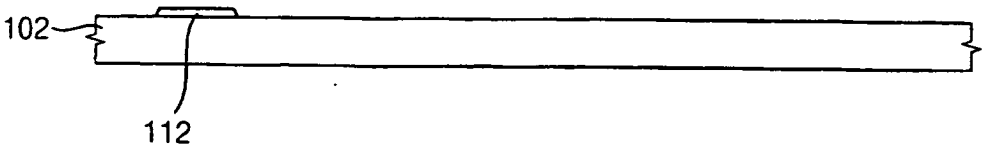

102
112

FIG. 4B

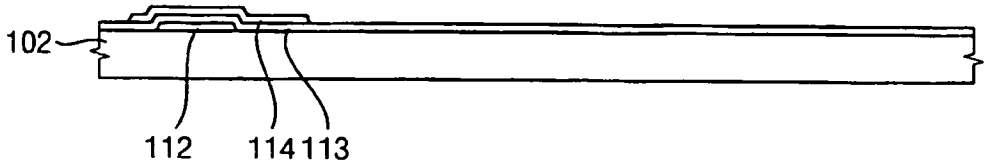


FIG. 4C

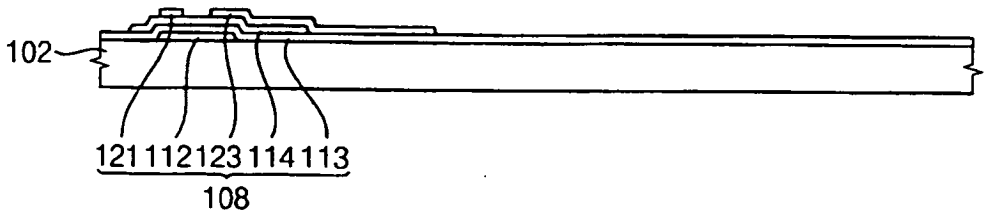


FIG. 4D

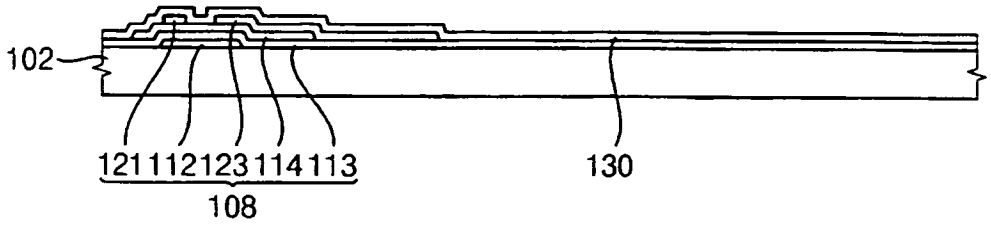

102
121 112 123 114 113
108
130

FIG. 4E

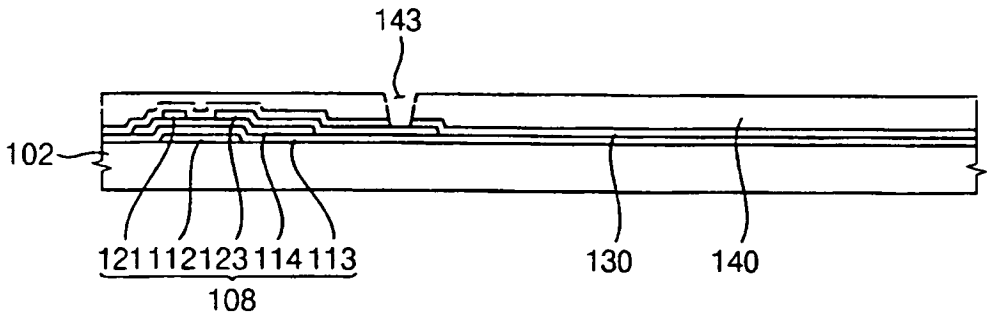

143
102
121 112 123 114 113
108
130
140

FIG. 4F

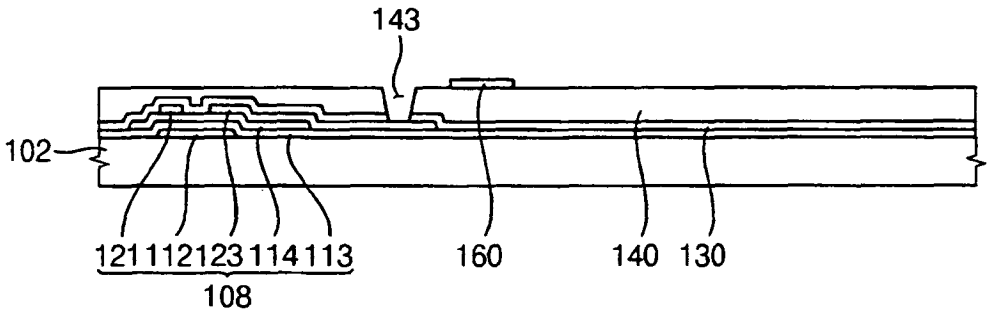

143
102
121 112 123 114 113
108
160
140
130

FIG. 4G

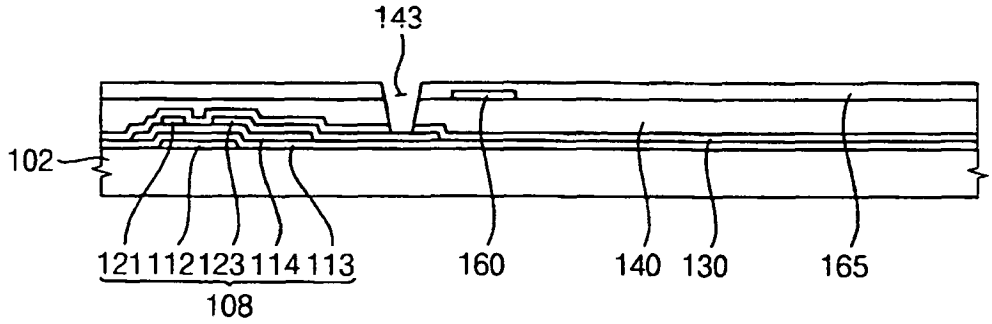

143
102
121 112 123 114 113
108
160
140
130
165

FIG. 4H

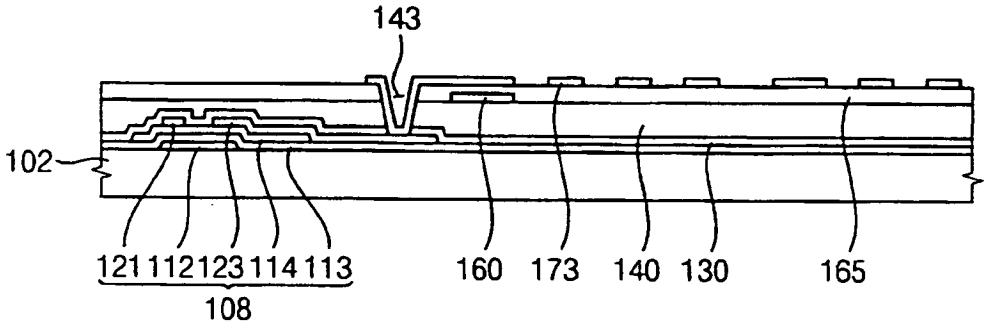

143
102
121 112 123 114 113
108
160
173
140
130
165

FIG. 4I

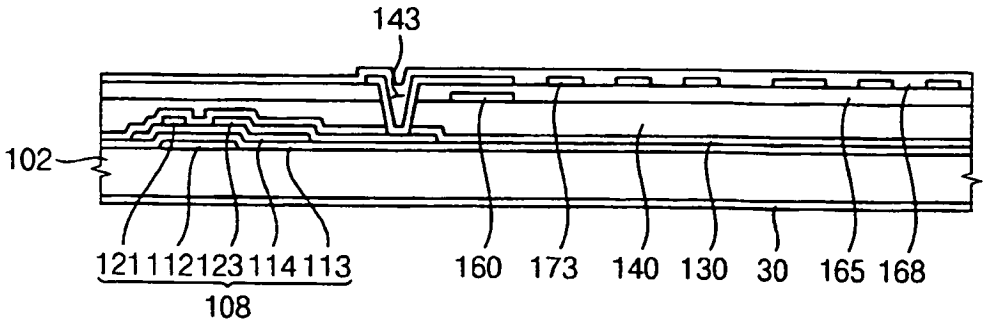

143
102
121 112 123 114 113
108
160
173
140
130
30
165
168

FIG. 5A

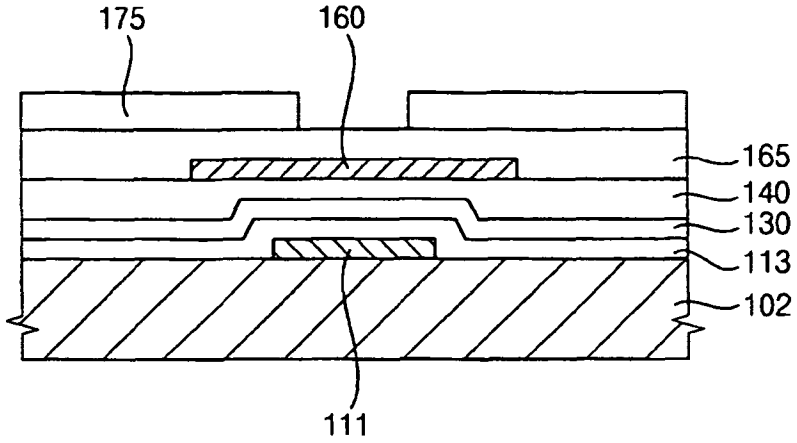


FIG. 5B

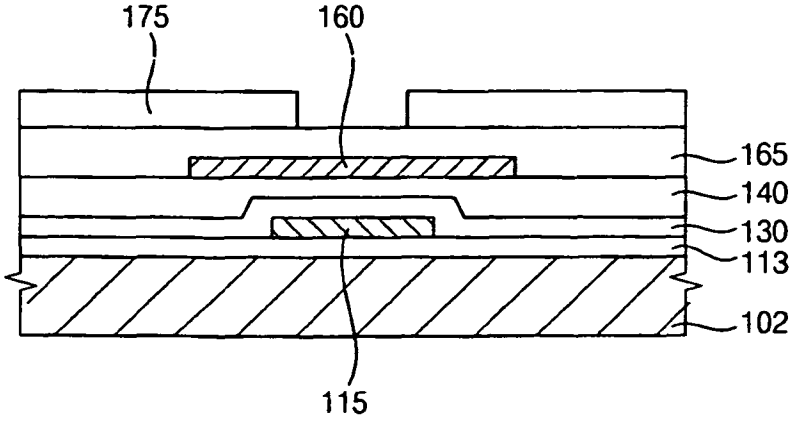


FIG. 6

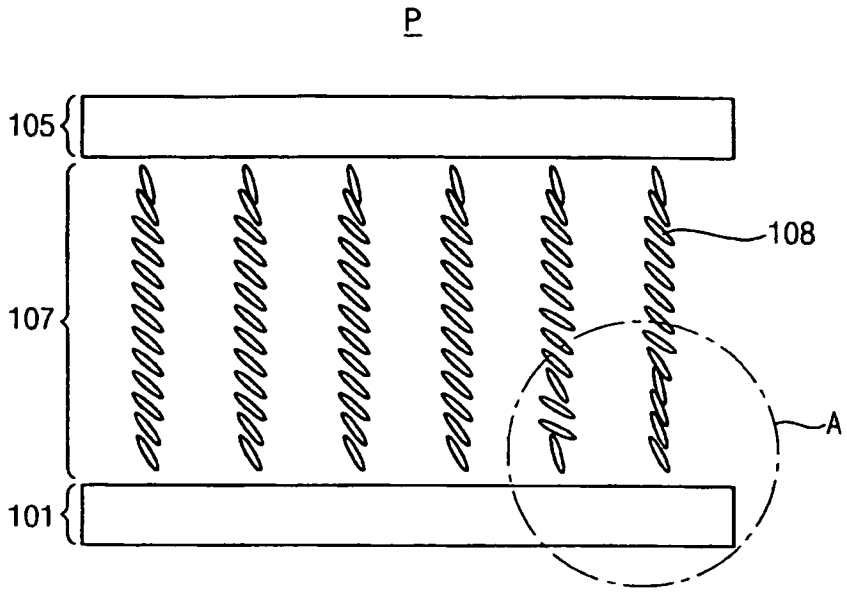


FIG. 8

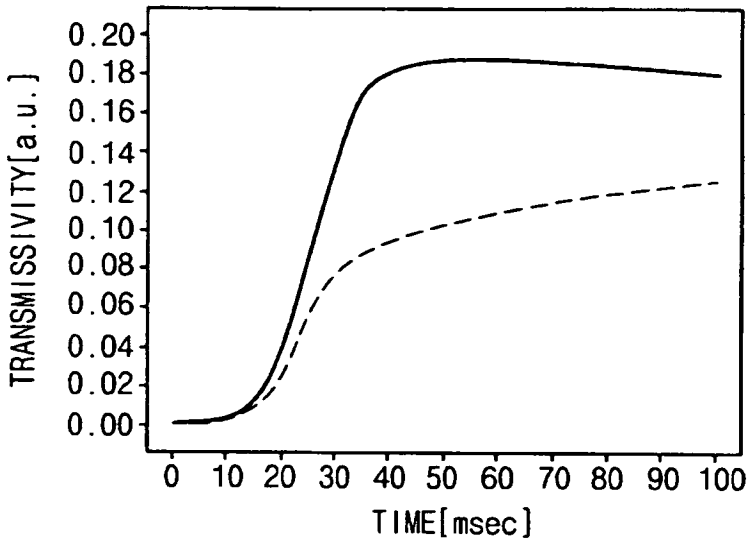

TRANSMISSIVITY[a.u.]
0.20
0.18
0.16
0.14
0.12
0.10
0.08
0.06
0.04
0.02
0.00
0 10 20 30 40 50 60 70 80 90 100
TIME[msec]

FIG. 9

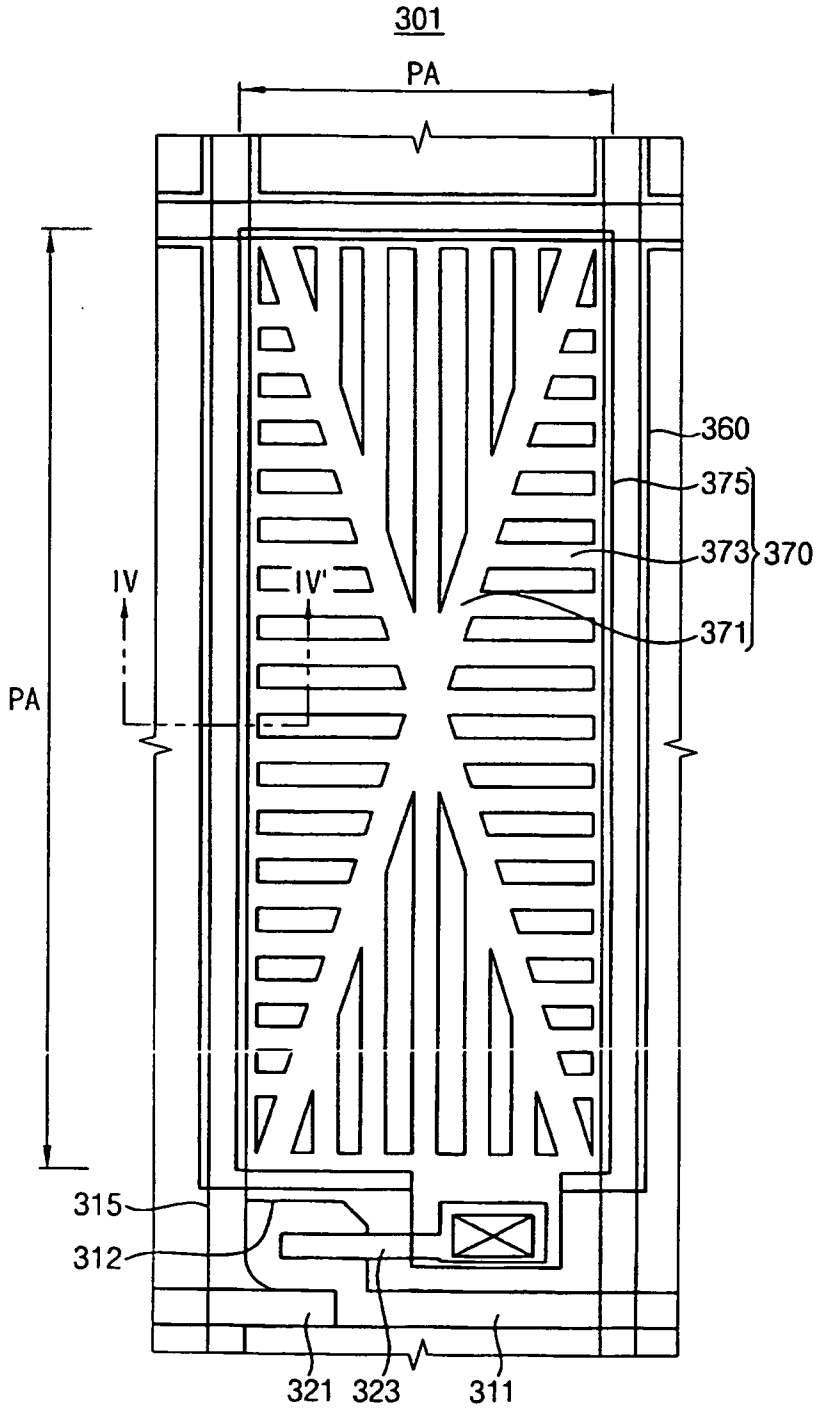


FIG. 10

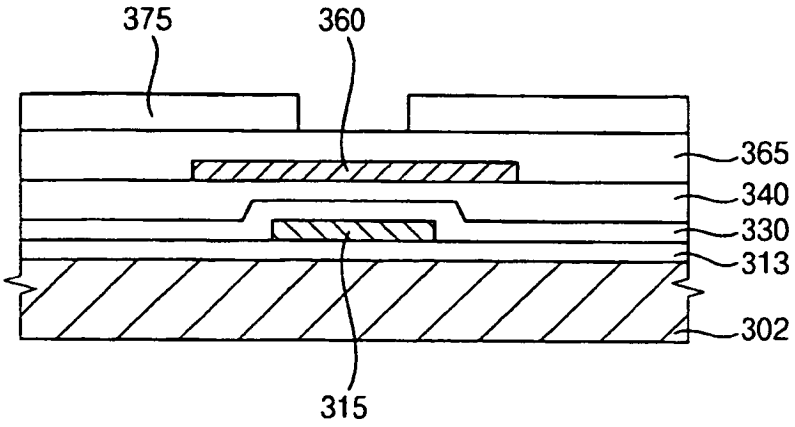


FIG. 11A

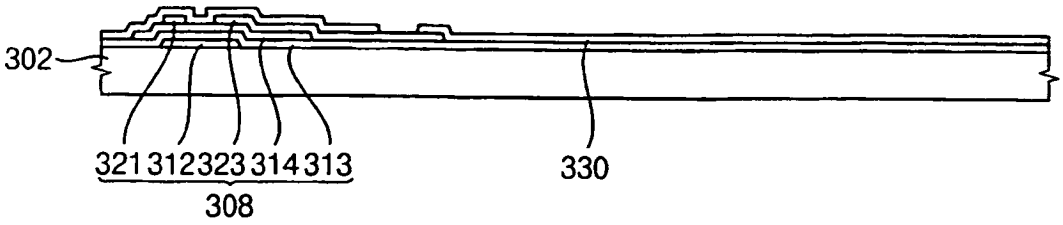


FIG. 11B

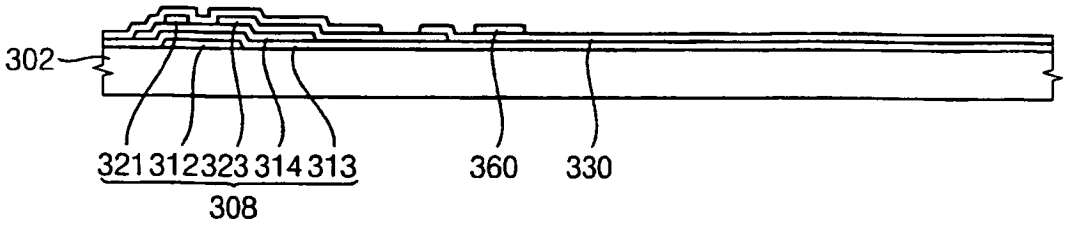


FIG. 11C

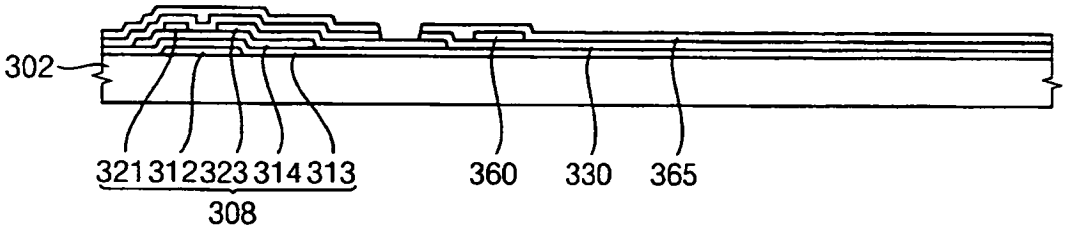
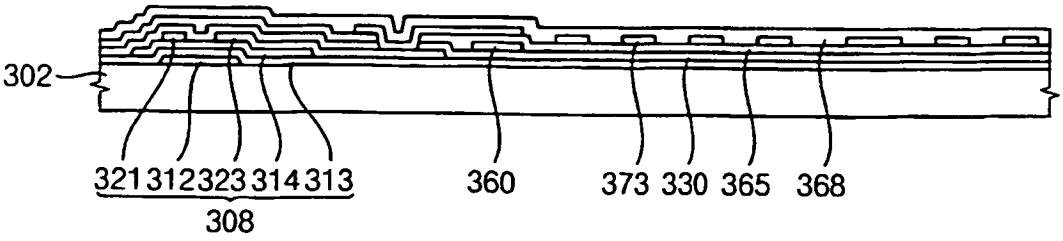


FIG. 11D



REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- US 2006061722 A **[0010]**
- US 2004100607 A **[0011]**

专利名称(译)	阵列基板，阵列基板的制造方法以及具有该阵列基板的液晶显示装置		
公开(公告)号	EP2149813B1	公开(公告)日	2012-05-02
申请号	EP2009004620	申请日	2009-03-31
[标]申请(专利权)人(译)	三星电子株式会社		
申请(专利权)人(译)	SAMSUNG ELECTRONICS CO.，LTD.		
当前申请(专利权)人(译)	三星DISPLAY CO.，LTD.		
[标]发明人	YOU HYE RAN UM YOON SUNG KIM SU JEONG LYU JAE JIN PARK SEUNG BEOM		
发明人	YOU, HYE-RAN UM, YOON-SUNG KIM, SU-JEONG LYU, JAE-JIN PARK, SEUNG-BEOM		
IPC分类号	G02F1/1333 G02F1/139		
CPC分类号	G02F1/1393 G02F1/133707 G02F2001/13606		
代理机构(译)	DR.威猛和合作伙伴		
优先权	1020080073647 2008-07-28 KR		
其他公开文献	EP2149813A1		
外部链接	Espacenet		

摘要(译)

在阵列基板中，制造阵列基板的方法，以及具有阵列基板的液晶显示（LCD）装置，像素电极（170）包括轮廓部分（175），连接部分（171），和剥离部分（173）。沿着数据线（115）和栅极线（111）布置轮廓部分（175），并且连接部分（171）在与数据线（115）和栅极线（111）交叉的方向上延伸分别连接到轮廓部分（175）。条带部分（173）从连接部分的侧面突出以连接到轮廓部分。屏蔽电极（160）沿数据线（115）和轮廓部分（175）之间的轮廓部分以及栅极线（111）和轮廓部分（175）布置。

FIG. 1