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(54) **Liquid crystal display**

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Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present invention relates to a liquid crystal display.

2. Description of the Related Art

[0002] A conventional liquid crystal display ("LCD") includes a liquid crystal capacitor connected to a gate line and charged with a data voltage, and a storage capacitor connected to the liquid crystal capacitor and maintaining the voltage of the liquid crystal capacitor. An image is displayed according to the voltage of the liquid crystal capacitor.

[0003] EP 1 241 655 A2 discloses liquid crystal display device having a liquid crystal composition sandwiched between a pair of substrates and a plurality of pixels disposed on one of the first substrates. Each of the pixels is supplied with a video signal via a switching element connected to a first electrode thereof, and is provided with a capacitance. One of two capacitance-forming electrodes forming the capacitance is connected to the first electrode of a corresponding one of the pixels, and another of the two capacitance-forming electrodes is supplied with a pixel-potential control signal.; Polarity of the video signal reverses with respect to a first reference voltage with a repetition period, and the pixel-potential control signal alternates between two voltage levels of same polarity with respect to a second reference voltage such that a voltage swing on the first electrodes of the pixels becomes larger than that of the video signal.

[0004] A LCD which displays an image not to be reversed even if a liquid crystal panel is turned around is in demand.

BRIEF SUMMARY OF THE INVENTION

[0005] The present invention has been made in an effort to solve the above-stated problem, and aspects of the present invention provide a liquid crystal display for reducing power consumption in a forward-scan mode and/or a reverse-scan mode for reducing power consumption in a forward-scan mode and/or a reverse-scan mode forward-scan mode.

[0006] In an exemplary embodiment, the present invention according to claim 1 provides a liquid crystal display which includes a liquid crystal capacitor charged with a data voltage during a first turn-on period of a first gate signal, a storage capacitor having one electrode connected to the liquid crystal capacitor, and a driving unit which supplies a boost voltage to the other electrode of the storage capacitor during a boost voltage-output period of a boost-control signal, the boost voltage includes a first edge and a second edge, the first and second edges

occur in the boost voltage-output period, and the first turn-on period occurs between the first and second edges.

[0007] In another exemplary embodiment, the present invention according to claim 1 provides a liquid crystal display which includes first to n-th gate lines, a liquid crystal capacitor connected to the i($1 \leq i \leq n$)-th gate line, a storage capacitor having one electrode connected to the liquid crystal capacitor, and a gate driver which supplies first to n-th gate signals to the first to n-th gate lines and supplies a boost voltage to the other electrode of the storage capacitor during a boost voltage-output period of a boost-control signal, each of the first to n-th gate signals having first to n-th turn-on period, respectively, the liquid crystal capacitor is charged with a data voltage during the i-th turn-on period, and the voltage of the liquid crystal capacitor is boosted up or decreased according to the boost voltage after the i-th turn-on period in the forward-scan mode in which the first to n-th turn-on period begins sequentially, or in the reverse-scan mode in which the n-th to first turn-on period begins sequentially.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] The above and/or other aspects, features, and advantages of the present invention will become more apparent from the following detailed description when taken in conjunction with the accompanying drawings, in which:

FIG. 1 is a block diagram of an exemplary embodiment of a liquid crystal display according to the present invention;

FIG. 2 is an equivalent circuit diagram of an exemplary embodiment of one pixel of the liquid crystal display according to the present invention in FIG 1; FIG. 3 is a schematic circuit diagram of an exemplary embodiment of an operation of the liquid crystal display in FIG 1;

FIGS. 4A and 4B are signal waveform timing charts of an exemplary embodiment of an operation of the liquid crystal display in FIG. 3;

FIG. 5 is a block diagram of an exemplary embodiment of the gate driver in FIG. 3, according to the present invention;

FIG. 6 is an equivalent schematic circuit diagram of an exemplary embodiment of the gate driver in FIG. 3, according to the present invention;

FIG. 7 is a signal waveform timing chart of an exemplary embodiment of an operation of the i-th stage in FIG. 6, according to the present invention;

FIG. 8 is a block diagram of a liquid crystal display; FIG. 9 is a signal waveform timing chart of an operation of the gate driver in FIG. 8;

FIG. 10 is an equivalent schematic circuit diagram of the i-th stage;

FIGS. 11A and 11B are signal waveform timing

charts illustrating an exemplary embodiment of an operation of the liquid crystal display in FIG. 8; FIG. 12 is an equivalent schematic circuit diagram of a boost voltage supplier of a liquid crystal display; FIG. 13 is an equivalent schematic circuit diagram of a boost voltage supplier of a liquid crystal display; FIG. 14 is a signal waveform timing chart illustrating another exemplary embodiment an operation of the boost voltage supplier in FIG. 13;

DETAILED DESCRIPTION OF THE INVENTION

[0009] The invention is described more fully hereinafter with reference to the accompanying drawings, in which exemplary embodiments of the invention are shown. The present invention may, however, be embodied in many different forms and should not be construed as being limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. Like reference numerals refer to like elements throughout.

[0010] It will be understood that when an element or layer is referred to as being "on", "connected to" or "coupled to" another element or layer, it can be directly on, connected or coupled to the other element or layer or intervening elements or layers may be present. In contrast, when an element is referred to as being "directly on", "directly connected to" or "directly coupled to" another element or layer, there are no intervening elements or layers present. Like numbers refer to like elements throughout. As used herein, the term "and/or" includes any and all combinations of one or more of the associated listed items.

[0011] It will be understood that, although the terms first, second, etc. may be used herein to describe various elements, components, regions, layers and/or sections, these elements, components, regions, layers and/or sections should not be limited by these terms. These terms are only used to distinguish one element, component, region, layer or section from another region, layer or section. Thus, a first element, component, region, layer or section discussed below could be termed a second element, component, region, layer or section without departing from the teachings of the present invention.

[0012] Spatially relative terms, such as "beneath", "below", "lower", "above", "upper" and the like, may be used herein for ease of description to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the figures. It will be understood that the spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. For example, if the device in the figures is turned over, elements described as "below" or "beneath" other elements or features would then be oriented "above" the other elements or features. Thus, the exemplary term "below" can encompass both an orientation of above and below.

The device may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein interpreted accordingly.

[0013] The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the invention. As used herein, the singular forms, "a", "an" and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "includes" and/or "including", when used in this specification, specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.

[0014] Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which this invention belongs. It will be further understood that terms, such as those defined in commonly used dictionaries, should be interpreted as having a meaning that is consistent with their meaning in the context of the relevant art and will not be interpreted in an idealized or overly formal sense unless expressly so defined herein.

[0015] Hereinafter, the present invention will be explained in detail with reference to the accompanying drawings.

[0016] A liquid crystal display according to an exemplary embodiment of the present invention and a driving method of the same will hereinafter be described in further detail with reference to FIGS. 1 through 7.

[0017] FIG. 1 is a block diagram of an exemplary embodiment of a liquid crystal display according to the present invention. FIG. 2 is an equivalent circuit diagram of an exemplary embodiment of one pixel of the liquid crystal display according to the present invention in FIG. 1. FIG. 3 is a schematic circuit diagram illustrating an exemplary embodiment of an operation of the liquid crystal display in FIG. 1. FIGS. 4A and 4B are signal waveform timing charts illustrating an exemplary embodiment of an operation of the liquid crystal display in FIG. 3. FIG. 5 is a block diagram of an exemplary embodiment of a gate driver in FIG. 3. FIG. 6 is an equivalent schematic circuit diagram of an exemplary embodiment of the gate driver in FIG. 3. FIG. 7 is a signal waveform timing chart illustrating an exemplary embodiment of an operation of the i-th stage in FIG. 6.

[0018] Referring to FIG. 1, an exemplary embodiment of an LCD 10 according to the present invention comprises a liquid crystal panel 300, a timing controller 500, a clock generator 600, a gate driver 400 and a data driver 700.

[0019] The liquid crystal panel 300 is divided into a display area DA, where an image is displayed, and a non-display area PA, where an image is not displayed.

[0020] The display area DA includes a first substrate 100, which includes a plurality of gate lines G1 to Gn, a

plurality of data lines D1 to Dm, a plurality of storage lines S1 to Sn, a pixel-switching element Qp (see FIG. 2) and pixel electrodes PE formed thereon, a second substrate 200, which includes color filters CF and a common electrode CE formed thereon and a liquid crystal layer 150 interposed between the first substrate 100 and the second substrate 200, such that an image is displayed within the display area DA. The gate lines G1 to Gn and the storage lines S1 to Sn extend in a first direction i.e., a row direction, so as to be substantially in parallel with one another, and the data lines D1 to Dm extend in a second direction, i.e., a column direction, so as to be substantially in parallel with one another. In exemplary embodiments of the present invention, the first direction is substantially perpendicular to the second direction.

[0021] Referring to FIG. 2, in exemplary embodiments, a pixel PX includes a color filter CF which may be formed on an area of the common electrode CE of the second substrate 200, such that the color filter CF is disposed to face the pixel electrode PE of the first substrate 100. In an exemplary embodiment, the pixel PX, which is connected to an i-th gate line Gi (i = 1 to n) and to a j-th data line Dj (j = 1 to m), includes the pixel-switching element Qp, which is connected to a signal line Gi, Dj, and the liquid crystal capacitor Clc and a storage capacitor Cst which are connected to the pixel-switching element Qp. In alternative exemplary embodiments, the pixel-switching element Qp may be a thin film transistor ("a-Si TFT") made from amorphous silicon. Specifically, one electrode of the storage capacitor Cst is connected to the liquid crystal capacitor Clc, the other electrode of the storage capacitor Cst is connected to the storage line Si.

[0022] As shown in FIG. 2, according to an exemplary embodiment, the first substrate 100 is larger in size than the second substrate 200, such that the non-display area PA does not display an image.

[0023] The timing controller 500 receives input RGB image signals and an input-control signal, which controls display of an image, from a graphics controller (not shown), and supplies an image signal DAT and a data control signal CONT1 to the data driver 700. In the current exemplary embodiment, the timing controller 500 receives the input control signal which includes, for example, a horizontal sync signal Hsync, a main clock signal Mclk and a data enable signal DE, and the timing controller 500 supplies the data control signal CONT1 to the data driver 700. In the current exemplary embodiment, the data control signal CONT1 controls an operation of the data driver 700, and includes, for example, a horizontal start signal which starts an operation of data driver 700 and a load signal which instructs an output of two data voltages. However, the present invention is not limited thereto, and may vary as necessary.

[0024] The data driver 700 receives the image signal DAT and the data control signal CONT1, and the data driver 700 supplies an image data voltage corresponding to the image signal DAT to the lines D1 to Dm. In the current exemplary embodiment, the data driver 700 is an

integrated circuit ("IC"), and is connected to the liquid crystal panel 300 in a tape carrier package ("TCP") manner, however, the present invention is not limited thereto, and may vary as necessary. In another exemplary embodiment, the data driver 700 may be formed on the non-display area PA of the liquid crystal panel 300.

[0025] Furthermore, the timing controller 500 supplies a clock-generation-control signal CONT2 to the clock generator 600, and supplies a scan-start signal STV and scan-direction-control signals DIR, DIRB to the gate driver 400. The clock-generation-control signal CONT2 includes a gate clock signal (not shown) which determines a timing when the gate on voltage Von is output, an output enable signal (not shown) which determines the pulse width of the gate-on voltage Von, for example, but is not limited thereto, and may vary as necessary.

[0026] The scan-direction-control signals DIR, DIRB may control sequence of a turn-on period when the gate-on voltage Von is applied to each of the gate lines G1~Gn. For example, when a first scan-direction-control signal DIR is at a high level and a second scan-direction-control signal DIRB is at a low level ("forward-scan mode"), a first turn-on period of the first gate line G1 begins first, a second turn-on period of the second gate line G2 follows the first turn-on period, and third to n-th turn-on periods of the third to n-th gate lines G3~Gn begin sequentially. When a first scan-direction-control signal DIR is at a low level and a second scan-direction-control signal DIRB is at a high level ("reverse-scan mode"), an n-th turn-on period of the n-th gate line Gn begins first, a (n-1)th turn-on period of the (n-1)th gate line G(n-1) follows the n-th turn-on period, and (n-2)th to first turn-on periods of the (n-2) to first gate lines G(n-2)~G1 begin sequentially.

[0027] The clock generator 600 receives the clock-generation-control signal CONT2, and outputs the clock signal CKV and the clock bar signal CKVB which swings between the gate-on voltage Von and the gate-off voltage Voff. In the current exemplary embodiment, the clock signal CKV is an inverse-phase signal of the clock bar signal CKVB.

[0028] The gate driver 400 receives scan-start signal STV, scan-direction-control signals DIR, DIRB, the clock signal CKV and the clock bar signal CKVB and the gate-off voltage Voff, and supplies the gate signals to the gate lines G1~Gn, respectively. Furthermore, the gate driver 400 supplies a boost voltage Vboost to the storage lines S1~Sn sequentially. The gate driver 400 will be described later in more detail with reference to FIGS. 5 through 7.

[0029] The operation of the liquid crystal display 10 will now be described in more detail with reference to FIGS. 3 and 4A.

[0030] Referring to FIG. 3, the liquid crystal display 10 includes (i-1)th to (i+1)th gate lines G(i-1)~G(i+1), (i-1)th to (i+1)th storage lines S(i-1)~S(i+1) and pixels connected to the gate lines G(i-1)~G(i+1) and the storage lines S(i-1)~S(i+1). Each of the pixels includes the liquid crystal capacitor Clc and the storage capacitor Cst. One electrode of the liquid crystal capacitor Clc is connected to

the pixel-switching element Qp, and the other electrode of the liquid crystal capacitor Clc receives a common voltage Vcom. One electrode of the storage capacitor Cst is connected to the liquid crystal capacitor Clc, and the other electrode of the storage capacitor Cst is connected to the storage line Si. A boost-switching element Qb applies the boost voltage to the storage line Si in response to boost-control signal CONT3(i).

[0031] The operation of liquid crystal display 10 in a forward-scan mode will now be described in more detail with reference to FIGS. 3 and 4A.

[0032] First, the (i-1)th gate signal Gout(i-1) having the (i-1)th turn-on period Pon(i-1) is supplied to the (i-1)th gate line G(i-1). Then, the i-th gate signal Gout(i) having the i-th turn-on period Pon(i) is supplied to the i-th gate line G(i). The (i+1)th gate signal Gout(i+1) having the (i+1)th turn-on period Pon(i+1) is supplied to the (i+1)th gate line G(i+1). That is, the (i-1)th to (i+1)th turn-on period Pon(i-1)~Pon(i+1) begins sequentially. According to an exemplary embodiment, the turn-on period Pon(i-1)~Pon(i+1) is 1 horizontal period 1H. During each of the turn-on periods Pon(i-1)~Pon(i+1), the liquid crystal capacitor Clc is charged with the data voltage.

[0033] The boost voltage Vboost swings between the high level and the low level, and includes edges E1, E2. The edges E1, E2 are a rising edge or a falling edge, respectively.

[0034] The i-th boost-control signal CONT3(i) includes a boost voltage-output period Pb. For example, the i-th boost-control signal CONT3(i) may be at the high level during the boost voltage-output period. The boost-switching element Qb is turned on during the boost voltage-output period Pb, and supplies the boost voltage Vboost to the storage line Si. Here, the boost voltage Vboost which is transmitted to the storage line Si is referred to as a boost voltage Sout(i). Therefore, the boost voltage Sout(i) of the storage line Si is as shown in FIG. 4A. According to the current exemplary embodiment, the first and second edges E1, E2 occur in the boost voltage-output period Pb, the i-th turn-on period Pon(i) occurs between the first and second edges E1, E2. That is, the boost voltage-output period Pb overlaps with the first edge E1, the i-th turn-on period Pon(i) and the second edge E2.

[0035] The voltage V_Clc of the liquid crystal capacitor Clc is described as follows. When the i-th turn-on period Pon(i) begins, the pixel-switching element Qp is turned on, and then the liquid crystal capacitor Clc is charged with a data voltage Vdat. In the current exemplary embodiment, the data voltage Vdat may be negative with respect to the common voltage Vcom.

[0036] Next, the pixel-switching element Qp is turned off after the i-th turn-on period Pon(i), the second edge E2 of the boost voltage Vboost is applied to the other of the storage capacitor Cst. When the falling edge E2 is applied to the other of the storage capacitor Cst, the voltage of the storage capacitor Cst is lowered, and the voltage of the liquid crystal capacitor Clc connected to the

storage capacitor Cst is lowered. For example, the capacitance of the storage capacitor Cst and the capacitance of the liquid crystal capacitor Clc are same, the voltage of the liquid crystal capacitor Clc is lowered by Vboost/2 at the falling edge E2.

[0037] That is, the voltage of the liquid crystal capacitor Clc is decreased by the second edge E2, which is applied to the other of the storage capacitor Cst after the i-th turn-on period Pon(i) so that the difference between the boosted voltage of the liquid crystal capacitor Clc and the common voltage Vcom becomes large. The difference between the boosted voltage of the liquid crystal capacitor Clc and the common voltage Vcom becomes larger than that of between the data voltage Vdat and the common voltage Vcom, and thus, power consumption is reduced.

[0038] The operation of liquid crystal display 10 in a reverse-scan mode is described in more detail in the following with reference to FIGS. 3 and 4B.

[0039] First, the (i+1)th gate signal Gout(i+1) having the (i+1)th turn-on period Pon(i+1) is supplied to the (i+1)th gate line G(i+1). Then, the i-th gate signal Gout(i) having the i-th turn-on period Pon(i) is supplied to the i-th gate line G(i). Next, the (i-1)th gate signal Gout(i-1) having the (i-1)th turn-on period Pon(i-1) is supplied to the (i-1)th gate line G(i-1). That is, the (i+1)th to (i-1)th turn-on period Pon(i+1)~Pon(i-1) begins sequentially.

[0040] According to an exemplary embodiment, the boost voltage Vboost comprises edges E1, E2.

[0041] The i-th boost-control signal CONT3(i) comprises a boost voltage-output period Pb. The first and second edges E1, E2 occur in the boost voltage-output period Pb, the i-th turn-on period Pon(i) occurs between the first and second edges E1, E2. That is, the boost voltage-output period Pb overlaps with the first edge E1, the i-th turn-on period Pon(i) and the second edge.

[0042] The voltage V_Clc of the liquid crystal capacitor Clc is described in the following. When the i-th turn-on period Pon(i) initiates, the pixel-switching element Qp is turned on, and then the liquid crystal capacitor Clc is charged with a data voltage Vdat. In the current exemplary embodiment, the data voltage Vdat may be negative with respect to the common voltage Vcom.

[0043] Next, the pixel-switching element Qp is turned off after the i-th turn-on period Pon(i), the first edge E1 of the boost voltage Vboost is applied to the other of the storage capacitor Cst. When the falling edge E1 is applied to the other of the storage capacitor Cst, the voltage of the storage capacitor Cst is lowered, and the voltage of the liquid crystal capacitor Clc connected to the storage capacitor Cst is lowered. For example, the capacitance of the storage capacitor Cst and the capacitance of the liquid crystal capacitor Clc are same, the voltage of the liquid crystal capacitor Clc is lowered by Vboost/2 at the falling edge E2.

[0044] Referring to FIGS. 4A, 4B, the boost voltage Vboost comprises the first edge E1 and the second edge E2 and the edges E1, E2 occur in the boost voltage-output period Pb so that the voltage V_Clc of the liquid

crystal capacitor C_{lc} is decreased or amplified in the forward-scan mode and/or in the reverse-scan mode. In the current exemplary embodiment, the boost voltage-output period P_b may overlap the $(i-1)$ th to $(i+1)$ th turn-on period $P_{on(i-1)} \sim P_{on(i+1)}$.

[0045] The gate driver 400 is described below in more detail, where the gate driver 400 operates in the forward-scan mode is described.

[0046] Referring to FIGS. 1 and 5, the gate driver 400 includes a plurality of stages ST_1 to ST_{n+1} , which are connected to one another in a cascade manner. Each of the stages ST_1 to ST_n , except for the last stage ST_{n+1} , is connected to a respective corresponding gate line of the plurality of gate lines G_1 to G_n and the storage line $S(i)$, and the stages ST_1 to ST_n output gate signals $G_{out}(1)$ to $G_{out}(n)$ and the boost voltage $S_{out}(1)$ to $S_{out}(n)$ during the boost voltage-output period P_b , respectively. Each of the stages ST_1 to ST_{n+1} receives the boost voltage V_{boost} , the gate-off voltage V_{off} , the clock signal CKV , the clock bar signal $CKVB$ and the scan-direction-control signals DIR , $DIRB$. Each of the stages ST_1 to ST_{n+1} includes a first scan-direction terminal D_1 , a second scan-direction terminal D_2 , a first clock terminal CK_1 , a second clock terminal CK_2 , a set terminal S , a reset terminal R , a power-supply-voltage terminal G , a boost voltage terminal B , a gate-output terminal OUT_1 and a storage-output terminal OUT_2 .

[0047] Among the stages ST_1 to ST_{n+1} , a i -th ($i \neq 1$) stage ST_i , for example, includes a set terminal S to which a gate signal $G_{out}(i-1)$ of a previous stage $ST_{(i-1)}$ is input, a reset terminal R to which a gate signal $G_{out}(i+1)$ of a next stage $ST_{(i+1)}$ is input, a first clock terminal CK_1 and a second clock terminal CK_2 to which the first clock signal CKV and the clock bar signal $CKVB$ are input, respectively, the power-supply voltage terminal G to which the gate-off voltage V_{off} is input, the first and second scan-direction terminals D_1 and D_2 to which the scan-direction-control signals DIR , $DIRB$ are input, respectively, and the boost voltage terminal B to which the boost voltage V_{boost} is input. The first scan-direction-control signal DIR is at high level and the second scan-direction-control signal $DIRB$ is at a low level. The i -th stage ST_i includes a gate-output terminal OUT_1 through which a i -th gate signal $G_{out}(i)$ is output, and a storage-output terminal OUT_2 through which the boost voltage $S_{out}(i)$ of the boost voltage-output period P_b is output.

[0048] According to an exemplary embodiment, the scan-start signal STV is input to the set terminal S of the first stage ST_1 .

[0049] A gate signal $G_{out}(n+1)$ of the last stage $ST_{(n+1)}$ is input to a reset terminal R of the n -th stage ST_n . The scan-start signal STV is input to a reset terminal R of the last stage $ST_{(n+1)}$.

[0050] While, in the reverse-scan mode, the scan-start signal STV may be input to the reset terminal R of the $(n+1)$ th stage $ST_{(n+1)}$, and the first scan-direction-control signal DIR may be at a low level and the second scan-direction-control signal $DIRB$ may be at high level.

[0051] The i -th stage ST_i is described in the following in more detail with reference to FIGS. 6 and 7.

[0052] Referring to FIG. 6, the i -th stage ST_i includes a gate signal supplier 410 and a boost voltage supplier 460. The gate signal supplier 410 outputs the i -th gate signal $G_{out}(i)$ to the i -th gate lines G_i , and the boost voltage supplier 460 outputs the boost voltage $S_{out}(i)$ to the i -th storage line S_i during the boost voltage-output period P_b .

[0053] According to an exemplary embodiment, the gate signal supplier 410 includes a pull-up-control unit 420, a pull-up unit 430, a pull-down unit 440, and a holding unit 450. In the forward-scan mode, the first scan-direction-control signal DIR is at high level and the second scan-direction-control signal $DIRB$ is at a low level.

[0054] The pull-up-control unit 420 comprises transistors T_2 , and T_3 . The gate of the transistor T_2 receives the $(i-1)$ th gate signal $G_{out}(i-1)$, and the transistor T_2 outputs the first scan-direction-control signal DIR to a first node N_1 in response to the $(i-1)$ th gate signal $G_{out}(i-1)$. The gate of the transistor T_3 receives the $(i+1)$ th gate signal $G_{out}(i+1)$, and the transistor T_3 outputs the second scan-direction-control signal $DIRB$ to the first node N_1 in response to the $(i+1)$ th gate signal $G_{out}(i+1)$.

[0055] The pull-up unit 430 comprises transistor T_1 and a capacitor C_1 which connect the gate and the source of the transistor T_1 . The gate of the transistor T_1 is connected to the first node N_1 , the drain of the transistor T_1 receives the clock signal CKV .

[0056] The pull-down unit 440 comprises a transistor T_6 , the drain of the transistor T_6 is connected to the source of the transistor T_1 . The source of the transistor T_6 receives the gate-off voltage V_{off} , and the gate of the transistor T_6 receives the clock bar signal $CKVB$.

[0057] The holding unit 450 includes transistors T_4 , T_5 , and T_7 . The gate of the transistor T_4 is connected to a second node N_2 , the drain of the transistor T_4 is connected to the first node N_1 , and the source of the transistor T_4 is connected to the gate-off voltage V_{off} . The gate of the transistor T_5 is connected to the second node N_2 , the drain of the transistor T_5 is connected to the source of the transistor T_1 , and the source of the transistor T_5 is connected to the gate-off voltage V_{off} . The gate of the transistor T_7 is connected to the first node N_1 , the drain of the transistor T_7 is connected to the second node N_2 , and the source of the transistor T_7 is connected to the gate-off voltage V_{off} . According to an exemplary embodiment, the transistors T_1 through T_7 are a-Si TFTs.

[0058] First, an operation in which the i -th gate signal $G_{out}(i)$ transitions to the gate-on voltage V_{on} from the gate-off voltage V_{off} is described in the following below.

[0059] During the $(i-1)$ th turn-on period $P_{on}(i-1)$, the transistor T_2 of the pull-up-control unit 420 receives the $(i-1)$ th gate signal $G_{out}(i-1)$ and the transistor T_2 is turned on. The transistor T_2 outputs the first scan-direction-control signal DIR to the first node N_1 . That is, the capacitor C_1 of the pull-up unit 430 is charged during the $(i-1)$ th

turn-on period $Pon(i-1)$.

[0060] After the capacitor C1 of the pull-up unit 430 is charged, the transistor T1 is turned on and outputs the clock signal CKV as the i -th gate signal Gout(i) during the i -th turn-on period $Pon(i)$

[0061] Next, an operation in which the i -th gate signal Gout(i) is held at the high level is described in the following.

[0062] When the i -th gate signal Gout(i) is at high level, the transistor T7 of the holding unit 450 is turned on, and supplies the gate-off voltage Voff to the gates of the transistors T4 and T5. The transistor T4 is turned off and does not turn off the transistor T1. Also, the transistor T5 is turned off and does not pull down the i -th gate signal Gout(i). That is, the holding unit 450 holds the i -th gate signal Gout(i) at high level during the i -th turn-on period $Pon(i)$.

[0063] Next, an operation in which the i -th gate signal Gout(i) transitions to the gate-off voltage Voff from the gate-on voltage Von is described in the following.

[0064] During the $(i+1)$ th turn-on period $Pon(i+1)$, the transistor T6 of the pull-down unit 440 receives the clock bar signal CLKB and is turned on. The transistor T6 pulls down the i -th gate signal Gout(i) to the gate-off voltage Voff.

[0065] According to the current exemplary embodiment, the transistor T3 of the pull-up-control unit 420 receives the $(i+1)$ th gate signal Gout($i+1$), transistor T3 is turned on, and transistor T3 supplies the second scan-direction-control signal DIRB to the first node N1. Therefore, the level of the first node N1 is decreased to the low level, and the transistor T1 of the pull-up unit 430 is turned off.

[0066] Next, an operation in which the i -th gate signal Gout(i) is held at the low level is described in the following below.

[0067] When the voltage of the first node N1 is at a low level, the transistor T7 of the holding unit 450 is turned off and does not supply the gate-off voltage Voff to the second node N2. Thus, the voltage of the second node N2 varies according to the clock signal CKV. For example, when the clock signal CKV is at the high level, the second node N2 is at high level and the transistors T4 and T5 are turned on. The transistor T4 supplies the gate-off voltage Voff to first node N1 so that the transistor T1 of the pull-up unit 430 is turned off and the first capacitor C1 is discharged. Also, the transistor T5 holds the i -th gate signal Gout(i) to the gate-off voltage Voff.

[0068] That is, the gate driver 400, as shown in FIG. 7, outputs the clock signal CKV as the $(i-2)$ th gate signal Gout($i-2$) during the $(i-2)$ th turn-on period $Pon(i-2)$ and outputs the clock bar signal CKVB as the $(i-1)$ th gate signal Gout($i-1$) during the $(i-1)$ th turn-on period $Pon(i-1)$ and outputs the clock signal CKV as the i -th gate signal Gout(i) during the i -th turn-on period $Pon(i)$, and outputs the clock bar signal CKVB as the $(i+1)$ th gate signal Gout($i+1$) during the $(i+1)$ th turn-on period $Pon(i+1)$, and outputs the clock signal CKV as the $(i+2)$ th gate signal Gout

($i+2$) during the $(i+2)$ th turn-on period $Pon(i+2)$.

[0069] Next, the boost voltage supplier 460 is described below in more detail.

[0070] According to an exemplary embodiment, the boost voltage supplier 460 includes a first switching element 470, a second switching element 480 and a switching unit 490. The first switching element 470 is a diode-connected transistor T8. The second switching element 480 is a diode-connected transistor T9. The switching unit 490 includes transistors T10 and T11. According to the current exemplary embodiment, the transistors T8 through T11 are a-Si TFTs.

[0071] During the $(i-2)$ th turn-on period $Pon(i-2)$, the transistor T10 of the switching unit 490 is turned on and supplies the ground voltage to a third node N3. Thus, the i -th boost-control signal CONT3(i) is at low level during the $(i-2)$ th turn-on period $Pon(i-2)$. At this time, the transistors T8, T9, and T11 are turned off.

[0072] During the $(i-1)$ th turn-on period $Pon(i-1)$, the diode-connected transistor T8 supplies $(i-1)$ th gate signal Gout($i-1$) to the third node N3. Thus, the i -th boost-control signal CONT3(i) is at high level during the $(i-1)$ th turn-on period $Pon(i-1)$. At this time, the transistors T9, T10, and T11 are turned off.

[0073] During $(i+1)$ th turn-on period $Pon(i+1)$, the diode-connected transistor T9 supplies the $(i+1)$ th gate signal Gout($i+1$) to the third node N3. Thus, the i -th boost-control signal CONT3(i) is at high level during the $(i+1)$ th turn-on period $Pon(i+1)$. At this time, the transistors T8, T10, and T11 are turned off.

[0074] During the $(i+2)$ -th turn-on period $Pon(i+2)$, the transistor T11 of the switching unit 490 is turned on and supplies the ground voltage to the third node N3. Thus, the i -th boost-control signal CONT3(i) is at low level during the $(i+2)$ th turn-on period $Pon(i+2)$. At this time, the transistors T8, T9, and T10 are turned off.

[0075] That is, the i -th boost-control signal CONT3(i) is at high level during the boost voltage-output period Pb as shown in the FIGS. 4A, 4B, and 7. In the above exemplary embodiments, the switching unit 490 includes two transistors T10 and T11, and each transistor operates in response to the $(i-2)$ th gate signal Gout($i-2$) or the $(i+2)$ th gate signal Gout($i+2$). However, the present invention is not limited thereto. For example, the switching unit 490 may include at least one transistor and supply the ground voltage during the period except for the $(i-1)$ th turn-on period $Pon(i-1)$ and the $(i+1)$ th turn-on period $Pon(i+1)$.

[0076] An LCD and a method of driving the same is described hereinafter in further detail with reference to FIGS. 8 through 11B.

[0077] FIG. 8 is a block diagram of a liquid crystal display. FIG. 9 is a signal waveform timing chart illustrating an exemplary embodiment of an operation of the gate driver in FIG 8. FIG. 10 is an equivalent schematic circuit diagram of an exemplary embodiment of the i -th stage. FIGS. 11A and 11B are signal waveform timing charts illustrating an exemplary embodiment of an operation of

the liquid crystal display in FIG 8.

[0078] Referring to FIG. 8, the LCD 11 includes an LCD panel 300, a timing controller 501, the first and the second clock generators 600a, and 600b, the first and second gate drivers 400a and 400b, and a data driver 700.

[0079] Each of the gate drivers 400a, 400b output the gate signals to a plurality of gate lines G1~G2n. For example, the first gate driver 400a is connected to odd-numbered gate lines G1~G(2n-1) among the gate lines G1~G2n and odd-numbered storage lines S1~S(2n-1) among the storage lines S1~S2n, and the second gate driver 402 is connected to even-numbered gate lines G2~G2n and even-numbered storage lines S2~S2n. According to an exemplary embodiment, the first and second drivers may not be apart from each other physically.

[0080] In more detail, the timing controller 501 supplies the first clock-generation-control signal CONT2a to the first clock generator 600a, and supplies the second clock-generation-control signal CONT2b to the second clock generator 600b. Also, the timing controller 501 supplies the first scan-start signal STV_L to the first gate driver 400a, and supplies the second scan-start signal STV_R to the second gate driver 400b. According to the current exemplary embodiment, the first scan start signal STV_L and the second scan start signal STV_R have a predetermined phase difference.

[0081] The first clock generator 600a receives the first clock-generation-control signal CONT2a, generates the first clock signal CKV_L and the first clock bar signal CKVB_L, and supplies the first clock signal CKV_L and the first clock bar signal CKVB_L to the first gate driver 400a. The second clock generator 600b receives the second clock-generation-control signal CONT2b, generates the second clock signal CKV_R, the second clock bar signal CKVB_R, and supplies the second clock signal CKV_R, the second clock bar signal CKVB_R to the second gate driver 400b. According to the current exemplary embodiment, the first clock signal CKV_L and the second clock signal CKV_R have a predetermined phase difference.

[0082] Next, the gate drivers 400a, and 400b are now described in more detail with reference to FIGS. 9 and 10, where the gate drivers 400a and 400b operate in the forward-scan mode.

[0083] Referring to FIG. 9, the first gate driver 400a outputs the (i-2)th gate signal Gout(i-2), the i-th gate signal Gout(i) and the (i+2)th gate signal Gout(i+2). The second gate driver 400b outputs the (i-1)th gate signal Gout(i-1) and the (i+1)th gate signal Gout(i+1). In the forward-scan mode, the (i-2)th turn-on period Pon(i-2) through the (i+2)th turn-on period Pon(i+2) begin sequentially as shown in FIG. 9.

[0084] The first gate driver 400a receives the first clock signal CKV_L and the first clock bar signal CKVB_L, and outputs the (i-2)th gate signal Gout(i-2), the i-th gate signal Gout(i) and the (i+2)th gate signal Gout(i+2). That is, the first gate driver 400a outputs the first clock bar signal

CKVB_L as the (i-2)th gate signal Gout(i-2) during the (i-2)th turn-on period Pon(i-2), outputs the first clock signal CKV_L as the i-th gate signal Gout(i) during the i-th turn-on period Pon(i), and outputs the first clock bar signal CKVB_L as the (i+2)th gate signal Gout(i+2) during the (i+2)th turn-on period Pon(i+2).

[0085] The second gate driver 400b receives the second clock signal CKV_R and the second clock bar signal CKVB_R, and outputs the (i-1)th gate signal Gout(i-1) and the (i+1)th gate signal Gout(i+1). According to the current exemplary embodiment, the second clock signal CKV_R has a phase difference to that of the first clock signal CKV_L. That is, the second gate driver 400b outputs the second clock signal CKV_R as the (i-1)th gate signal Gout(i-1) during the (i-1)th turn-on period Pon(i-1), and outputs the second clock bar signal CKVB_R as the (i+1)th gate signal Gout(i+1) during the (i+1)th turn-on period Pon(i+1).

[0086] In the forward-scan mode, the (i-2)th turn-on period Pon(i-2) through (i+2)th turn-on period Pon(i+2) begin sequentially.

[0087] Each of the turn-on periods Pon(i-2) through Pon(i+2) overlaps the adjacent another turn-on period. Each of the turn-on periods Pon(i-2) through Pon(i+2) has a precharge-period Ppre(i-2) to Ppre(i+2) and a main-charge-period Pmain(i-2) to Pmain(i+2). The precharge-period Ppre(i) of the i-th turn-on period Pon(i) overlaps the main charge period Pmain(i-1) of the (i-1)th turn-on period Pon(i-1), and the main charge period Pmain(i) of the i-th turn-on period Pon(i) overlaps the precharge-period Ppre(i+1) of the (i+1)th turn-on period Pon(i+1).

[0088] The i-th stage STi of the first gate driver 400a is described hereinafter in further detail with reference to FIG. 10.

[0089] Referring to FIG. 10, the i-th stage STi includes a gate signal supplier 410a and a boost voltage supplier 460a. The gate signal supplier 410a outputs the i-th gate signal Gout(i) to the i-th gate line Gi, and the boost voltage supplier 460a outputs the boost voltage Sout(i) to the i-th storage line Si during the boost voltage-output period Pb.

[0090] The gate signal supplier 410a includes a pull-up-control unit 420a, a pull-up unit 430a, a pull-down unit 440a and a holding unit 450a. Further, referring to FIGS. 6 and 7, the pull-up-control unit 420a of the gate signal supplier 410a receives the (i-2)th gate signal Gout(i-2) and the (i+2)th gate signal Gout(i+2), and outputs the first clock signal CKV_L as the i-th gate signal Gout(i) during the i-th turn-on period Pon(i), as shown in FIG. 11.

[0091] The boost voltage supplier 460a outputs the boost voltage Sout(i) during the boost voltage-output period Pb according to the boost-control signal CONT3(i) as shown in FIG. 9. According to the current exemplary embodiment, the boost voltage Vboost includes edges E1 and E2. The edges E1 and E2 may be a rising edge and a falling edge, respectively. The i-th boost-control signal CONT3(i) includes the boost voltage-output period

Pb. Here, the first edge E1 and the second edge E2 occur in the boost voltage-output period Pb, the i-th turn-on period Pon(i) occurs between the first edge E1 and the second edge E2. That is, the boost voltage-output period Pb overlaps the first edge E1, the i-th turn-on period Pon(i) and the second edge E2. Also, the boost voltage-output period Pb may overlap the (i-1)th turn-on period Pon(i-1) and the (i+1)th turn-on period Pon(i+1).

[0092] According to an exemplary embodiment, the boost voltage supplier 460a comprises the firsts switching element 470a, the second switching element 480a and a switching unit 490a. The first switching element 470a is a diode-connected transistor T8. The second switching element 480a is a diode-connected transistor T9. The switching unit 490a may include transistors T12 and T13.

[0093] The diode-connected transistor T8 supplies the (i-1)th gate signal Gout(i-1) to the third node N3 during the (i-1)th turn-on period Pon(i-1). According to an exemplary embodiment, when the transistor T12 of the switching unit 490a receives the second clock signal CKV_R and turned on supplies the (i-1)th gate signal Gout(i-1) to the third node N3. The diode-connected transistor T9 and the transistor T13 of the switching unit 490a are turned off.

[0094] The diode-connected transistor T9 supplies the (i+1)th gate signal Gout(i+1) to third node N3 during the (i+1)th turn-on period Pon(i+1). Here, the transistor T13 of the switching unit 490a receives the second clock bar signal CKVB_R and when turned on supplies the (i+1)th gate signal Gout(i+1) to the third node N3. The diode-connected transistor T8 and the transistor T12 of the switching unit 490a are turned off.

[0095] After the (i-1)th turn-on period Pon(i-1) and the (i+1)th turn-on period Pon(i+1), the transistors T12 and T13 of the switching unit 490a are enabled according the second clock signal CKV_R and the second clock bar signal CKVB_R, and supply the (i-1)th gate signal Gout(i-1) and the (i+1) the gate signal Gout(i+1) to the third node N3, respectively.

[0096] Therefore, the boost voltage supplier 460a generates the i-th boost-control signal CONT3(i) that has the boost voltage-output period Pb overlapping the (i-1)th turn-on period Pon(i-1) and the (i+1)th turn-on period Pon(i+1), as shown in FIG. 9.

[0097] The boost switching element Qb outputs the boost voltage Sout(i) in response to the i-th boost-control signal CONT3(i) during the boost voltage-output period Pb. The transistors T8, T9, T12, and T13 are a-Si TFTs.

[0098] Operations of the LCD in the forward-scan mode and reverse-scan mode are described with reference to FIGS. 3, 11A, and 11B.

[0099] The operation of the LCD in the forward-scan mode is described with reference to FIGS. 3 and 11A.

[0100] When the precharge-period Ppre(i) begins in the i-th turn-on period Pon(i), the pixel-switching element Qp is turned on, the data voltage applied to the liquid crystal capacitor (not shown) connected with the (i-1)th

gate line G(i-1) is applied to the liquid crystal capacitor Clc connected to the i-th gate line G(i), and the liquid crystal capacitor Clc is pre-charged with the predetermined voltage Vpre, and the liquid crystal capacitor Clc is charged with an image-data voltage Vdat during the main-charge-period Pmain(i).

[0101] After the i-th turn-on period Pon(i), the pixel-switching element Qp is turned off, the storage capacitor Cst receives the second edge E2 of the boost voltage Vboost. When the falling edge E2 is supplied to the storage capacitor Cst, the voltage level of the storage capacitor Cst is lowered with respect to the common voltage Vcom, and the voltage level of liquid crystal capacitor Clc connected to the storage capacitor Cst is lowered with respect to the common voltage Vcom. For example, the capacitance of the storage capacitor Cst and the capacitance of the liquid crystal capacitor Clc are the same, and the voltage of the liquid crystal capacitor Clc is lowered by Vboost/2 according to the falling edge E2.

[0102] That is, the voltage of the liquid crystal capacitor Clc is decreased by the second edge E2, which is applied to the other of the storage capacitor Cst after the i-th turn-on period Pon(i) so that the difference between the boosted voltage of the liquid crystal capacitor Clc and the common voltage Vcom becomes large.

[0103] The operation of the LCD in the reverse-scan mode is described with reference to FIGS. 3 and 11B.

[0104] The (i+2)th through (i-2)th turn-on periods Pon(i+2)-Pon(i-2) begin sequentially.

[0105] The precharge-period Ppre(i) in the i-th turn-on period Pon(i) overlaps the main-charge-period Pmain(i+1) of the (i+1)th turn-on period(Pon(i+1)), and the main-charge-period Pmain(i) of the i-th turn-on period Pon(i) overlaps the precharge-period Ppre(i-1) of the (i-1)th turn-on period Pon(i-1).

[0106] The boost voltage Vboost includes edges E1 and E2.

[0107] The i-th boost-control signal CONT3(i) includes the boost voltage-output period Pb. As described above, the first and second edges E1 and E2 occur in the boost voltage-output period Pb, the i-th turn-on period Pon(i) occurs between the first edge E1 and the second edge E2. That is, the boost voltage-output period Pb overlaps the first edge E1, the i-th turn-on period Pon(i) and the second edge E2. According to an exemplary embodiment, the boost voltage-output period Pb may overlap the (i-1)th turn-on period Pon(i-1) and the (i+1)th turn-on period Pon(i+1).

[0108] When the precharge-period Ppre(i) of the i-th turn-on period Pon(i) begins, the pixel-switching element Qp is turned on, the data voltage applied to the liquid crystal capacitor (not shown) connected with the (i+1)th gate line G(i+1) is applied to the liquid crystal capacitor Clc connected to the i-th gate line G(i), and the liquid crystal capacitor Clc is pre-charged with the predetermined voltage Vpre, and the liquid crystal capacitor Clc is charged with an image-data voltage Vdat during the main charge period Pmain(i).

[0109] After the i -th turn-on period $P_{on}(i)$, the pixel-switching element Q_p is turned off, the storage capacitor C_{st} receives the first edge $E1$ of the boost voltage V_{boost} . When the rising edge $E1$ is supplied to the storage capacitor C_{st} , the voltage level of the storage capacitor C_{st} is increased with respect to the common voltage V_{com} , and the voltage level of liquid crystal capacitor C_{lc} connected to the storage capacitor C_{st} is increased with respect to the common voltage V_{com} . For example, the capacitance of the storage capacitor C_{st} and the capacitance of the liquid crystal capacitor C_{lc} are the same, and the voltage of the liquid crystal capacitor C_{lc} is increased by $V_{boost}/2$ according to the rising edge $E1$.

[0110] That is, when the boost voltage V_{boost} includes the first edge $E1$ and the second edge $E2$, the edges $E1$, and $E2$ occur during the boost voltage-output period P_b , and the i -th turn-on period $P_{on}(i)$ occurs between the first edge $E1$ and the second edge $E2$, the voltage of liquid crystal capacitor C_{lc} is boosted up or decreased in the forward-scan mode or the reverse-scan mode. According to an exemplary embodiment, the boost voltage-output period P_b may overlap with the $(i-1)$ th turn-on period $P_{on}(i-1)$ through the $(i+1)$ th turn-on period.

[0111] However, the boost voltage supplier 460a may be included in the second gate drivers 400b.

[0112] An LCD is described hereinafter in further detail with reference to FIG 12. FIG. 12 is an equivalent schematic circuit diagram of a boost voltage supplier of a liquid crystal display.

[0113] Referring to FIGS. 9, and 12, the boost voltage supplier 461a includes a first switching element $T12$, a second switching element $T13$, a third switching element $T14$, and a fourth switching element $T15$.

[0114] The first switching element $T12$ supplies the $(i-1)$ th gate signal $G_{out}(i-1)$ to the third node $N3$ during the $(i-1)$ th turn-on period $P_{on}(i-1)$, and the second switching element $T13$ supplies the $(i+1)$ th gate signal $G_{out}(i+1)$ to the third node $N3$ during the $(i+1)$ th turn-on period $P_{on}(i+1)$, and the third switching element $T14$ supplies the $(i-1)$ th gate signal $G_{out}(i-1)$ to the third node $N3$ in the $(i-2)$ th turn-on period $P_{on}(i-2)$, and the fourth switching element $T15$ supplies the $(i+1)$ th gate signal $G_{out}(i+1)$ to the third node $N3$ in the $(i+2)$ th turn-on period $P_{on}(i+2)$.

[0115] In more detail, the third switching element $T14$ supplies the $(i-1)$ th gate signal $G_{out}(i-1)$ to the third node $N3$ during the precharge-period $P_{pre}(i-2)$ in the $(i-2)$ th turn-on period $P_{on}(i-2)$ so that the i -th boost-control signal $CONT3(i)$ is at low level during the $(i-2)$ th turn-on period $P_{on}(i-2)$.

[0116] The first switching element $T12$ receives the second clock signal CKV_R and is turned on and supplies the $(i-1)$ th gate signal $G_{out}(i-1)$ to the third node $N3$ during the $(i-1)$ th turn-on period $P_{on}(i-1)$ so that the i -th boost-control signal $CONT3(i)$ is at high level during the $(i-1)$ th turn-on period $P_{on}(i-1)$. Here, the second switching element $T13$ and the fourth switching element $T15$ are turned off.

[0117] The second switching element $T13$ receives the

second clock bar signal $CKVB_R$ and is turned on and supplies the $(i+1)$ th gate signal $G_{out}(i+1)$ to the third node $N3$ during the $(i+1)$ th turn-on period $P_{on}(i+1)$ so that the i -th boost-control signal $CONT3(i)$ is at high level during the $(i+1)$ th turn-on period $P_{on}(i+1)$. Here, the first switching element $T12$ and the third switching element $T14$ are turned off.

[0118] The fourth switching element $T15$ supplies the $(i+1)$ th gate signal $G_{out}(i+1)$ to the third node $N3$ during the main-charge-period $P_{main}(i+2)$ in the $(i+2)$ th turn-on period $P_{on}(i+2)$ so that the i -th boost-control signal $CONT3(i)$ is at low level during the $(i-2)$ th turn-on period $P_{on}(i-2)$. According to the current exemplary embodiment, the switching elements $T12\sim T15$ are a-Si TFTs.

[0119] That is, the first through fourth switching elements $T12\sim T15$ supply the i -th boost-control signal $CONT3(i)$ to the third node $N3$ during the boost voltage-output period P_b as shown in the FIG. 9. Here the boost voltage-output period P_b may overlap the $(i-1)$ th turn-on period $P_{on}(i-1)$ and the $(i+1)$ th turn-on period $P_{on}(i+1)$.

[0120] An LCD is described hereinafter in further detail with reference to FIGS. 13 and 14. FIG. 13 is an equivalent schematic circuit diagram of a boost voltage supplier of a liquid crystal display, and FIG 14 is a signal waveform timing chart illustrating an operation of the boost voltage supplier in FIG. 13.

[0121] Referring to FIGS. 13 and 14, the boost voltage supplier 462a includes a first switching element $T12$, a second switching element $T13$, and switching units $T16$, $T17$.

[0122] The first switching element $T12$ supplies the $(i-1)$ th gate signal $G_{out}(i-1)$ to the third node $N3$ during the $(i-1)$ th turn-on period $P_{on}(i-1)$. The second switching element $T13$ supplies the $(i+1)$ th gate signal $G_{out}(i+1)$ to the third node $N3$. The switching unit $T16$, $T17$ supplies the ground voltage to the third node $N3$.

[0123] The third switching element $T16$ receives the $(i-3)$ th gate signal $G_{out}(i-3)$ during the $(i-3)$ th turn-on period $P_{on}(i-3)$ and when turned on supplies the ground voltage to the third node $N3$ so that the i -th boost-control signal $CONT3(i)$ is at low level during the $(i-3)$ th turn-on period $P_{on}(i-3)$.

[0124] The first switching element $T12$ receives the second clock signal CKV_R during the $(i-1)$ th turn-on period $P_{on}(i-1)$ and when turned on supplies the $(i-1)$ th gate signal $G_{out}(i-1)$ to the third node $N3$ so that the i -th boost-control signal $CONT3(i)$ is at high level during the $(i-1)$ th turn-on period $P_{on}(i-1)$. The second switching element $T13$ and the fourth switching element $T17$ are turned off.

[0125] Next, during the $(i+1)$ th turn-on period ($P_{on}(i+1)$), the second switching element $T13$ receives the second clock bar signal $CKVB_R$ and is turned on and supplies the $(i+1)$ th gate signal $G_{out}(i+1)$ to the third node $N3$ so that the boost-control signal $CONT3(i)$ is at high level during the $(i+1)$ th turn-on period $P_{on}(i+1)$. The first switching element $T12$ and the third switching element $T16$ are turned off.

[0126] Next, the fourth switching element $T17$ receives

the (i+3) gate signal $G_{out(i+3)}$ during the (i+3)th turn-on period $P_{on(i+3)}$ and is turned on and supplies the ground voltage to the third node N3 so that the i-th boost-control signal $CONT3(i)$ is at low level during the (i+3)th turn-on period $P_{on(i+3)}$. According to the current exemplary embodiment, the switching elements T12, T13, T16, and T17 are a-Si TFTs.

[0127] That is, the first through fourth switching elements T12, T13, T16, and T17 supply the i-th boost-control signal $CONT3(i)$ at high level during the boost voltage-output period P_b to the third node N3 as shown in Fig. 13. According to the current exemplary embodiment, the boost voltage-output period P_b overlaps the (i-1)th turn-on period $P_{on(i-1)}$ and the (i+1)th turn-on period $P_{on(i+1)}$.

[0128] As described above, according to the liquid crystal display and the driving method of the same of present invention, power consumption is decreased in the forward-scan mode and the reverse-scan mode.

Claims

1. A liquid crystal display (10, 11) comprising:

first to n-th gate lines (G_1, \dots, G_n);
 first to n-th storage lines (S_1, \dots, S_n);
 first to m-th data lines (D_1, \dots, D_m);
 a plurality of pixels, each pixel being connected to a $i(1 \leq i \leq n)$ -th gate line (G_i), to a i-th storage line (S_i), to a $j(1 \leq j \leq m)$ -th data line (D_j) and to a common voltage (V_{com}), wherein each pixel comprises
 a pixel-switching element (Q_p) connected to an i-th gate line (G_i) and having one terminal connected to the j-th data line (D_j);
 a liquid crystal capacitor (C_{lc});
 a storage capacitor (C_{st}), wherein
 a first electrode of the storage capacitor (C_{st}) is connected to another terminal of the pixel-switching element (Q_p), a second electrode of the storage capacitor (C_{st}) is connected to a storage line (S_i), and
 a first electrode of the liquid crystal capacitor (C_{lc}) is connected to the other terminal of the pixel-switching element (Q_p) and a second electrode of the liquid crystal capacitor (C_{lc}) is connected to the common voltage (V_{com});
 a data driver (700) adapted to supply a data voltage (V_{dat}) to the first to m-th data lines (D_1, \dots, D_m); and
 a gate driver (400; 400a, 400b) connected to the first to n-th gate lines (G_1, \dots, G_n) and to the first to n-th storage lines (S_1, \dots, S_n), wherein the gate driver (400; 400a, 400b) is adapted to supply first to n-th gate signals ($G_{out(1)}, \dots, G_{out(n)}$) to the first to n-th gate lines (G_1, \dots, G_n) during first to n-th turn-on periods ($P_{on(1)}, \dots,$

$P_{on(n)}$) so that the pixel-switching element (Q_p) is turned on,

the gate driver (400; 400a, 400b) is further adapted to operate in one of a forward-scan mode in which the first to n-th turn-on period ($P_{on(1)}, \dots, P_{on(n)}$) begins sequentially and a reverse-scan mode in which the n-th to first turn-on period ($P_{on(n)}, \dots, P_{on(1)}$) begins sequentially in response to a scan direction-control signal (DIR; DIRB),

the gate driver is further adapted to supply first to n-th boost voltages ($S_{out(1)}, \dots, S_{out(n)}$) to the plurality of storage lines (S_1, \dots, S_n), respectively; and

the gate driver includes a plurality of stages (ST_1, \dots, ST_n), which are connected to one another in a cascade manner, each of the stages (ST_1, \dots, ST_n) being connected to a respective corresponding gate line (G_i) of the plurality of gate lines (G_1, \dots, G_n) and to a respective corresponding storage line ($S(i)$) of the plurality of storage lines (S_1, \dots, S_n), the stages (ST_1, \dots, ST_n) being adapted to output the gate signals ($G_{out(1)}, \dots, G_{out(n)}$) to the plurality of gate lines (G_1, \dots, G_n), respectively, and the boost voltages ($S_{out(1)}, \dots, S_{out(n)}$) to the plurality of storage lines (S_1, \dots, S_n) during a boost voltage-output period (P_b), respectively, and wherein each of the stages (ST_1, \dots, ST_n) is adapted to receive the scan-direction-control signal (DIR, DIRB).

characterized in that

the liquid crystal display is adapted to provide to all the stages (ST_1, \dots, ST_n) a boost voltage (V_{boost}) that swings between a high level and a low level; and each of the stages (ST_1, \dots, ST_n) comprises a first switching unit (Q_b) having one terminal connected to the boost voltage (V_{boost}), another terminal connected to the respective storage line, the first switching unit (Q_b) of the i-th stage (ST_i) being turned-on by a boost-control signal ($CONT3(i)$) such that the boost-switching element (Q_b) of the i-th stage (ST_i) applies the boost voltage (V_{boost}) to the storage line (S_i) in response to the boost-control signal ($CONT3(i)$) during the boost-voltage output period (P_b) and the gate driver is further adapted to provide the boost control signal ($CONT3(i)$) to the first switching unit (Q_b) during the boost voltage-output period (P_b) such that the boost voltage ($S_{out(i)}$) comprises a first edge (E_1) occurring during the (i-1)-th turn-on period ($P_{on(i-1)}$), then an edge occurring during the (i-th turn-on period ($P_{on(i)}$), then a second edge (E_2) occurring during the (i+1)th turn-on period ($P_{on(i+1)}$), the first and second edges (E_1, E_2) occurring in the boost voltage-output period (P_b) and being both either rising edges or a falling edges, and the i-th turn-on period ($P_{on(i)}$) occurring between the first and

- second edges (E1, E2), and such that the liquid crystal capacitor (Clc) of the pixel connected to the i-th gate line is charged with a data voltage (Vdat) during an i-th turn-on period (Pon(i)) via the pixel-switching element, and the data voltage (Vdat) of the liquid crystal capacitor (Clc) is boosted up or decreased by the first edge (E1) or the second edge (E2) supplied to the second electrode of the storage capacitor (Cst) after the i-th turn-on period (Pon(i)).
2. The liquid crystal display (10, 11) of claim 1, the i-th stage (STi) comprising a gate signal supplier (410; 410a) adapted to the i-th gate signal (Gout(i)) and a boost voltage supplier (460; 460a) which is adapted to supply the boost voltage (Vboost) to the other electrode of the storage capacitor (Cst) during the boost voltage-output period (Pb).
 3. The liquid crystal display (10, 11) of claim 2, wherein the boost voltage supplier (460; 460a) comprises:
 - a boost-control signal generator (460) which is adapted to generate the boost-control signal (CONT3(i)) having the boost voltage-output period (Pb).
 4. The liquid crystal display (10, 11) of claim 3, wherein the boost voltage-output period (Pb) overlaps the (i-1)th turn-on period (Pon(i-1)) of the (i-1)th gate signal (Gout(i-1)) and the (i+1)th turn-on period (Pon(i+1)) of the (i+1)th gate signal (Gout(i+1)).
 5. The liquid crystal display (10, 11) of claim 4, wherein the boost-control signal generator (460) is connected to the storage line (Si) and is adapted to output the boost-control signal (CONT3(i)) to the storage line (Si), the boost-control signal generator (460) comprising:
 - a first switching element (470) connected to the (i-1)th gate line (G(i-1)) and adapted to supply the (i-1)th gate signal (Gout(i-1)) at a first level to the output node during the (i-1)th turn-on period (Pon(i-1));
 - a second switching element (480) connected to the (i+1)th gate line (G(i+1)) and adapted to supply the (i+1)th gate signal (Gout(i+1)) at the first level to the output node during the (i+1)th turn-on period (Pon(i+1)); and
 - a second switching unit (490) adapted to change the storage line (Si) to a second level after the (i-1)th turn-on period (Pon(i-1)) and the (i+1)th turn-on period (Pon(i+1)).
 6. The liquid crystal display (10, 11) of claim 5, wherein the first and second switching elements (470, 480) are diode-connected amorphous silicon thin film

transistors, respectively, and the second switching unit (490) comprises an amorphous silicon thin film transistor.

7. The liquid crystal display (10, 11) of claim 2, wherein the gate signal supplier (410; 410a) comprises an amorphous silicon thin film transistor which outputs the i-th gate signal.

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Patentansprüche

1. Flüssigkristallanzeige (10, 11), umfassend:
 - erste bis n-te Gateleitungen (G1, ..., Gn);
 - erste bis n-te Speicherleitungen (S1, ..., Sn);
 - erste bis m-te Datenleitungen (D1, ..., Dm);
 - eine Vielzahl von Pixeln, wobei jedes Pixel mit einer i(1 ≤ i ≤ n)-ten Gateleitung (Gi), mit einer i-ten Speicherleitung (Si), mit einer j(1 ≤ j ≤ m)-ten Datenleitung (Dj) und mit einer gemeinsamen Spannung (Vcom) verbunden ist, wobei jedes Pixel umfasst:
 - ein Pixel-Schaltelement (Qp), das mit einer i-ten Gateleitung (Gi) verbunden ist und dessen einer Anschluss mit der j-ten Datenleitung (Dj) verbunden ist;
 - einen Flüssigkristallkondensator (Clc);
 - einen Speicherkondensator (Cst), wobei eine erste Elektrode des Speicherkondensators (Cst) mit einem anderen Anschluss des Pixel-Schaltelements (Qp) und eine zweite Elektrode des Speicherkondensators (Cst) mit einer Speicherleitung (Si) verbunden ist, und
 - eine erste Elektrode des Flüssigkristallkondensators (Clc) mit dem anderen Anschluss des Pixel-Schaltelements (Qp) und eine zweite Elektrode des Flüssigkristallkondensators (Clc) mit der gemeinsamen Spannung (Vcom) verbunden ist;
 - einen Datentreiber (700), der dazu eingerichtet ist, den ersten bis m-ten Datenleitungen (D1, ..., Dm) eine Datenspannung (Vdat) zuzuführen; und
 - einen Gate-Treiber (400; 400a, 400b), der mit den ersten bis n-ten Gateleitungen (G1, ..., Gn) und mit den ersten bis n-ten Speicherleitungen (S1, ..., Sn) verbunden ist, wobei der Gate-Treiber (400; 400a, 400b) dazu eingerichtet ist, den ersten bis n-ten Gateleitungen (G1, ..., Gn) während erster bis n-ter Einschaltperioden (Pon(1), ..., Pon(n)) erste bis n-te Gatesignale (Gout(1), ..., Gout(n)) zuzuführen, so dass das Pixel-Schaltelement (Qp) eingeschaltet ist,

wobei der Gate-Treiber (400; 400a, 400b) ferner dazu eingerichtet ist, als Reaktion auf ein Scanrichtungssteuersignal (DIR; DIRB) entweder in einem Vorwärtsscan-Modus, in dem nacheinander die erste bis n-te Einschaltperiode (Pon(1), ..., Pon(n)) beginnen, oder in einem Rückwärtsscan-Modus, in dem nacheinander die n-te bis erste Einschaltperiode (Pon(n), ..., Pon(1)) beginnen, zu arbeiten, wobei der Gate-Treiber ferner dazu eingerichtet ist, der Vielzahl von Speicherleitungen (S1, ..., Sn) jeweils erste bis n-te Boostspannungen (Sout(1), ..., Sout(n)) zuzuführen, und der Gate-Treiber eine Vielzahl von Stufen (ST1, ..., STn) umfasst, die kaskadenartig miteinander verbunden sind, wobei jede der Stufen (ST1, ..., STn) mit einer entsprechenden Gateleitung (Gi) der Vielzahl von Gateleitungen (G1, ..., Gn) und mit einer jeweiligen entsprechenden Speicherleitung (S(i)) der Vielzahl von Speicherleitungen (S1, ..., Sn) verbunden ist, wobei die Stufen (ST1, ..., STn) dazu eingerichtet sind, die Gatesignale (Gout(1), ..., Gout(n)) jeweils an die Vielzahl von Gateleitungen (G1, ..., Gn) auszugeben, und die Boostspannungen (Sout(1), ..., Sout(n)) während einer Boostspannungs-Ausgabeperiode (Pb) jeweils an die Vielzahl von Speicherleitungen (S1, ..., Sn) auszugeben, und wobei jede der Stufen (ST1, ..., STn) dazu eingerichtet ist, das Scanrichtungssteuersignal (DIR, DIRB) zu empfangen,

dadurch gekennzeichnet, dass

die Flüssigkristallanzeige dazu eingerichtet ist, allen Stufen (ST1, ..., STn) eine Boostspannung (Vboost) bereit zu stellen, die zwischen einem hohen Pegel und einem niedrigen Pegel schwingt, und jede der Stufen (ST1, ..., STn) eine erste Schalteinheit (Qb) umfasst, deren einer Anschluss mit der Boostspannung (Vboost) und deren anderer Anschluss mit der jeweiligen Speicherleitung verbunden ist, wobei die erste Schalteinheit (Qb) der i-ten Stufe (STi) durch ein Booststeuersignal (CONT3(i)) eingeschaltet wird, so dass das Boostschaltelement (Qb) der i-ten Stufe (STi) die Boostspannung (Vboost) während der Boostspannungsausgabeperiode (Pb) als Reaktion auf das Booststeuersignal (CONT3(i)) an die Speicherleitung (Si) anlegt, und der Gate-Treiber ferner dazu eingerichtet ist, das Booststeuersignal (CONT3(i)) der ersten Schalteinheit (Qb) während der Boostspannungsausgabeperiode (Pb) so bereit zu stellen, dass die Boostspannung (Sout(i)) eine erste Flanke (E1), die während

der (i-1)-ten Einschaltperiode (Pon(i-1)) auftritt, dann eine Flanke, die während der i-ten Einschaltperiode (Pon(i)) auftritt, dann eine zweite Flanke (E2), die während der (i+1)-ten Einschaltperiode (Pon(i+1)) auftritt, aufweist, wobei die ersten und zweiten Flanken (E1, E2) in der Boostspannungsausgabeperiode (Pb) auftreten und beide entweder ansteigende oder abfallende Flanken sind, und die i-te Einschaltperiode (Pon(i)) zwischen den ersten und zweiten Flanken (E1, E2) auftritt, und so, dass der Flüssigkristallkondensator (Cic) des mit der i-ten Gateleitung verbundenen Pixels über das Pixel-Schaltelement während einer i-ten Einschaltperiode (Pon(i)) mit einer Datenspannung (Vdat) geladen wird, und die Datenspannung (Vdat) des Flüssigkristallkondensators (Cic) durch die erste Flanke (E1) oder die zweite Flanke (E2), die der zweiten Elektrode des Speicherkondensators (Cst) nach der i-ten Einschaltperiode (Pon(i)) zugeführt wird, erhöht oder verringert wird.

2. Flüssigkristallanzeige (10, 11) nach Anspruch 1, wobei die i-te Stufe (STi) eine Gatesignal-Zuführeinrichtung (410; 410a), die dazu eingerichtet ist, das i-te Gatesignal (Gout(i)) auszugeben, und eine Boostspannungszuführeinrichtung (460; 460a), die dazu eingerichtet ist, die Boostspannung (Vboost) der anderen Elektrode des Speicherkondensators (Cst) während der Boostspannungsausgabeperiode (Pb) zuzuführen, umfasst.
3. Flüssigkristallanzeige (10, 11) nach Anspruch 2, wobei die Boostspannungszuführeinrichtung (460; 460a) folgendes umfasst:

Einen Booststeuersignalgenerator (460), der dazu eingerichtet ist, das Booststeuersignal (CONT3(i)) mit der Boostspannungsausgabeperiode (Pb) zu erzeugen.

4. Flüssigkristallanzeige (10, 11) nach Anspruch 3, wobei die Boostspannungsausgabeperiode (Pb) die (i-1)-te Einschaltperiode (Pon(i-1)) des (i-1)-ten Gatesignals (Gout(i-1)) und die (i+1)-te Einschaltperiode (Pon(i+1)) des (i+1)-ten Gatesignals (Gout(i+1)) überlappt.
5. Flüssigkristallanzeige (10, 11) nach Anspruch 4, wobei der Booststeuersignalgenerator (460) mit der Speicherleitung (Si) verbunden und dazu eingerichtet ist, das Booststeuersignal (CONT3(i)) an die Speicherleitung (Si) auszugeben, und der Booststeuersignalgenerator (460) folgendes umfasst:

ein erstes Schaltelement (470), das mit der (i-1)-ten Gateleitung (G(i-1)) verbunden und dazu eingerichtet ist, das (i-1)-te Gatesignal (Gout(i-1)) mit einem ersten Pegel während der (i-1)-ten

- Einschaltperiode (Pon(i-1)) dem Ausgabeknoten zuzuführen;
 ein zweites Schaltelement (480), das mit der (i+1)-ten Gateleitung (G(i+1)) verbunden und dazu eingerichtet ist, das (i+1)-te Gatesignal (Gout(i+1)) mit dem ersten Pegel während der (i+1)-ten Einschaltperiode (Pon(i+1)) dem Ausgabeknoten zuzuführen, und
 eine zweite Schalteinheit (490), die dazu eingerichtet ist, die Speicherleitung (Si) nach der (i-1)-ten Einschaltperiode (Pon(i-1)) und der (i+1)-ten Einschaltperiode (Pon(i+1)) auf einen zweiten Pegel umzuschalten.
6. Flüssigkristallanzeige (10, 11) nach Anspruch 5, wobei die ersten und zweiten Schaltelemente (470, 480) Dioden-verbundene Dünnschichttransistoren aus amorphem Silicium sind und die zweite Schalteinheit (490) einen Dünnschichttransistor aus amorphem Silicium umfasst.
7. Flüssigkristallanzeige (10, 11) nach Anspruch 2, wobei die Gatesignal-Zuführeinrichtung (410; 410a) einen Dünnschichttransistor aus amorphem Silicium umfasst, der das i-te Gatesignal ausgibt.

Revendications

1. Un écran à cristaux liquides (10, 11) comprenant :
- La première à la n^{ième} ligne de porte (G1, ..., Gn) ;
 - La première à la n^{ième} ligne de stockage (S1, ..., Sn) ;
 - La première à la m^{ième} ligne de données (D1, ..., Dm) ;
 - Une pluralité de pixels, chaque pixel étant connecté à une i(1 ≤ i ≤ n)-ième ligne de porte (Gi), à une i-^{ième} ligne de stockage (Si), à une j(1 ≤ j ≤ m)-ième ligne de donnée (Dj) et à une tension ordinaire (Vcom), où chaque pixel comprend
 - Un élément de commutation à pixel (Qp) connecté à un i^{ème} ligne de porte (Gi) et ayant un terminal connecté à la j^{ème} ligne de donnée (Dj) ;
 - Un condensateur à cristaux liquides (Clc) ;
 - Un condensateur de stockage (Cst), où
 - Une première électrode du condensateur de stockage (Cst) est connectée à un autre terminal de l'élément de commutation à pixel (Qp), une deuxième électrode du condensateur de stockage (Cst) est connectée à une ligne de stockage (Si), et
 - Une première électrode du condensateur à cristaux liquides (Clc) est connectée à l'autre terminal de l'élément de commutation à pixel (Op) et

une deuxième électrode du condensateur à cristaux liquides (Clc) est connectée à la tension ordinaire (Vcom) ;

Un conducteur de données (700) adapté pour fournir une tension de données (Vdat) vers la première à la m^{ième} lignes de donnée (D1, ..., Dm) ; et

Un conducteur de porte (400 ; 400a, 400b) connecté à la première à n^{ième} ligne de porte (G1, ..., Gn) et à la première à n^{ième} ligne de stockage (S1, ..., Sn), où le conducteur de porte (400 ; 400a, 400b) est adapté pour fournir d'abord au n^{ième} signal de porte (Gout(1), ..., Gout(n)) à la première à n^{ième} ligne de porte (G1, ..., Gn) pendant la première à la n^{ième} période de mise en marche (Pon(1), ..., Pon(n)) pour que l'élément de commutation à pixel (Qp) soit en marche,

Le conducteur de porte (400 ; 400a, 400b) est de plus adapté pour fonctionner dans un mode de balayage avant dans lequel la première à n^{ième} période de mise en marche (Pon(1), ..., Pon(n)) commence séquentiellement et un mode de balayage arrière dans lequel la n^{ième} à première période de mise en marche (Pon(n), ..., Pon(1)) commence séquentiellement en réponse à un signal de contrôle de direction de balayage (DIR ; DIRB),

Le conducteur de porte est de plus adapté pour fournir la première à la n^{ième} tension d'amplification (Sout(1), ..., Sout(n)) à la pluralité de lignes de stockage (S1, ..., Sn), respectivement ; et

Le conducteur de porte inclut une pluralité de stades (ST1, ..., STn) qui sont connectés les uns aux autres en cascade, chacun des stades (ST1, ..., STn) étant connecté à une ligne de porte correspondante respective (Gi) de la pluralité des lignes de porte (G1, ..., Gn) et à une ligne de stockage correspondante respective (S(i)) de la pluralité de lignes de stockage (S1, ..., Sn), les stades (ST1, ..., STn) étant adaptés pour faire sortir les signaux de porte (Gout(n)) vers la pluralité des lignes de porte (G1, ..., Gn), respectivement, et les tensions d'amplification (Sout(1), ..., Sout(n)) vers la pluralité de lignes de stockage (S1, ..., Sn) pendant une période de sortie de tension d'amplification (Pb), respectivement, et où chacun des stades (ST1, ..., STn) est adapté pour recevoir le signal de contrôle de direction de balayage (DIR, DIRB).

Caractérisé en ce que

L'écran en cristaux liquides est adapté pour fournir à tous les stades (ST1, ... STn) une tension d'amplification (Vboost) qui oscille entre un haut niveau et un niveau bas ; et

Chacun des stades (ST1, ..., STn) comprend une première unité de commutation (Qb) ayant un

terminal connecté à la tension d'amplification (Vboost), un autre terminal connecté à la ligne de stockage respective, la première unité de commutation (Qb) du i -ième stade (STi) étant mise en marche par un signal de contrôle d'amplification (CONT3(i)) tel que l'élément de commutation d'amplification (Qb) du i -ième stade (STi) applique la tension d'amplification (Vboost) à la ligne de stockage (Si) en réponse au signal de contrôle d'amplification (CONT3(i)) pendant la période de sortie de tension d'amplification (Pb), et

Le conducteur de porte est de plus adapté pour fournir le signal de contrôle d'amplification (CONT3(i)) à la première unité de commutation (Qb) pendant la période de sortie de tension d'amplification (Pb) de sorte que la tension d'amplification (Sout(i)) comprenne un premier bord (E1) se produisant pendant la $(i-1)$ -ième période de mise en marche (Pon(i-1)), puis un bord se produisant pendant la (i) -ième période de mise en marche (Pon(i)), puis un deuxième bord (E2) se produisant pendant la $(i+1)$ -ième période de mise en marche (Pon(i+1)), le premier et le deuxième bord (E1, E2) se produisant dans la période de sortie de tension d'amplification (Pb) et étant tous les deux soit des coins montants soit des coins descendants, et la i -ième période de mise en marche (Pon(i)) se produisant entre le premier et le deuxième bords (E1, E2), et

De sorte que le condensateur en cristaux liquides (Clc) du pixel connecté à la i -ième ligne de porte est chargé d'une tension de données (Vdat) pendant une i -ième période de mise en marche (Pon(i)) via l'élément de commutation à pixel, et la tension de données (Vdat) du condensateur en cristaux liquides (Clc) est amplifiée ou diminuée du premier bord (E1) ou du deuxième bord (E2) fournie à la deuxième électrode du condensateur de stockage (Cst) après la i -ième période de mise en marche (Pon(i)).

2. L'écran en cristaux liquides (10, 11) de la revendication 1, le i -ième stade (STi) comprenant un fournisseur de signal de porte (410 ; 410a) adapté pour faire sortir le i -ième signal de porte (Gout(i)) et un fournisseur de tension d'amplification (460 ; 460a) qui est adapté pour fournir la tension d'amplification (Vboost) à l'autre électrode du condensateur de stockage (Cst) pendant la période de sortie de tension d'amplification (Pb).

3. L'écran en cristaux liquides (10, 11) de la revendication 2, où le fournisseur de tension d'amplification (460 ; 460a) comprend :

Un générateur de signal de contrôle d'amplification (460) qui est adapté pour générer le signal de contrôle d'amplification (CONT3(i)) ayant la période de sortie de tension d'amplification (Pb).

4. L'écran en cristaux liquides (10, 11) de la revendication 3, où la période de sortie de tension d'amplification (Pb) chevauche la $(i-1)$ -ième période de mise en marche (Pon(i-1)) du $(i-1)$ -ième signal de porte (Gout(i-1)) et la $(i+1)$ -ième période de mise en marche (Pon(i+1)) du $(i+1)$ -ième signal de porte (Gout(i+1)).

5. L'écran en cristaux liquides (10, 11) de la revendication 4, où le générateur de signal de contrôle d'amplification (460) est connecté à la ligne de stockage (Si) et est adapté pour faire sortir le signal de contrôle d'amplification (CONT3(i)) vers la ligne de stockage (Si), le générateur de signal de contrôle d'amplification (460) comprenant :

Un premier élément de commutation (470) connecté à la $(i-1)$ -ième ligne de porte (G(i-1)) et adapté pour fournir le $(i-1)$ -ième signal de porte (Gout(i-1)) à un premier niveau au noeud de sortie pendant la $(i-1)$ -ième période de mise en marche (Pon(i-1)) ;

Un deuxième élément de commutation (480) connecté à la $(i+1)$ -ième ligne de porte (G(i+1)) et adapté pour fournir le $(i+1)$ -ième signal de porte (Gout(i+1)) au premier niveau au noeud de sortie pendant la $(i+1)$ -ième période de mise en marche (Pon(i+1)) ; et

Une deuxième unité de commutation (490) adaptée pour changer la ligne de stockage (Si) à un deuxième niveau après la $(i-1)$ -ième période de mise en marche (Pon(i-1)) et la $(i+1)$ -ième période de mise en marche (Pon(i+1)).

6. L'écran en cristaux liquides (10, 11) de la revendication 5, où les premiers et deuxièmes éléments de commutation (470, 480) sont des transistors à couche mince en silicone amorphe connectés par diode, respectivement, et la deuxième unité de commutation (490) comprend un transistor à couche mince en silicone amorphe.

7. L'écran en cristaux liquides (10, 11) de la revendication 2, où le fournisseur de signal de porte (410 ; 410a) comprend un transistor à couche mince en silicone amorphe qui fait sortir le i -ième signal de porte.

FIG. 1

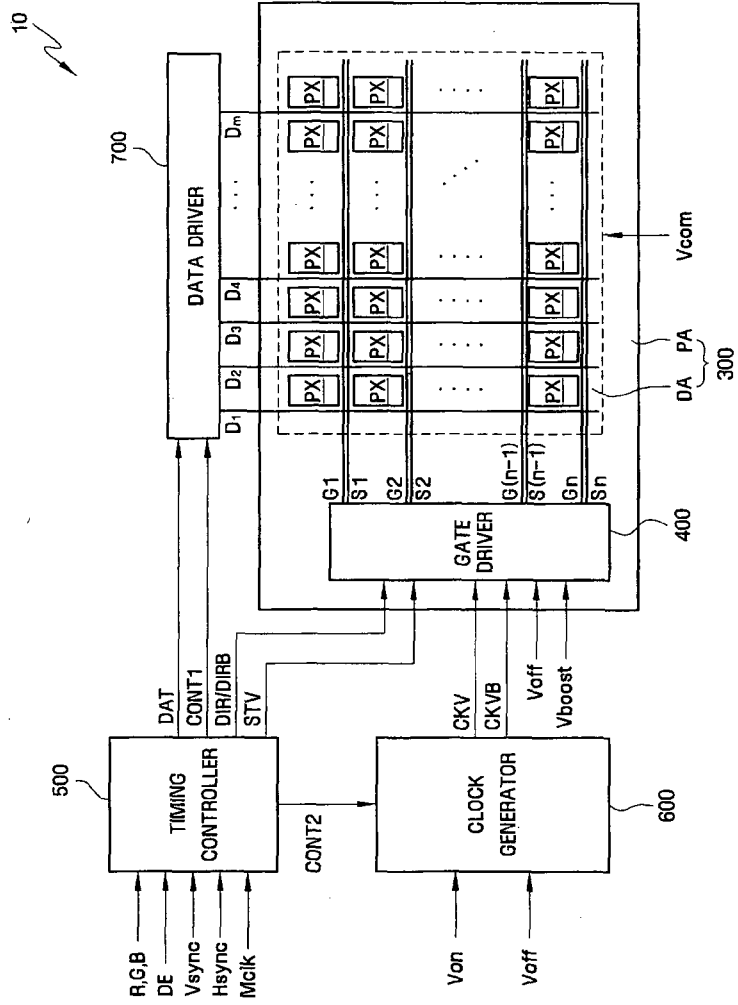


FIG. 2

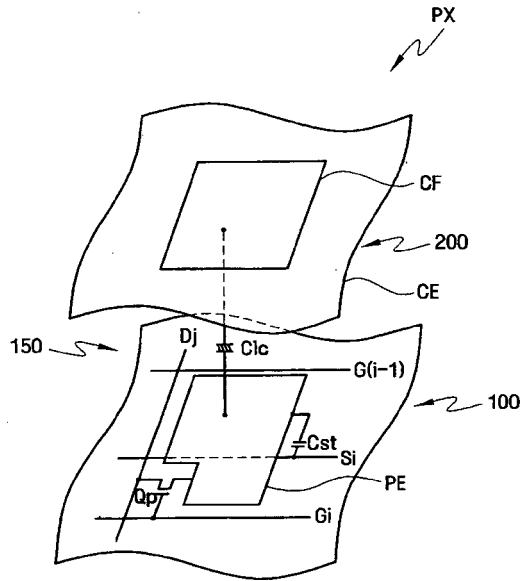


FIG. 3

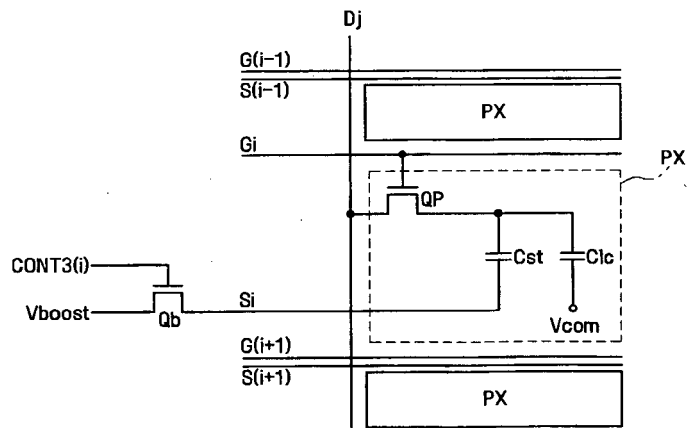
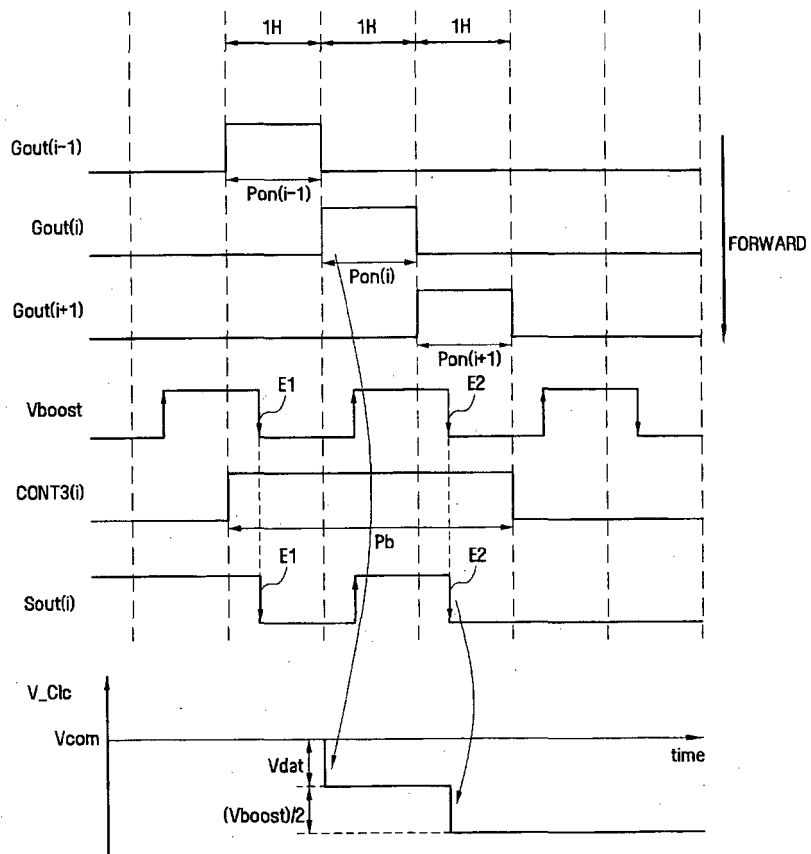
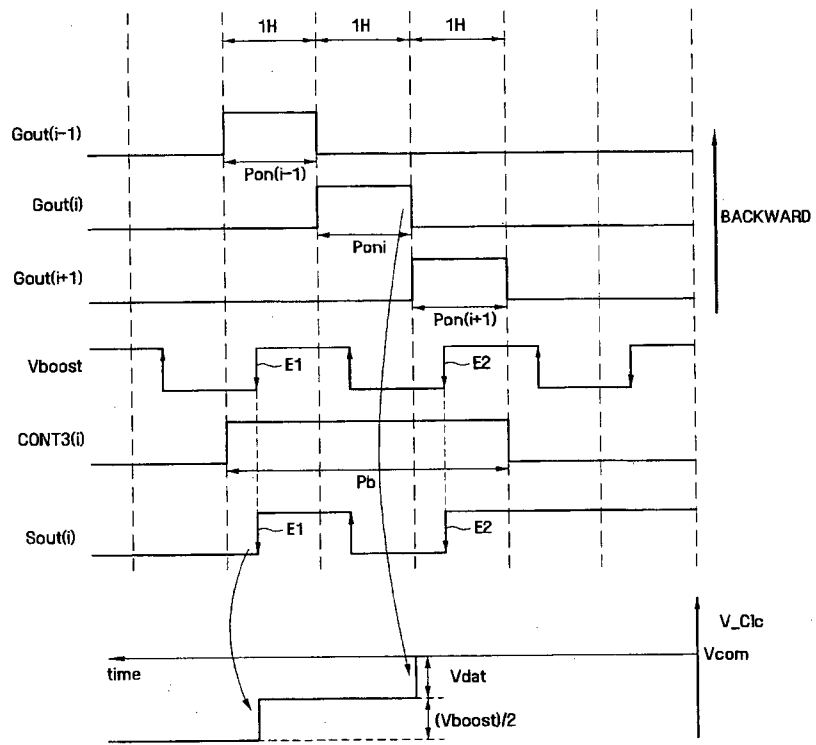


FIG. 4A



< FORWARD-SCAN MODE >

FIG. 4B



< REVERSE-SCAN MODE >

FIG. 5

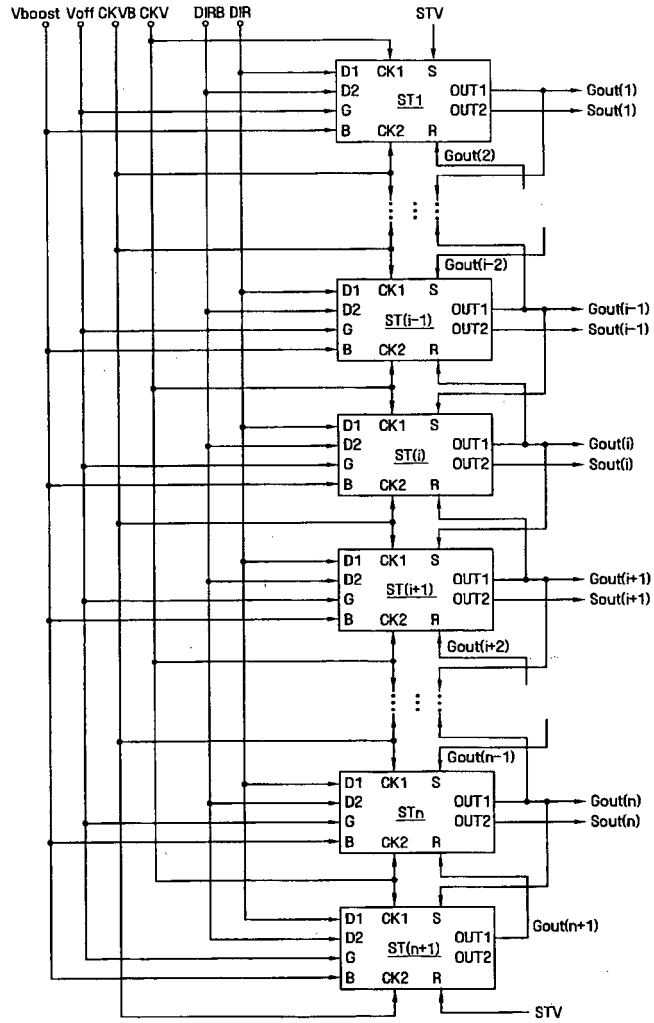


FIG. 7

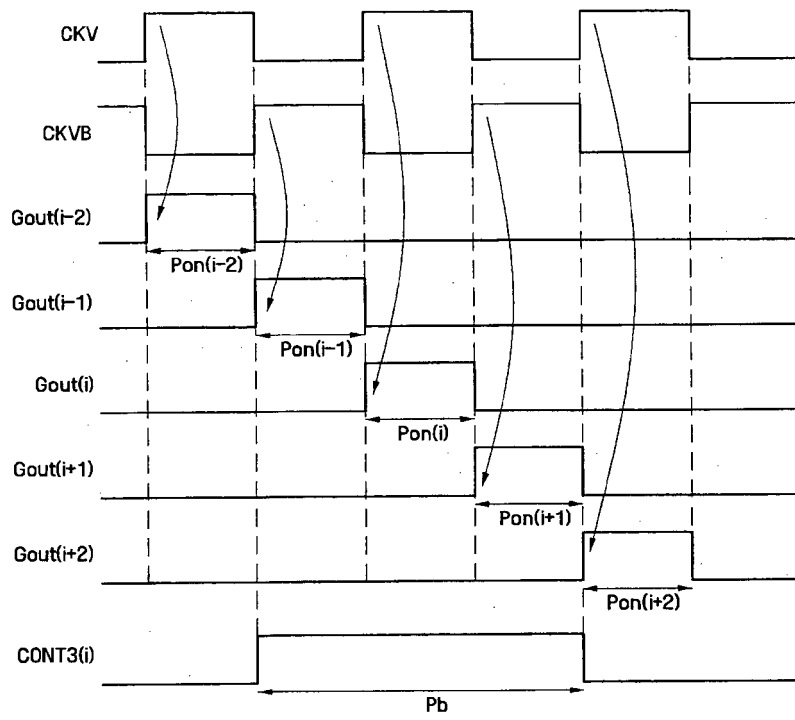


FIG. 8

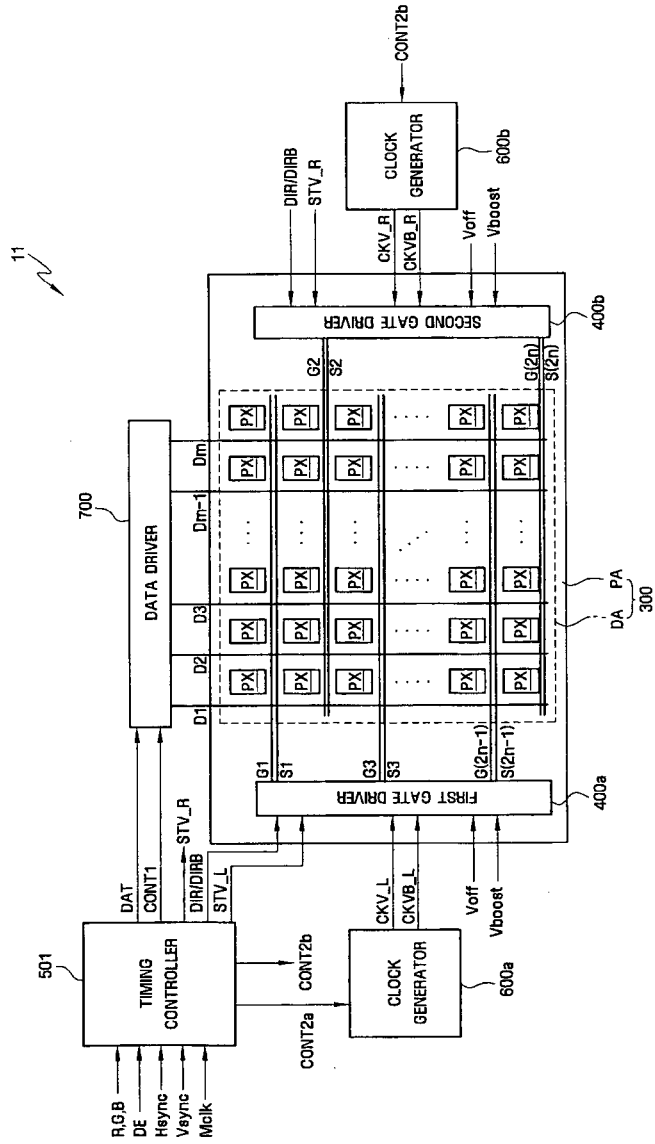


FIG. 9

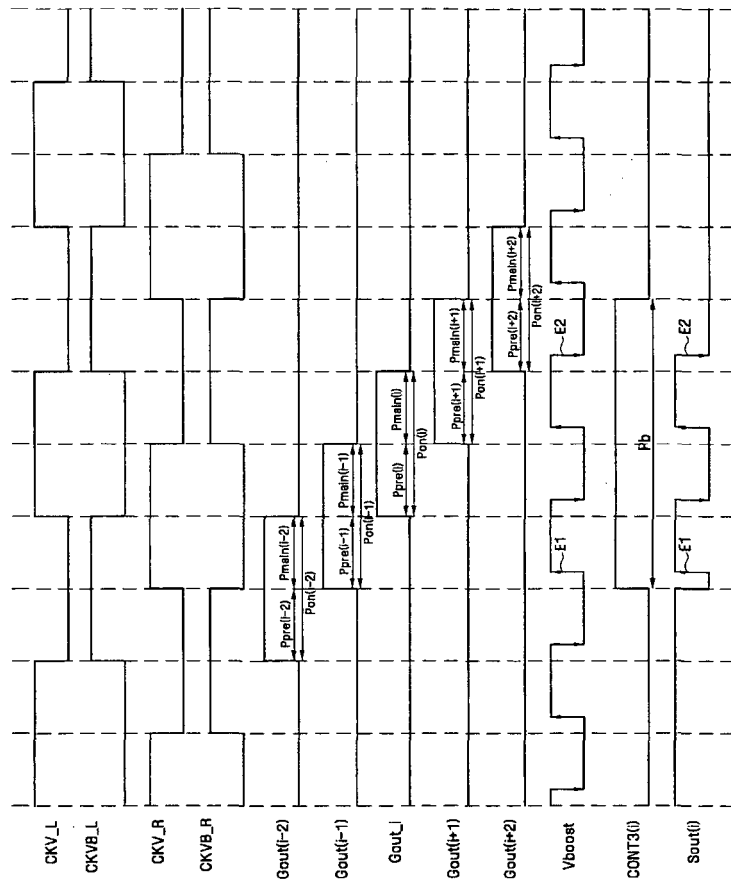


FIG. 11A

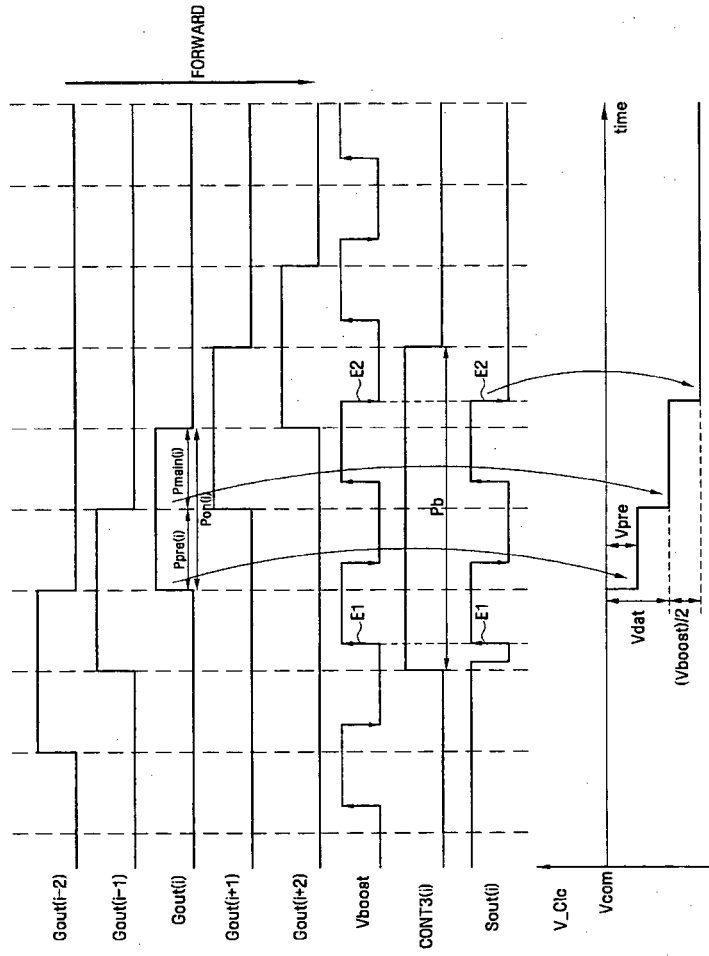


FIG. 11B

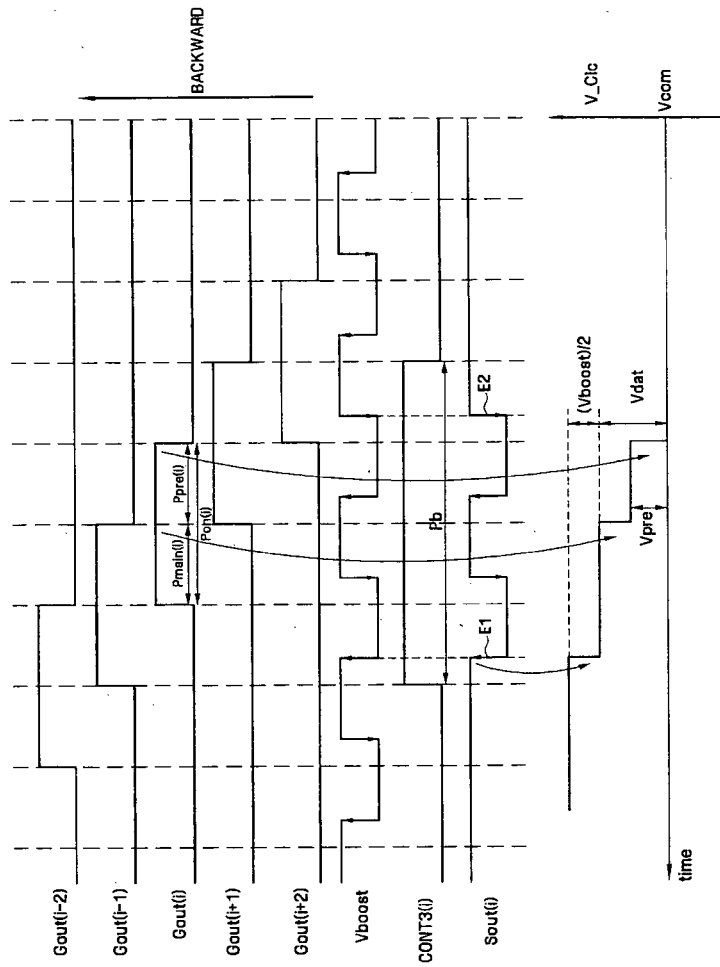


FIG. 12

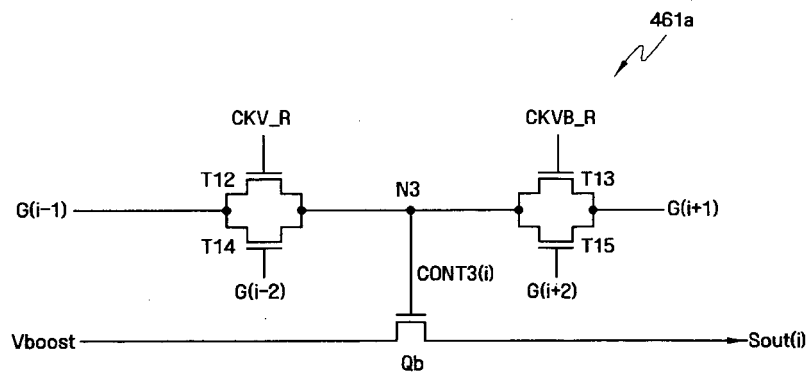
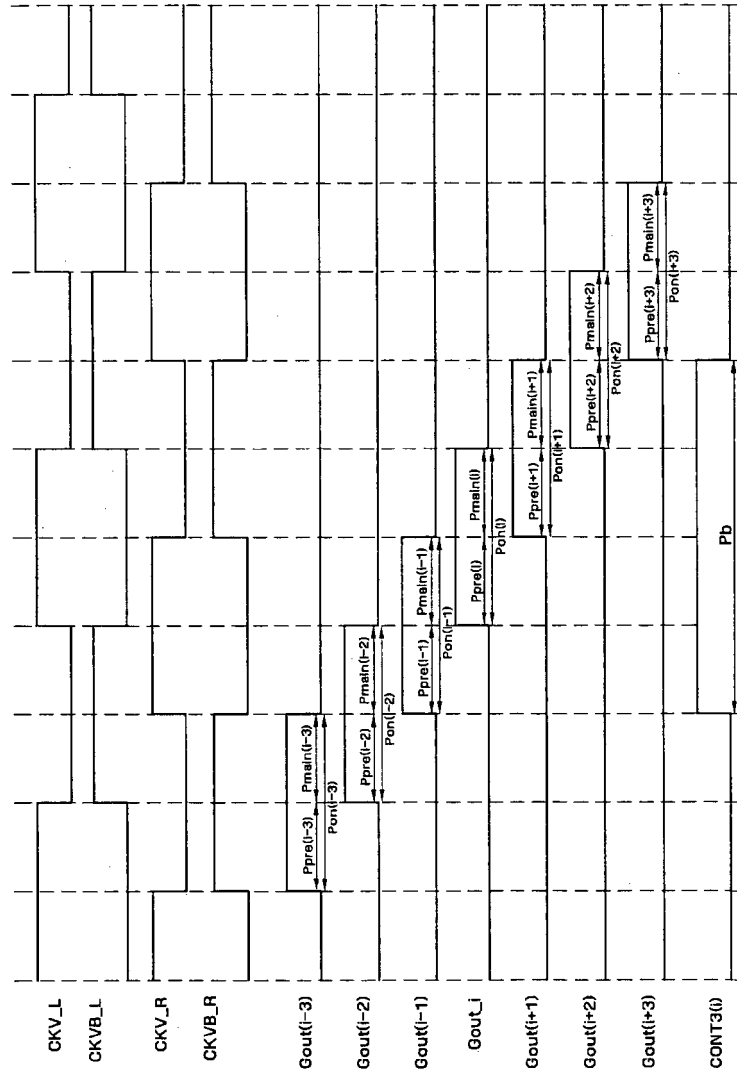


FIG. 13



REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- EP 1241655 A2 [0003]

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外部链接	Espacenet		

摘要(译)

液晶显示器 (LCD) 及其驱动方法。 LCD 包括在第一栅极信号的第一导通时段期间充电数据电压的液晶电容器 (C_{lc}) , 具有连接到液晶电容器的一个电极的存储电容器 (C_{st}) 和驱动单元 (Q_b) 其在升压控制信号 (CONT3) 的升压电压输出时段期间向存储电容器的另一电极提供升压电压 (V_{boost}) 。升压电压具有第一边沿和第二边沿, 第一和第二边沿出现在升压电压输出时段中, 并且第一导通时段出现在第一和第二边沿之间。

