(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) **EP 1 890 188 B1**

(12) **EUROPEAN PATENT SPECIFICATION**

(45) Date of publication and mention of the grant of the patent:
24.10.2018 Bulletin 2018/43

(51) Int Cl.:
G02F 1/1362 *(2006.01)*

(21) Application number: **07015869.6**

(22) Date of filing: **13.08.2007**

(54) **Liquid crystal display panel having floating electrode**

Flüssigkristallanzeigetafel mit schwebender Elektrode

Panneau d'affichage à cristaux liquides doté d une électrode flottante

(84) Designated Contracting States:
DE FR GB NL

(30) Priority: **16.08.2006 KR 20060077135**
26.10.2006 KR 20060104553

(43) Date of publication of application:
20.02.2008 Bulletin 2008/08

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US-A1- 2004 263 710
US-B1- 6 525 788

EP 1 890 188 B1

Printed by Jouve, 75001 PARIS (FR)

Description

[0001] This application claims priority to Korean Patent Application Nos. 10-2006-0077135, and 10-2006-0104553, filed on August 16, 2006, and October 26, 2006, respectively, and all the benefits accruing therefrom under 35 U.S.C. §119.

BACKGROUND OF THE INVENTION

Field of the Invention

[0002] The present invention relates to a liquid crystal display (LCD) panel, and more particularly, the present invention relates to a LCD panel having improved image quality.

Description of the Related Art

[0003] A liquid crystal display (LCD) panel comprises a pair of opposing substrates with a liquid crystal layer therebetween. One of the substrate is a common electrode substrate having a common electrode while the other substrate is a thin film transistor (TFT) substrate having a plurality of TFTs. The common electrode substrate and the TFT substrate are assembled by a seal line disposed at the edge of both the common electrode substrate and the TFT substrate. The liquid crystal layer is disposed between the common electrode substrate and the TFT substrate. Liquid crystal molecules of the liquid crystal layer are arranged in accordance with the electricity given to the common electrode substrate and TFT substrate respectively.

[0004] The TFT substrate has a plurality of gate lines, a plurality of data lines and a plurality of pixels. Each of the gate lines extends horizontally and transmits gate signals. On the other hand, each of the data lines extends vertically and transmits data signals. Each of the pixels may be defined by one gate line and one data line and has a switching element and a storage capacitor.

[0005] A switching element may be formed near the cross point of one gate line and one data line. The switching element is a thin film transistor (TFT) with a gate electrode connected to the gate line, source electrode connected to the data line and drain electrode connected to a pixel electrode. The drain electrode may be electrically connected to a liquid crystal capacitor and to a storage capacitor.

[0006] Not being a self-emitting display device, an LCD module has a backlight unit behind the LCD panel that provides light to the LCD panel. With light provided from the backlight unit, transmittance of the LCD panel is controlled by arrangement of the liquid crystal molecules of each pixel by selectively passing light to a display image.

[0007] With the conventional LCD module of the above structure, light is apt to leak in the gap between the data line and pixel electrode to make poor image quality. Thus, to lessen the light leakage, a black matrix is generally adapted on the common electrode substrate. Specifically, the black matrix is located where the leaked light passes. However, the black matrix may result in a smaller aperture ratio of the overall LCD module to decrease the luminance of the display resulting in poor image quality.

[0008] Also, with the conventional LCD module, data signals and pixel electrodes may influence each other. Namely, charge coupling between the data line and pixel electrode can occur causing irregular vertical crosstalk along the data line.

[0009] US6525788 discloses the features of the preamble of the independent claim.

BRIEF SUMMARY OF THE INVENTION

[0010] Accordingly, it is an aspect of the present invention to provide a LCD module with less light leakage and charge coupling between the data line and pixel electrode to enhance image quality of LCD module.

[0011] The foregoing and/or other aspects of the present invention are achieved by providing an LCD according to the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] The above and/or other aspects and advantages of the present invention will become apparent and more readily appreciated from the following description of the exemplary embodiments, taken in conjunction with the accompanying drawings of which:

FIG. 1A is a layout of a pixel of a thin film transistor (TFT) substrate of an exemplary embodiment according to the present invention;

FIG. 1B is a cross-sectional view of a pixel taken along a line Ib - Ib' of the exemplary embodiment of FIG. 1A according to the present invention;

FIG. 1C is a cross-sectional view of a pixel taken along a line Ic - Ic' of the exemplary embodiment of FIG. 1A according to the present invention;

FIG. 1D is a layout of a floating electrode formed on the TFT substrate of the exemplary embodiment of FIG. 1A according to the present invention;

FIG. 2 is a layout of a pixel of a common electrode substrate of an exemplary embodiment according to the present invention;

FIG. 3A is a combined layout of a pixel of a liquid crystal display (LCD) panel which is an assembly of the TFT substrate of FIG. 1A and common electrode substrate of FIG. 2 of an exemplary embodiment according to the present invention;

FIG. 3B is a cross-sectional view of the pixel taken along a line IIIb - IIIb' of the exemplary embodiment of FIG. 3A according to the present invention;

FIG. 4 is a simplified overall layout of the TFT substrate of the exemplary embodiment according to the present invention;

FIG. 5A is a layout of a pixel of a TFT substrate of

an exemplary embodiment according to the present invention;

FIG. 5B is a layout of a floating pattern formed on the TFT substrate of the exemplary embodiment of FIG. 5A according to the present invention;

FIG. 6A is a layout of a pixel of a TFT substrate of an exemplary embodiment according to the present invention;

FIG. 6B is a cross-sectional view of a pixel taken along a line VIb - VIb' of the exemplary embodiment of FIG. 6A according to the present invention;

FIG. 6C is a layout of a floating pattern formed on the TFT substrate of the exemplary embodiment of FIG. 6A according to the present invention;

FIG. 7A is a layout of a pixel of a TFT substrate of an exemplary embodiment according to the present invention;

FIG. 7B is a cross-sectional view of a pixel taken along a line VIIb - VIIb' of the exemplary embodiment of FIG. 7A according to the present invention;

FIG. 7C is a layout of a floating pattern and a bridge electrode formed on the TFT substrate of the exemplary embodiment of FIG. 7A according to the present invention;

FIG. 7D is a simplified overall layout of the TFT substrate of the exemplary embodiment of FIG. 7A according to the present invention;

FIG. 8A is a layout of a pixel of a TFT substrate of an exemplary embodiment according to the present invention;

FIG. 8B is a layout of a floating pattern and a bridge electrode formed on the TFT substrate of the exemplary embodiment of FIG. 8A according to the present invention;

FIG. 9A is a layout of a pixel of a TFT substrate of an exemplary embodiment according to the present invention;

FIG. 9B is a layout of a floating pattern and a bridge electrode formed on the TFT substrate of the exemplary embodiment of FIG. 9A according to the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0013] Reference will now be made in detail to exemplary embodiments of the present invention, examples of which are illustrated in the accompanying drawings, wherein like reference numerals refer to like elements throughout. The embodiments are described below in order to explain the present invention by referring to the figures.

[0014] The LCD panel shown in FIGS. 1A through 4 is explained according to one embodiment of the invention. The LCD panel includes a TFT substrate, a common electrode substrate and a liquid crystal layer disposed inbetween the TFT substrate and the common electrode substrate. The TFT substrate includes a plurality of gate lines, a plurality of data lines, and a plurality of TFTs electrically connected to the gate line and the data line to transmit voltage to a pixel electrode. The common electrode substrate faces the TFT substrate and includes a common electrode to control the liquid crystal layer.

[0015] FIG. 1A is a layout of a pixel of the TFT substrate. FIG. 1B is a cross-sectional view of a pixel taken along a line Ib - Ib' of FIG. 1A. FIG. 1C is a cross-sectional view of a pixel taken along a line Ic - Ic' of FIG. 1A. At last, FIG. 1D is a layout of a floating electrode formed on the TFT substrate of FIG. 1A.

[0016] On insulating substrate 10, a gate wiring which comprises a gate line 22 and gate electrode 26 projected from gate line 22 is formed. The floating electrode 21 is formed on the insulation substrate 10 and arranged in horizontal direction with vertically extending light blocking pattern 21a near the data line 62. The floating electrode 21 of each pixel is, throughout the TFT substrate, interconnected to each other and electrically isolated from external voltage source of the TFT substrate. Alternatively, the interconnected floating electrode 21 throughout the TFT substrate is give a predetermined voltage as long as the floating electrode is effective for vertical crosstalk.

[0017] Specifically, floating electrode 21 comprises a light blocking pattern 21a, intra-pixel connection pattern 21b, and inter-pixel connection pattern 21c. The light blocking pattern 21a is located along the data line 62 to prevent light leakage between the data line 62 and a pixel electrode 82. The light blocking pattern 21a may or may not overlap with data line 62. Also, light blocking pattern 21a may or may not overlap with pixel electrode 82.

[0018] A plurality of light blocking patterns 21a may be formed within one pixel. Thus, because every pixel may have the same or similar structure within one horizontal line of the TFT substrate, every pixel may have a plurality of light blocking patterns 21a. Here, a plurality of light blocking patterns 21a is connected by an intra-pixel connection pattern 21b of floating electrode 21. Similarly, different pixel's light blocking patterns 21a are connected by an inter-pixel connection pattern 21c of floating, electrode 21.

[0019] Thus, every light blocking pattern 21a is electrically connected by inter-pixel connection patterns 21c and intra-pixel connection patterns 21b within one horizontal line along gate line 22. On the other hand, the whole floating electrode 21 is not electrically connected to external voltage source.

[0020] For designing of storage capacitance of the LCD module, previous capacitance type and independent capacitance line type has been introduced. Previous capacitance type uses storage capacitance by overlapping pixel electrode 82 and previous gate's extended width, whereas independent capacitance line type uses storage capacitance by overlapping pixel electrode 82 and specially added common voltage (Vcom) line of the same gate metal., Even though the present invention is shown with previous capacitance type, the independent capacitance line type may also be used within the scope

of the present invention.

[0021] On the TFT substrate, gate wiring 22, 26 and floating electrode 21 may include at least one of Al, Al alloy, Ag, Ag alloy, Cu, Cu alloy, Mo, Mo alloy, Cr, Ti and Ta. Gate wiring 22, 26 and floating electrode 21 may have a multi-layered structure with conductive layers of different physical characteristics. At least one of the multi-layered structures may be a low resistivity conductive metal of Al, Al alloy, Ag, Al alloy, Cu, or Cu alloy to reduce signal delay or voltage drop of the gate wiring 22, 26 and floating electrode 21. On the contrary, at least one layer of the multi-layered structure may be Indium Tin Oxide (ITO) or Indium Zinc Oxide (IZO) friendly material such as Mo, Mo alloy, Cr, Ti, or Ta. Exemplary combinations of low resistivity and good contact characteristics are either lower layer of Cr and upper layer of Al or lower layer of Al and upper layer of Mo. However, the gate wiring and floating electrode material is not limited to the already introduced examples and may be any combination of various conductive materials.

[0022] On the gate wiring and floating electrode 21, a gate insulating layer 30 is formed with insulating material such as SiNx. On the gate insulating layer 30, semiconductor layer 40 is formed with material such as hydrogenated amorphous silicon or poly-silicon. The semiconductor layer 40 may be either line pattern or isolated pattern. The isolated pattern semiconductor layer is formed on the gate line 22 as shown in the present invention while the line pattern semiconductor layer may be formed under the data line 62 and extends to the gate line 22 with data line's 62 shape.

[0023] On the semiconductor layer 40, resistive contact layer 55, 56 is formed with highly doped hydrogenated amorphous silicon or silicide. The resistive contact layer 55, 56 may be either line pattern or isolated pattern. For example, isolated pattern resistive contact layer can be located under the source and drain electrode as in the present invention, whereas the line pattern resistive contact layer may extend under the data line 62.

[0024] On the resistive contact layer 55, 56 and gate insulation layer 30, data line 62, source electrode 65 and drain electrode 66 are formed. Data line 62 extends vertically to cross the gate line 22. Source electrode 65 is projected from the data line 62 and extends to the semiconductor layer 40 while drain electrode 66 on the semiconductor layer is separated from and facing the source electrode 65 with gate electrode 26 in the middle. The TFT consists of the gate electrode 22, source electrode 65 and drain electrode 66 and transmits electricity from source electrode 65 to drain electrode 66 when gate electrode 26 receives gate voltage.

[0025] Drain electrode 66 includes a bar type pattern on the semiconductor layer 40 and an extensive area that is elongated from the bar type pattern with contact hole 76. The data line 62, source electrode 65 and drain electrode 66 are collectively called data wiring.

[0026] Further, a capacitance electrode 67 of the same material and layer with data line 62 may be formed to overlap the previous gate line 22 by being electrically connected with the pixel electrode 82 via contact hole 77. The combination of capacitance electrode 67, previous gate line 22 and intervening gate insulation layer 30 can store capacitance of the liquid crystal layer.

[0027] Data wiring and the capacitance electrode 67 may be either a single layer or multi-layer including at least one of Al, Cr, Mo, Ta and Ti. For example, data wiring and capacitance electrodes may be a multi layer of Cr, Mo based material, Ta or Ti in one layer with a lower layer of Cr, Mo based material, Ta or Ti and an upper layer of low resistivity. More specifically, a lower layer of Cr and upper layer of Al, a lower layer of Al and upper layer of Mo, or a lower layer of Mo, middle layer of Al and upper layer of Mo may be used as the multi layered data wiring and capacitance electrode.

[0028] In the TFT, the confronting source electrode 65 and drain electrode 66 at least partially overlap with both gate electrode 26 and semiconductor layer 40 to transmit pixel driving voltage. Additionally, resistive contact layer 55, 56 is sandwiched between a semiconductor layer and either the source electrode 65 or the drain electrode 66 to reduce contact resistance.

[0029] On the data wiring 62, 65, 66, storage capacitance conductor 67 and exposed semiconductor layer 40, a passivation layer 70 are disposed. The passivation layer may be made of various materials such as inorganic material, organic material, or insulating material with a low dielectric constant. Here, inorganic material can be either SiNx or SiOx while organic material may be photosensitive and used for making a flat surface. Insulating material with a low dielectric constant is disposed by plasma enhanced chemical vapor deposition (PECVD) and can be either a-Si:C:O or a-Si:O:F. More than two different materials can be used for passivation layer 70. For example, when organic material is applied, an additional bottom layer of inorganic material can be used to prevent the organic material's direct contact with exposed semiconductor layer of TFT. Contact holes 76, 77 are formed to partially uncover either a drain electrode 66 or storage capacitance electrode 67. On the passivation layer, pixel electrode 82 is formed along the inner line of each pixel. The pixel electrode 82 is electrically connected to the drain electrode 66 via drain electrode contact hole 76. Further, pixel electrode 82 is electrically connected to the storage capacitance electrode 67 via storage capacitance electrode contact hole 77.

[0030] Thus, pixel electrode 82 with a pixel driving voltage can control the arrangement of liquid crystal molecules by causing electric field in cooperation with the common electrode 90 of the common electrode substrate. Here, pixel electrode 82 is made of either transparent conductive material such as Indium Tin Oxide (ITO) and Indium Zinc Oxide (IZO) or reflective conductive material such as Al. On the pixel electrode 82 or passivation layer 70, an orientation layer (not shown) may be disposed to setup a basic orientation of the liquid crystal molecules.

[0031] Now, referring to FIGS. 1A, 1C, and 1D, floating electrode 21 is explained in detail. In FIG. 1A, floating electrode 21 extends along data line 62 with at least a partially overlapping relationship. In addition, a part of pixel electrode closest to the data line overlaps with the floating line, too. More specifically, light blocking pattern 21a of floating electrode 21 is disposed along the data line 62 and partially overlaps with a portion of pixel electrode 82. Further, inter-pixel connection electrode 21c partially overlaps with data line 62.

[0032] From here, the light blocking electrode's function is explained. Liquid crystal molecules around the data line may be undesirably arranged because the electric field from data line 62 is more dominant than the electric field from the pixel electrode. Therefore, light around the data line passes in a wrong direction and light leakage can be seen outside of the LCD panel. However, wrongly directed light can be screened by a pattern around the data line. In FIG. 1A, light blocking pattern 21a screens the wrongly directed light and prevents light leakage.

[0033] However, the floated light blocking electrode 21a may be electrically coupled to data line 62 and may cause irregular vertical crosstalk of LCD panel. To solve this potential problem, in the current embodiment, each of the light blocking patterns 21a is electrically interconnected to a neighboring light blocking electrode 21a by inter-pixel connection pattern 21c and intra-pixel connection pattern 21b. Now, because the unified floating electrode is not influenced or coupled by or to a specific data line, irregular vertical crosstalk may not be seen.

[0034] If the unified floating electrode 21 passes a common voltage, liquid crystal molecules around the data line may experience an undesired electric field and be arranged incorrectly because it is being influenced by a common voltage rather than pixel electrode's voltage. Thus, floating electrode 21 is electrically independent from any other voltage to prevent light leakage.

[0035] In FIG. 2, a layout of a pixel of a common electrode substrate is introduced according to one embodiment of the present invention. Additionally, in FIG. 3A, a layout of a pixel of an assembled LCD panel with a TFT substrate, common electrode substrate and liquid crystal layer is introduced. Further, FIG. 3B shows a cross-sectional view of the LCD panel taken along a line IIIb-IIIb' of FIG. 3A.

[0036] Throughout FIGS. 2, 3A and 3B, a black matrix 94 is formed on a transparent glass substrate 96. Black matrix 94 is also disposed around each of the pixels to prevent undesired light's transmitting. Black matrix 94 may be made of at least one such as Cr, metal oxide such as CrOx and organic material.

[0037] In the light passing area between neighboring black matrix 94, color filter 98 is disposed to transmit red, green or blue light. An additional overcoat layer (not shown) may be formed on the color filter layer 98 and black matrix 94 to cover an uneven color filter layer and make one flat surface. Finally, on either color filter layer 98 or overcoat layer, transparent common electrode layer 90 of ITO or IZO is formed. A supplemental orientation layer (not shown) may be coated on the common electrode layer 90 to align liquid crystal molecules around the common electrode 90.

[0038] As shown in FIG. 3B, the LCD panel has a liquid crystal layer 300 and combined TFT substrate 100 and common electrode substrate 200. In assembling, color filter 98 of common electrode substrate 200 is aligned to overlap almost exactly with pixel electrode 82 of TFT substrate 100. Then the LCD panel is completed by perpendicularly attaching a pair of polarizers on the outer surface of TFT substrate 100 and common electrode substrate 200. Finally, the LCD module is completed by assembling the LCD panel, a backlight unit behind the LCD panel and frames encompassing the LCD panel and backlight unit.

[0039] Referring to FIG. 4, floating electrode FP is explained in detail. In FIG. 4, the TFT substrate has a plurality of horizontally extending gate lines (G1, G2... Gn), a plurality of vertically extending data lines (D1, D2... Dm) and a plurality of pixels PX defined by each of gate lines and data lines. Throughout the whole LCD panel, each and every of the floating electrodes (FP) is interconnected between pixels in one horizontal line along each gate line and each of the horizontal lines' end points are interconnected to each other. Further, a whole floating electrode is isolated from external voltage source.

[0040] Referring to FIGS. 5A and 5B, another embodiment of present invention is explained. FIG. 5A is a layout of one pixel of the TFT substrate of the present embodiment, while FIG. 5B is a layout of a floating electrode of FIG. 5A. For a brief explanation, the same elements shown in FIGS. 1 through 4 are expressed with the same reference numeral and corresponding explanations will be omitted. Basically, every element other than the floating electrode in FIGS. 5A and 5B is the same with the corresponding element in FIGS. 1 through 4.

[0041] In FIGS. 5A and 5B, a pair of floating electrode's light blocking pattern 21a is interconnected by a plurality of inter-pixel connection patterns 21c. At this point, even though FIGS. 5A and 5B show two inter-pixel connection patterns, the number of inter-pixel connection patterns may be more than two.

[0042] With more than two inter-pixel connection patterns 21c, more overlap area between data line 62 and floating electrode 21 can be obtained.

[0043] The enlarged overlap area can contribute in reducing the possible overlay difference between neighboring light blocking patterns 21a of floating electrodes 21 of different pixels. Then, the reduced overlay difference may contribute in overcoming the coupling capacitance difference of each data line and each of the light blocking patterns 21a. Thus, irregular vertical crosstalk can be less recognized by a viewer.

[0044] When a semiconductor layer is extended beneath data line 62, the enlarged overlap area between data line 62 and light blocking pattern 21a can be even more efficient for image quality. In detail, light entering

the data line 62 area can induce unwanted photo current to damage image quality because a photo sensitive semiconductor layer is beneath data line 62. However, with enlarged inter-pixel connection pattern 21c, the photo current can be suppressed as floating electrode 21 is formed with gate wirings to block light from entering data line 62. Accordingly, image quality can be enhanced.

[0045] Referring to FIGS. 6A through 6C, another embodiment of this invention is explained. FIG. 6A is a layout of one pixel of the TFT substrate of the present embodiment while FIGS. 6B and 6C are cross-sectional views of a pixel taken along a line VIb - Vib' of FIG. 6A and layout of floating electrode of FIG. 6A respectively. For a brief explanation, the same elements shown in FIGS. 5A and 5B are expressed with the same reference numerals and corresponding explanations will be omitted. Basically, every element other than the floating electrode in FIGS. 6A through 6C is the same as the corresponding, element in FIGS. 5A and 5B.

[0046] Specifically, floating electrode 221 of FIGS. 6A through 6C consists of a light blocking pattern 221a overlapping data line 62 and inter-pixel connection pattern 21b connecting a pair of light blocking patterns 221a within one pixel. More specifically, light blocking pattern 221a may be wide enough to fully overlap in at least one horizontal direction with data line 62. Further, light blocking pattern 221a may be widened to partially overlap with a pair of pixel electrodes 82 next to one data line 62. Similar to the embodiment of FIGS. 5A and 5B, the semiconductor layer may be under the data line 62. Consequently, the widened light blocking pattern 221a may lessen the recognition of vertical crosstalk and photo leakage occurring on the semiconductor layer beneath the data line 62.

[0047] Referring to FIGS. 7A through 7D, another embodiment of this invention is explained. FIG. 7A is a layout of one pixel of the TFT substrate of the present embodiment while FIGS. 7B and 7C are cross-sectional views of a pixel taken along a line VIIb - VIIb' of FIG. 7A and a layout of the floating electrode and bridge electrode of FIG. 7A respectively. For more explanation, FIG. 7D shows a simplified LCD panel of this embodiment. To make the explanation brief, the same elements shown in FIGS. 1A through 4 are expressed with the same reference numerals and corresponding explanations will be omitted. Basically, every element other than the bridge electrode in FIGS. 7A through 7D is the same as the corresponding element in FIGS. 1A through 4.

[0048] In this embodiment of FIGS. 7A through 7D, a vertically extending bridge electrode 84 electrically connects different pixel's different floating electrodes 21. More specifically, bridge electrode 84 electrically connects the intra-pixel connecting pattern 21b of one pixel and light blocking pattern 21a of the other pixel.

[0049] In FIGS. 7B and 7C, floating electrodes 21a under passivation layer 30 of two neighboring pixels are partially exposed to bridge electrode 84 for electrical connection. In this embodiment, bridge electrode 84 may be the same material with pixel electrode 82 on the same layer.

[0050] With the simplified LCD panel of FIG. 7D, floating electrode FP covers all the pixels PX of the TFT substrate which are inter connected to each other while the floating electrode is isolated from outer circuits. More specifically, floating electrode FP is formed on every row of pixels to extend in parallel with the gate lines of the TFT substrate. Each end portions of respective floating electrodes are connected to each other. Finally, respective floating electrodes are electrically connected to each other within the image display area by bridges extended in the data line direction.

[0051] Consequently, every floating electrode within the display area of the panel bears uniform floating potential all over the TFT panel because horizontally extending floating electrodes are vertically connected by vertically extending bridge electrodes. Evenly distributed floating potential can prevent uneven coupling between data lines and floating electrodes of each pixel to minimize irregular vertical crosstalk by suppressing differently coupled potential between data lines and pixel electrodes of each pixel.

[0052] Referring to FIGS. 8A and 8B, another embodiment of this invention is explained. FIG. 8A is a layout of one pixel of the TFT substrate of the present embodiment; FIG. 8B is a layout of the floating electrode and bridge electrode of FIG. 8A. For a brief explanation, the same elements shown in FIG. 7A through FIG. 7D are expressed with the same reference numeral and corresponding explanations will be omitted. Basically, every element other than the shape of the floating electrode in FIGS. 8A and 8B is the same as the corresponding element in FIGS. 7A through 7D.

[0053] The floating pattern of FIGS. 8A and 8B has a pair of light blocking patterns 21a with one data line in-between and an inter-pixel connection pattern 21c which connects the pair of light blocking patterns 21a. Here, the number of inter-pixel connecting pattern may be more than one although FIGS. 8A and 8B shows one inter-pixel connection pattern.

[0054] With the enlarged overlap area between floating electrode 21 and data line 62, the coupling capacitance difference between each light blocking pattern 21a of floating electrode and data line 62 can be reduced when each light blocking pattern 21a does not have the same overlay with data line 62. Consequently, irregular vertical crosstalk is less recognized.

[0055] If the semiconductor layer is extended to beneath the data line 62, photo leakage may be incurred by the light entering the semiconductor layer from backlight and cause poor image quality. However, the enlarged overlap area of this embodiment can screen light entering the semiconductor layer and enhance the image quality.

[0056] Referring FIGS. 9A and 9B, another embodiment of this invention is explained. FIG. 9A is a layout of one pixel of a TFT substrate of present embodiment; FIG.

9B is a layout of the floating electrode and bridge electrode of FIG. 9A. For brief explanation, the same elements shown in FIG. 8A through FIG. 8B are expressed with the same reference numeral and corresponding explanations will be omitted. Basically, every element other than the shape of floating electrode in FIGS. 9A and 9B is the same as the corresponding element in FIGS. 8A and 8B.

[0057] The floating electrode 21 of FIGS. 9A and 9B comprises a light blocking pattern 21a overlapping with data line 62 and an intra-pixel connecting pattern 21b. The light blocking pattern 21a may be wide enough to fully cover the data line 62 with a bigger width than the data line's width at least in one horizontal direction. The light blocking pattern 21a may be also partially overlapped with pixel electrodes 82 disposed along with data line 62.

[0058] Thus, the enlarged light blocking pattern is effective for controlling irregular vertical crosstalk. Moreover, the enlarged light blocking pattern 21a is even more effective when the TFT substrate has a semiconductor layer under data line 62 because semiconductor layer is apt to cause a photo leakage current which adversely affects image quality.

Claims

1. A liquid crystal display panel comprising:

an insulating substrate (10);
a plurality of gate lines (22; G1, G2, ..., Gn) extending in a first direction on the insulating substrate (10);
a plurality of data lines (62; D1, D2, ..., Dm) extending in a second direction that crosses with the first direction at a cross point to define a pixel;
a thin film transistor formed near the cross point of the gate line (22; G1, G2, ..., Gn) and the data line (62; D1, D2, ..., Dm) and connected to the gate line (22; G1, G2, ..., Gn) and the data line (62; D1, D2, ..., Dm);
a pixel electrode (82) connected to the thin film transistor and disposed within said pixel, wherein the pixel electrode (82) comprising a lower boundary adjacent to the gate line;
a plurality of first light blocking electrodes (21; 221; FP) comprising a first portion (21a) extending in the second direction and substantially parallel to the data line (62; D1, D2, ..., Dm), a second portion (21c) extending in the first direction and across the data line (62; D1, D2, ..., Dm), and a third portion (21b) extending from an area where the first portion (21a) and the second portion (21c) meet each other and extending along at least a first part of the lower boundary of the pixel electrode (82), wherein the third portion (21b) comprises a bent portion, and wherein the first, second and third portions contact one another near a second part of the lower boundary of the pixel electrode;
characterized by
a bridge electrode (84) connecting the first light blocking electrode (21; 221; FP) and a second light blocking electrode, wherein the second light blocking electrode is disposed next to the first light blocking electrode in the second direction.

2. The liquid crystal display panel of claim 1, wherein the third portion (21b) of the first light blocking electrode (21; 221; FP) extends in the first direction within the first pixel, wherein the third portion (21b) connects a plurality of the first portion (21a) positioned within the first pixel.

3. The liquid crystal display panel of claim 2, wherein the first light blocking electrode (21; 221; FP) is disposed and interconnected in a series pixels (PX) of the first direction to form a first light blocking electrode line and a second light blocking electrode line, wherein the first light blocking electrode line and the second light blocking electrode line are in different series of pixels (PX), wherein the first light blocking electrode line has a first end point and a second end point, and wherein the second light blocking electrode line has a third end point and a fourth end point.

4. The liquid crystal display panel of claim 3, wherein the first end point and the third end point are at a first side of the substrate and interconnected and wherein the second end point and the fourth end point are at a second side of the substrate and interconnected.

5. The liquid crystal display panel of claim 4, wherein the first light blocking electrode line and the second light blocking electrode line are electrically disconnected from outer circuits.

6. The liquid crystal display panel of claim 1, wherein the bridge electrode (84) crosses the gate electrode (26).

7. The liquid crystal display panel of claim 1, wherein the third pixel has a first contact hole (79) exposing the first portion (21a) of the first light blocking electrode (21; 221; FP) and wherein the fourth pixel has a second contact hole (78) exposing the third portion (21b) of the first light blocking electrode (21; 221; FP).

8. The liquid crystal display panel of claim 1, wherein the bridge electrode (84) is the same layer with pixel electrode (82).

9. The liquid crystal display panel of claim 1, wherein

the first portion (21a) blocks light leakage in the gap between the data line (62; D1, D2, ..., Dm) and the pixel electrode (82) of the first pixel.

10. The liquid crystal display panel of claim 9, wherein the first portion (21a) of the first light blocking electrode (21; 221; FP) is at least partially overlapping the data line (62; D1, D2, ..., Dm).

11. The liquid crystal display panel of claim 9, wherein the first portion (21a) of the first light blocking electrode (21; 221; FP) is partially overlapping the pixel electrode (82).

12. The liquid crystal display panel of claim 2 comprising: wherein the first portion (21a) of the first light blocking electrode (21; 221; FP) comprises a light blocking pattern extending along the data line (62; D1, D2, ..., Dm) and the second and third portion (21c; 21b) of the first light blocking electrode (21; 221; FP) comprises an intra-pixel connection pattern, wherein the intra-pixel connection pattern connects a plurality of light blocking pattern within one pixel.

13. The liquid crystal display panel of claim 12, wherein the light blocking pattern (21a) has a first width wider than the width of the data line (62; D1, D2, ..., Dm) in the first direction.

14. The liquid crystal display panel of claim 13, wherein the light blocking pattern (21a) fully overlaps the data line (62; D1, D2, ..., Dm) of a fifth pixel.

15. The liquid crystal display panel of claim 14, wherein the light blocking pattern (21a) partially overlaps the pixel electrode (82).

16. The liquid crystal display panel of claim 12, wherein the bridge electrode (84) connects a light blocking pattern (21a) of a sixth pixel and a intra-pixel connection pattern (21b; 21c) of a seventh pixel next to the sixth pixel in the second direction.

17. The liquid crystal display panel of claim 16, the bridge electrode (84) is the same layer with the pixel electrode (82).

18. The liquid crystal display panel of claim 12, wherein the first light blocking electrodes (21; 221; FP) are electrically connected with each other within a display area, wherein the display area is for effective image display.

19. The liquid crystal display panel of claim 12, wherein the first light blocking electrode (21; 221; FP) is electrically disconnected from external circuits.

20. The liquid crystal display of clam 12, wherein the first light blocking electrode (21; 221; FP) is the same layer with gate line (22; G1, G2, ..., Gn).

Patentansprüche

1. Flüssigkristallanzeigetafel, umfassend:

ein isolierendes Substrat (10);
eine Vielzahl von Gate-Leitungen (22; G1, G2,..., Gn), die sich in eine erste Richtung auf dem isolierenden Substrat (10) erstrecken;
eine Vielzahl von Datenleitungen (62; D1, D2,..., Dm), die sich in eine zweite Richtung erstrecken, die die erste Richtung an einem Kreuzungspunkt kreuzt, um ein Pixel zu definieren;
einen Dünnfilmtransistor, der in der Nähe des Kreuzungspunktes der Gate-Leitung (22; G1, G2,..., Gn) und der Datenleitung (62; D1, D2,..., Dm) gebildet und mit der Gate-Leitung (22; G1, G2,..., Gn) und der Datenleitung (62; D1, D2,..., Dm) verbunden ist;
eine Pixelelektrode (82), die mit dem Dünnfilmtransistor verbunden und innerhalb des Pixels angeordnet ist, wobei die Pixelelektrode (82) eine untere Begrenzung benachbart zu der Gate-Leitung umfasst;
eine Vielzahl von ersten Lichtblockierungselektroden (21; 221; FP), umfassend einen ersten Abschnitt (21a), der sich in die zweite Richtung und im Wesentlichen parallel zu der Datenleitung (62; D1, D2,..., Dm) erstreckt, einen zweiten Abschnitt (21c), der sich in die erste Richtung und quer durch die Datenleitung (62; D1, D2,..., Dm) erstreckt, und einen dritten Abschnitt (21b), der sich von einem Bereich, in dem der erste Abschnitt (21a) und der zweite Abschnitt (21c) aufeinandertreffen, erstreckt und sich entlang zumindest einem ersten Teil der unteren Begrenzung der Pixelelektrode (82) erstreckt, wobei der dritte Abschnitt (21b) einen gebogenen Abschnitt umfasst und wobei der erste, zweite und dritte Abschnitt einander in der Nähe eines zweiten Teils der unteren Begrenzung der Pixelelektrode kontaktieren;
gekennzeichnet durch
eine Brückenelektrode (84), die die erste Lichtblockierungselektrode (21; 221; FP) und eine zweite Lichtblockierungselektrode verbindet, wobei die zweite Lichtblockierungselektrode neben der ersten Lichtblockierungselektrode in der zweiten Richtung angeordnet ist.

2. Flüssigkristallanzeigetafel nach Anspruch 1, wobei sich der dritte Abschnitt (21b) der ersten Lichtblockierungselektrode (21; 221; FP) in die erste Richtung innerhalb des ersten Pixels erstreckt, wobei der dritte Abschnitt (21b) eine Vielzahl des ersten Ab-

schnitts (21a), der innerhalb des ersten Pixels positioniert ist, verbindet.

3. Flüssigkristallanzeigetafel nach Anspruch 2, wobei die erste Lichtblockierungselektrode (21; 221; FP) in einem Reihenpixel (PX) der ersten Richtung angeordnet und verbunden ist, um eine erste Lichtblockierungselektrodenleitung und eine zweite Lichtblockierungselektrodenleitung zu bilden, wobei die erste Lichtblockierungselektrodenleitung und die zweite Lichtblockierungselektrodenleitung in unterschiedlichen Reihen an Pixeln (PX) sind, wobei die erste Lichtblockierungselektrodenleitung einen ersten Endpunkt und einen zweiten Endpunkt aufweist, und wobei die zweite Lichtblockierungselektrodenleitung einen dritten Endpunkt und einen vierten Endpunkt aufweist.

4. Flüssigkristallanzeigetafel nach Anspruch 3, wobei der erste Endpunkt und der dritte Endpunkt auf einer ersten Seite des Substrats und miteinander verbunden sind und wobei der zweite Endpunkt und der vierte Endpunkt auf einer zweiten Seite des Substrats und miteinander verbunden sind.

5. Flüssigkristallanzeigetafel nach Anspruch 4, wobei die erste Lichtblockierungselektrodenleitung und die zweite Lichtblockierungselektrodenleitung von äußeren Kreisläufen elektrisch getrennt sind.

6. Flüssigkristallanzeigetafel nach Anspruch 1, wobei die Brückenelektrode (84) die Gate-Elektrode (26) kreuzt.

7. Flüssigkristallanzeigetafel nach Anspruch 1, wobei das dritte Pixel ein erstes Kontaktloch (79) aufweist, das den ersten Abschnitt (21a) der ersten Lichtblockierungselektrode (21; 221; FP) freilegt und wobei das vierte Pixel ein zweites Kontaktloch (78) aufweist, das den dritten Abschnitt (21b) der ersten Lichtblockierungselektrode (21; 221; FP) freilegt.

8. Flüssigkristallanzeigetafel nach Anspruch 1, wobei die Brückenelektrode (84) die gleiche Schicht mit der Pixelelektrode (82) ist.

9. Flüssigkristallanzeigetafel nach Anspruch 1, wobei der erste Abschnitt (21a) Lichtlecks in der Lücke zwischen der Datenleitung (62; D1, D2,..., Dm) und der Pixelelektrode (82) des ersten Pixels blockiert.

10. Flüssigkristallanzeigetafel nach Anspruch 9, wobei der erste Abschnitt (21a) der ersten Lichtblockierungselektrode (21; 221; FP) die Datenleitung (62; D1, D2,..., Dm) zumindest teilweise überlappt.

11. Flüssigkristallanzeigetafel nach Anspruch 9, wobei der erste Abschnitt (21a) der ersten Lichtblockierungselektrode (21; 221; FP) die Pixelelektrode (82) teilweise überlappt.

12. Flüssigkristallanzeigetafel nach Anspruch 2, umfassend:
wobei der erste Abschnitt (21a) der ersten Lichtblockierungselektrode (21; 221; FP) ein Lichtblockierungsmuster umfasst, das sich entlang der Datenleitung (62; D1, D2,..., Dm) erstreckt und der zweite und dritte Abschnitt (21c; 21b) der ersten Lichtblockierungselektrode (21; 221; FP) ein Intrapixelverbindungsmuster umfassen, wobei das Intrapixelverbindungsmuster eine Vielzahl von Lichtblockierungsmustern innerhalb eines Pixels verbindet.

13. Flüssigkristallanzeigetafel nach Anspruch 12, wobei das Lichtblockierungsmuster (21a) eine erste Breite aufweist, die breiter ist als die Breite der Datenleitung (62; D1, D2,..., Dm) in die erste Richtung.

14. Flüssigkristallanzeigetafel nach Anspruch 13, wobei das Lichtblockierungsmuster (21a) die Datenleitung (62; D1, D2,..., Dm) eines fünften Pixels vollständig überlappt.

15. Flüssigkristallanzeigetafel nach Anspruch 14, wobei das Lichtblockierungsmuster (21a) die Pixelelektrode (82) teilweise überlappt.

16. Flüssigkristallanzeigetafel nach Anspruch 12, wobei die Brückenelektrode (84) ein Lichtblockierungsmuster (21a) eines sechsten Pixels und ein Intrapixelverbindungsmuster (21b; 21c) eines siebten Pixels neben dem sechsten Pixel in der zweiten Richtung verbindet.

17. Flüssigkristallanzeigetafel nach Anspruch 16, wobei die Brückenelektrode (84) die gleiche Schicht mit der Pixelelektrode (82) ist.

18. Flüssigkristallanzeigetafel nach Anspruch 12, wobei die ersten Lichtblockierungselektroden (21; 221; FP) innerhalb eines Anzeigebereichs elektrisch miteinander verbunden sind, wobei der Anzeigebereich der effektiven Bildanzeige dient.

19. Flüssigkristallanzeigetafel nach Anspruch 12, wobei die erste Lichtblockierungselektrode (21; 221; FP) von externen Kreisläufen elektrisch getrennt ist.

20. Flüssigkristallanzeige nach Anspruch 12, wobei die erste Lichtblockierungselektrode (21; 221; FP) die gleiche Schicht mit der Gate-Leitung (22; G1, G2,..., Gn) ist.

Revendications

1. Ecran d'affichage à cristaux liquides comprenant :

un substrat isolant (10) ;
une pluralité de lignes de grille (22 ; G1, G2, ..., Gn) s'étendant dans une première direction sur le substrat isolant (10) ;
une pluralité de lignes de données (62 ; D1, D2, ..., Dm) s'étendant dans une seconde direction qui croise la première direction en un point de croisement pour définir un pixel ;
un transistor à film mince formé près du point de croisement de la ligne de grille (22 ; G1, G2, ..., Gn) et de la ligne de données (62 ; D1, D2, ..., Dm) et connecté à la ligne de grille (22 ; G1, G2, ..., Gn) et la ligne de données (62 ; D1, D2, ..., Dm) ;
une électrode pixel (82) connectée au transistor à film mince et disposée au sein dudit pixel, dans lequel l'électrode pixel (82) comprend une limite inférieure adjacente à la ligne de grille ;
une pluralité de premières électrodes de blocage de lumière (21 ; 221 ; FP) comprenant une première portion (21a) s'étendant dans la seconde direction et sensiblement parallèle à la ligne de données (62 ; D1, D2, ..., Dm), une deuxième portion (21c) s'étendant dans la première direction et à travers la ligne de données (62 ; D1, D2, ..., Dm), et une troisième portion (21b) s'étendant depuis une zone où la première portion (21a) et la deuxième portion (21c) se rencontrent et s'étendant le long d'au moins une première partie de la limite inférieure de l'électrode pixel (82), dans lequel la troisième portion (21b) comprend une portion courbée, et dans lequel les première, deuxième et troisième portions entrent en contact les unes avec les autres près d'une seconde partie de la limite inférieure de l'électrode pixel ;
caractérisé par
une électrode pont (84) connectant la première électrode de blocage de lumière (21 ; 221 ; FP) et une seconde électrode de blocage de lumière, dans lequel la seconde électrode de blocage de lumière est disposée près de la première électrode de blocage de lumière dans la seconde direction.

2. Ecran d'affichage à cristaux liquides selon la revendication 1, dans lequel la troisième portion (21b) de la première électrode de blocage de lumière (21 ; 221 ; FP) s'étend dans la première direction au sein du premier pixel, dans lequel la troisième portion (21b) connecte une pluralité de la première portion (21a) positionnée au sein du premier pixel.

3. Ecran d'affichage à cristaux liquides selon la revendication 2, dans lequel la première électrode de blocage de lumière (21 ; 221 ; FP) est disposée et interconnectée dans une série de pixels (PX) de la première direction pour former une première ligne d'électrode de blocage de lumière et une seconde ligne d'électrode de blocage de lumière, dans lequel la première ligne d'électrode de blocage de lumière et la seconde ligne d'électrode de blocage de lumière sont dans des séries de pixels (PX) différentes, dans lequel la première ligne d'électrode de blocage de lumière a un premier point d'extrémité et un deuxième point d'extrémité, et dans lequel la seconde ligne d'électrode de blocage de lumière a un troisième point d'extrémité et un quatrième point d'extrémité.

4. Ecran d'affichage à cristaux liquides selon la revendication 3, dans lequel le premier point d'extrémité et le troisième point d'extrémité sont d'un premier côté du substrat et interconnectés et dans lequel le deuxième point d'extrémité et le quatrième point d'extrémité sont d'un second côté du substrat et interconnectés.

5. Ecran d'affichage à cristaux liquides selon la revendication 4, dans lequel la première ligne d'électrode de blocage de lumière et la seconde ligne d'électrode de blocage de lumière sont déconnectées électriquement de circuits extérieurs.

6. Ecran d'affichage à cristaux liquides selon la revendication 1, dans lequel l'électrode pont (84) croise l'électrode grille (26).

7. Ecran d'affichage à cristaux liquides selon la revendication 1, dans lequel le troisième pixel a un premier trou de contact (79) exposant la première portion (21a) de la première électrode de blocage de lumière (21 ; 221 ; FP) et dans lequel le quatrième pixel a un second trou de contact (78) exposant la troisième portion (21b) de la première électrode de blocage de lumière (21 ; 221 ; FP).

8. Ecran d'affichage à cristaux liquides selon la revendication 1, dans lequel l'électrode pont (84) est dans la même couche que l'électrode pixel (82).

9. Ecran d'affichage à cristaux liquides selon la revendication 1, dans lequel la première portion (21a) bloque une fuite de lumière dans l'écartement entre la ligne de données (62 ; D1, D2, ..., Dm) et l'électrode pixel (82) du premier pixel.

10. Ecran d'affichage à cristaux liquides selon la revendication 9, dans lequel la première portion (21a) de la première électrode de blocage de lumière (21 ; 221 ; FP) chevauche au moins partiellement la ligne de données (62 ; D1, D2, ..., Dm).

11. Ecran d'affichage à cristaux liquides selon la revendication 9, dans lequel la première portion (21a) de la première électrode de blocage de lumière (21 ; 221 ; FP) chevauche partiellement l'électrode pixel (82).

12. Ecran d'affichage à cristaux liquides selon la revendication 2,
dans lequel la première portion (21a) de la première électrode de blocage de lumière (21 ; 221 ; FP) comprend un motif de blocage de lumière s'étendant le long de la ligne de données (62 ; D1, D2, ..., Dm) et les deuxième et troisième portions (21c ; 21b) de la première électrode de blocage de lumière (21 ; 221 ; FP) comprennent un motif de connexion intra-pixel, dans lequel le motif de connexion intra-pixel connecte une pluralité de motifs de blocage de lumière au sein d'un pixel.

13. Ecran d'affichage à cristaux liquides selon la revendication 12, dans lequel le motif de blocage de lumière (21a) a une première largeur supérieure à la largeur de la ligne de données (62 ; D1, D2, ..., Dm) dans la première direction.

14. Ecran d'affichage à cristaux liquides selon la revendication 13, dans lequel le motif de blocage de lumière (21a) chevauche totalement la ligne de données (62 ; D1, D2, ..., Dm) d'un cinquième pixel.

15. Ecran d'affichage à cristaux liquides selon la revendication 14, dans lequel le motif de blocage de lumière (21a) chevauche partiellement l'électrode pixel (82).

16. Ecran d'affichage à cristaux liquides selon la revendication 12, dans lequel l'électrode pont (84) connecte un motif de blocage de lumière (21a) d'un sixième pixel et un motif de connexion intra-pixel (21b ; 21c) d'un septième pixel près du sixième pixel dans la seconde direction.

17. Ecran d'affichage à cristaux liquides selon la revendication 16, dans lequel l'électrode pont (84) est dans la même couche que l'électrode pixel (82).

18. Ecran d'affichage à cristaux liquides selon la revendication 12, dans lequel les premières électrodes de blocage de lumière (21 ; 221 ; FP) sont connectées électriquement les unes aux autres au sein d'une zone d'affichage, dans lequel la zone d'affichage sert à un affichage d'image efficace.

19. Ecran d'affichage à cristaux liquides selon la revendication 12, dans lequel la première électrode de blocage de lumière (21 ; 221 ; FP) est déconnectée électriquement de circuits externes.

20. Ecran d'affichage à cristaux liquides selon la revendication 12, dans lequel la première électrode de blocage de lumière (21 ; 221 ; FP) est dans la même couche que la ligne de grille (22 ; G1, G2, ..., Gn).

FIG. 1A

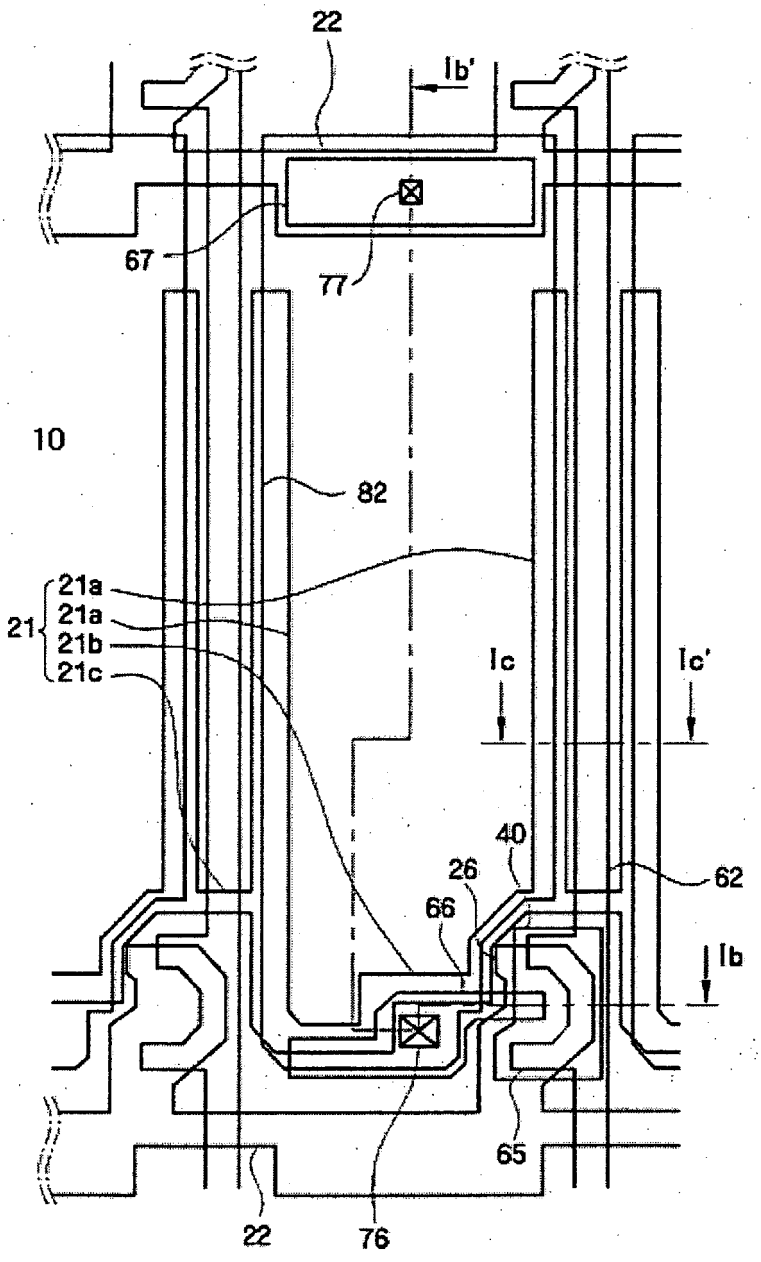


FIG. 1B

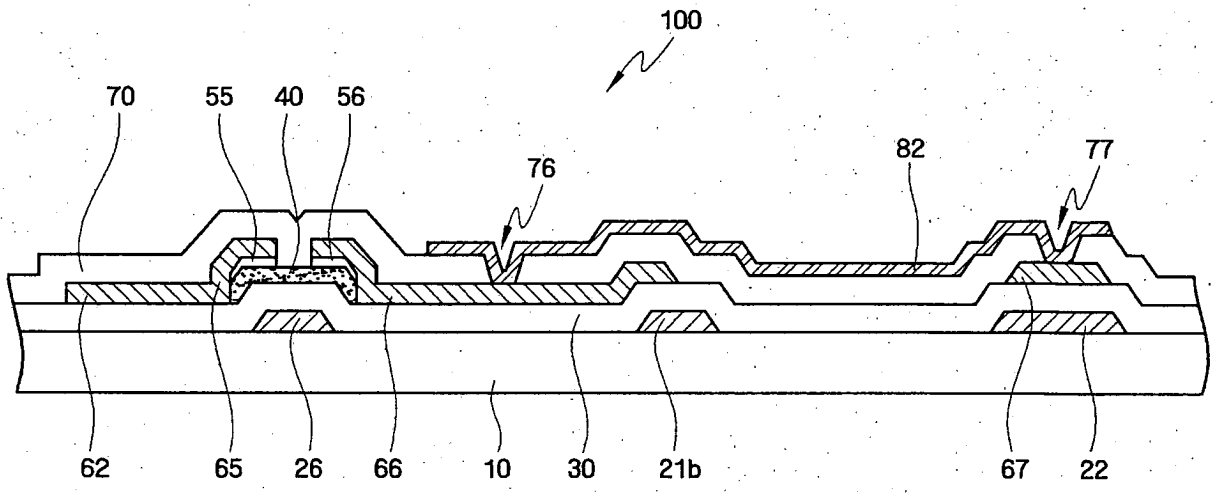

100
70
55
40
56
76
82
77
62
65
26
66
10
30
21b
67
22

FIG. 1C

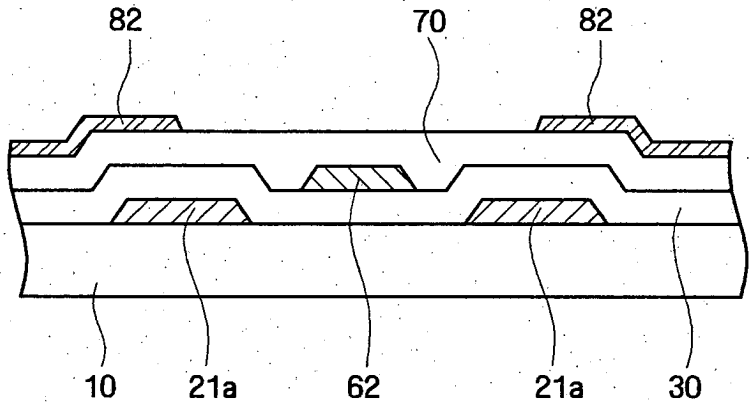

82
70
82
10
21a
62
21a
30

FIG. 1D

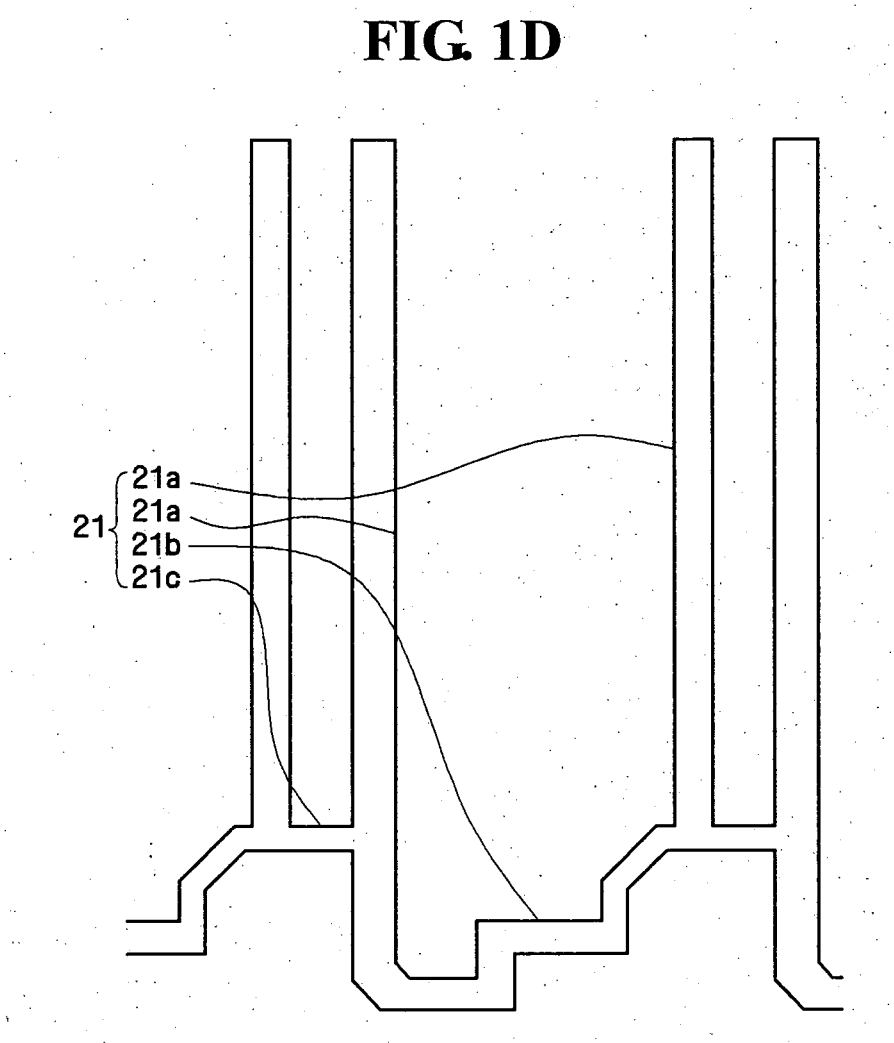


FIG. 2

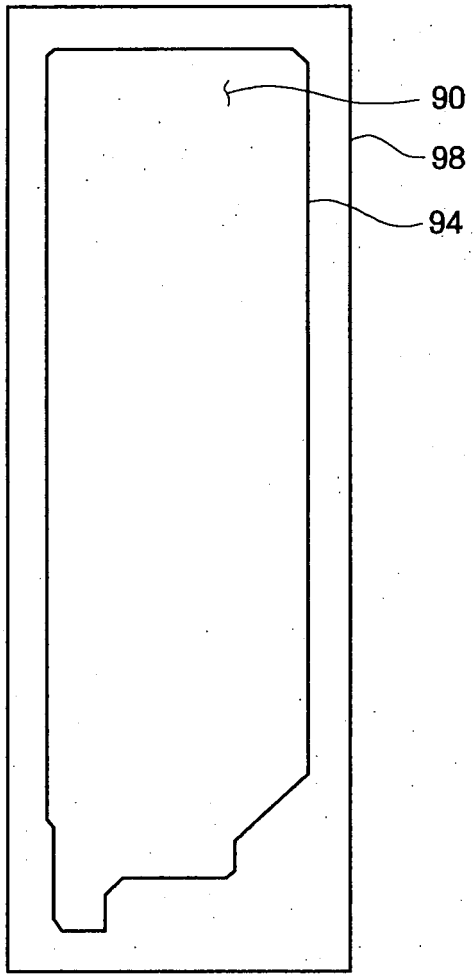


FIG. 3A

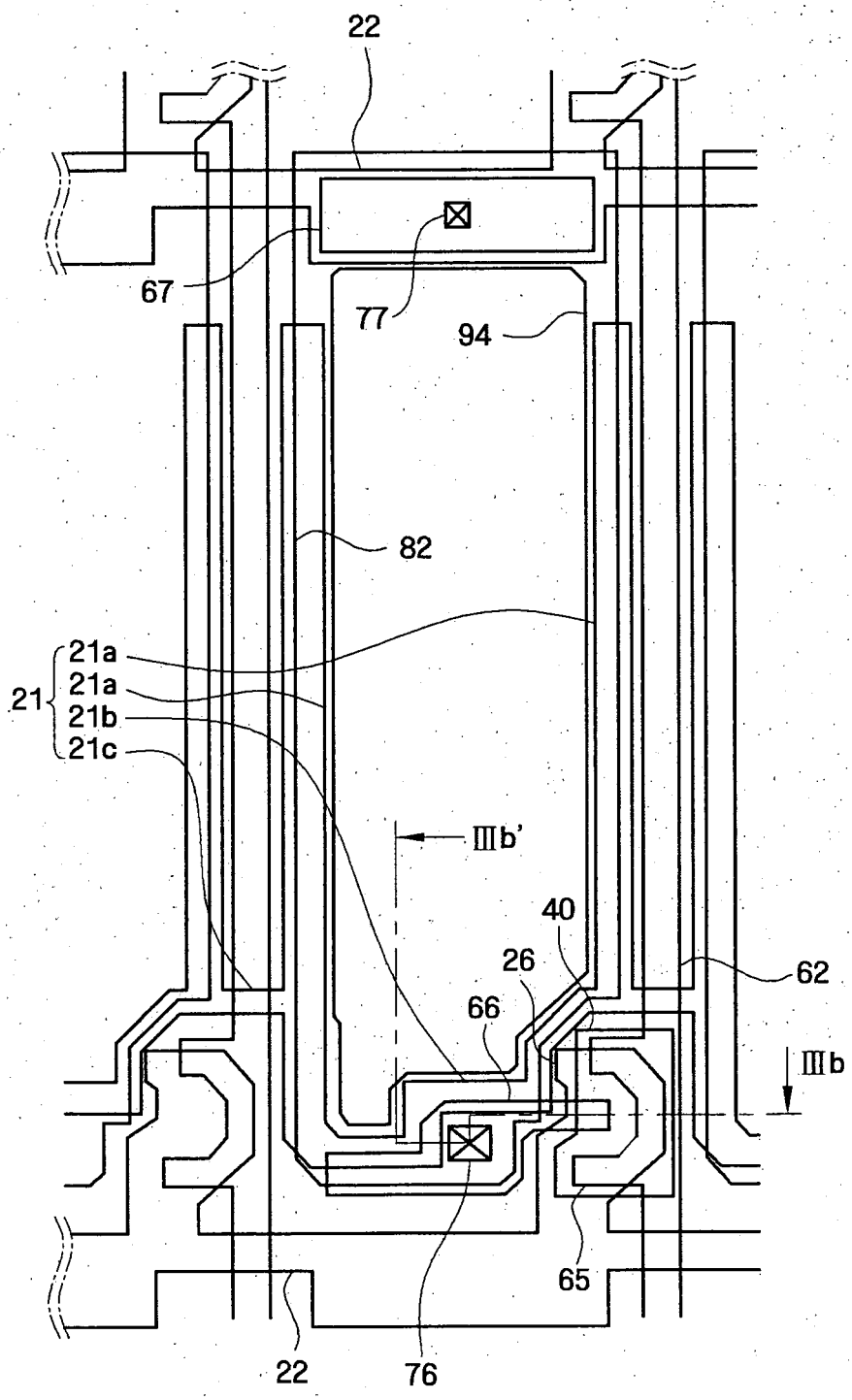


FIG. 3B

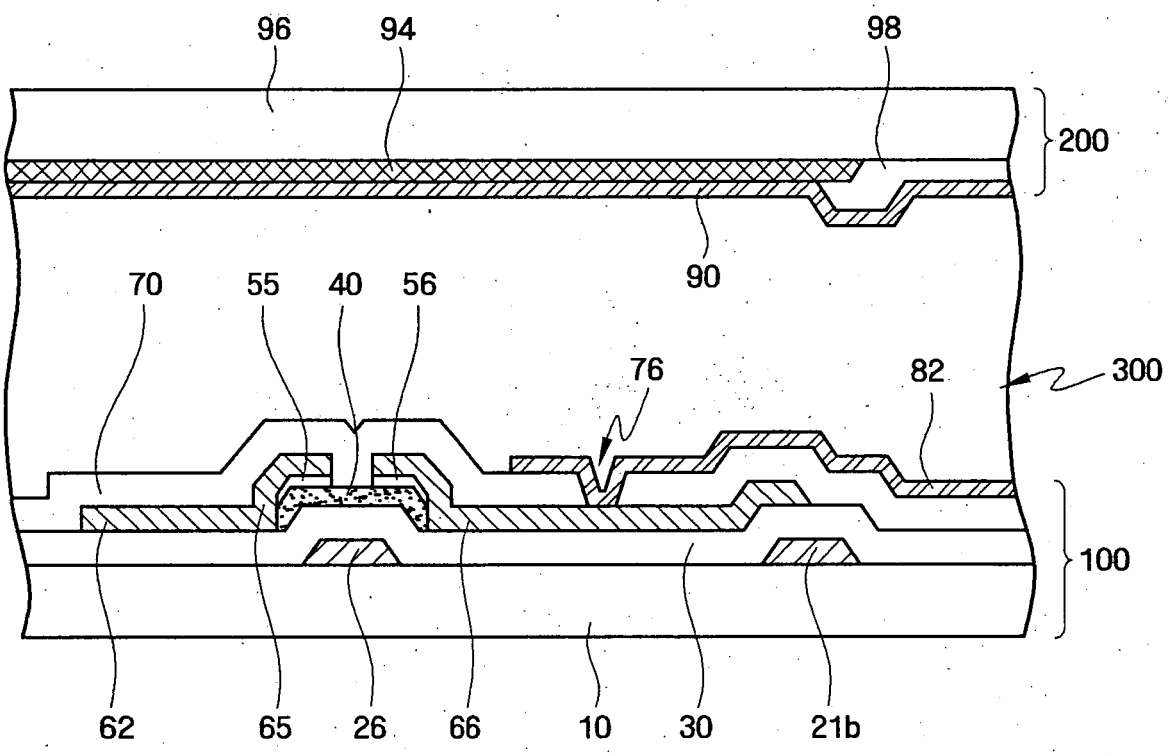


FIG. 4

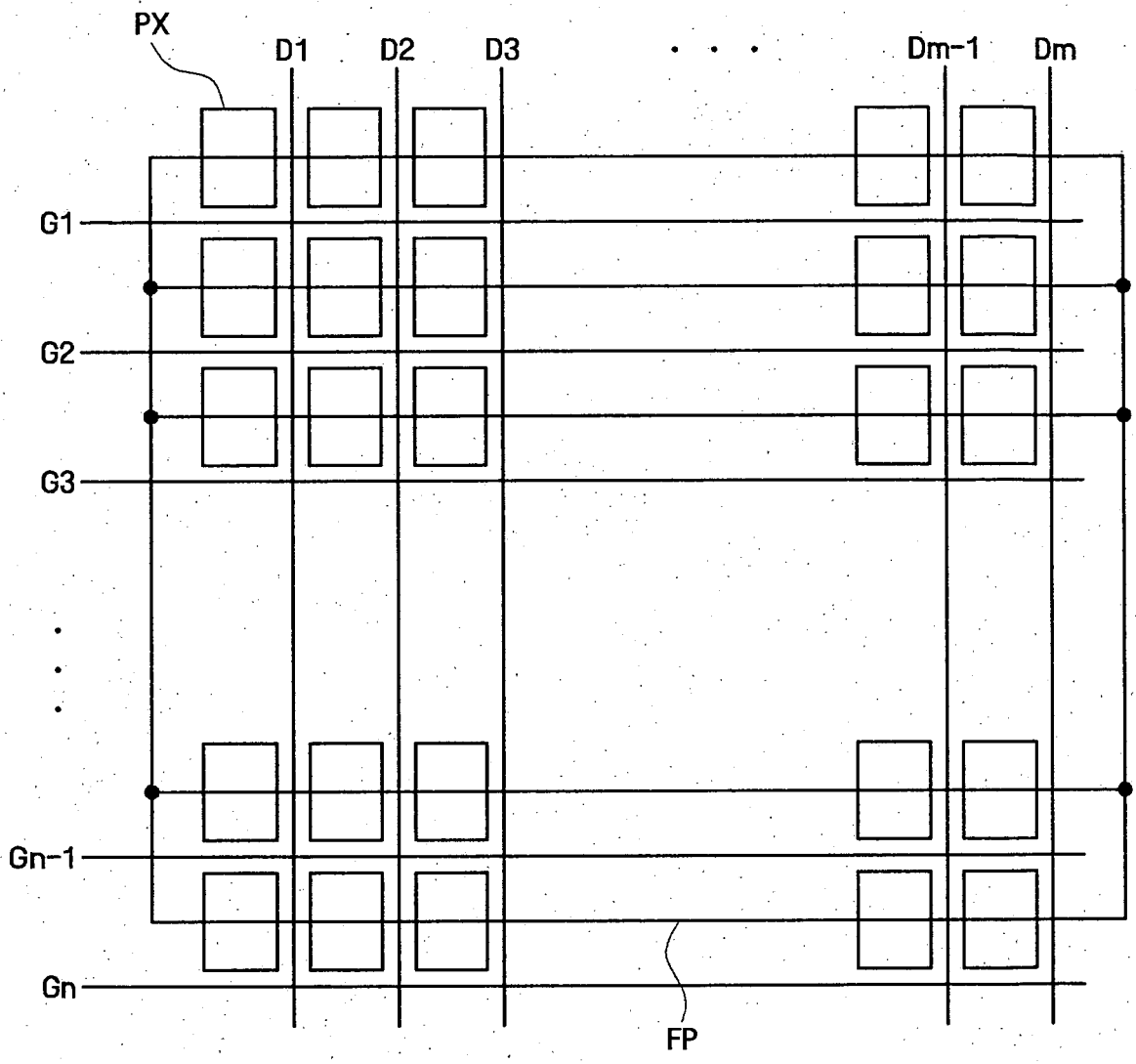


FIG. 5A

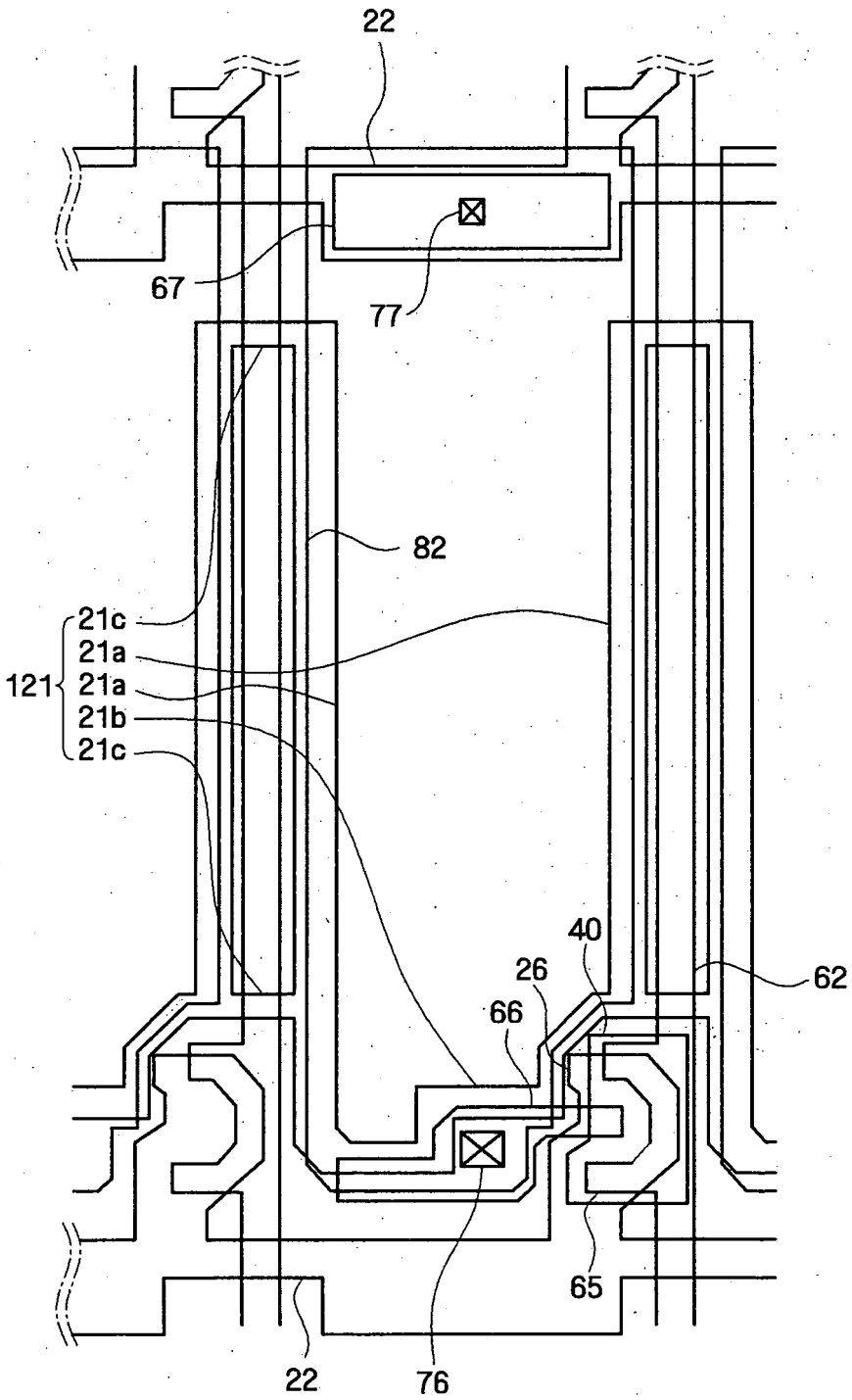


FIG. 5B

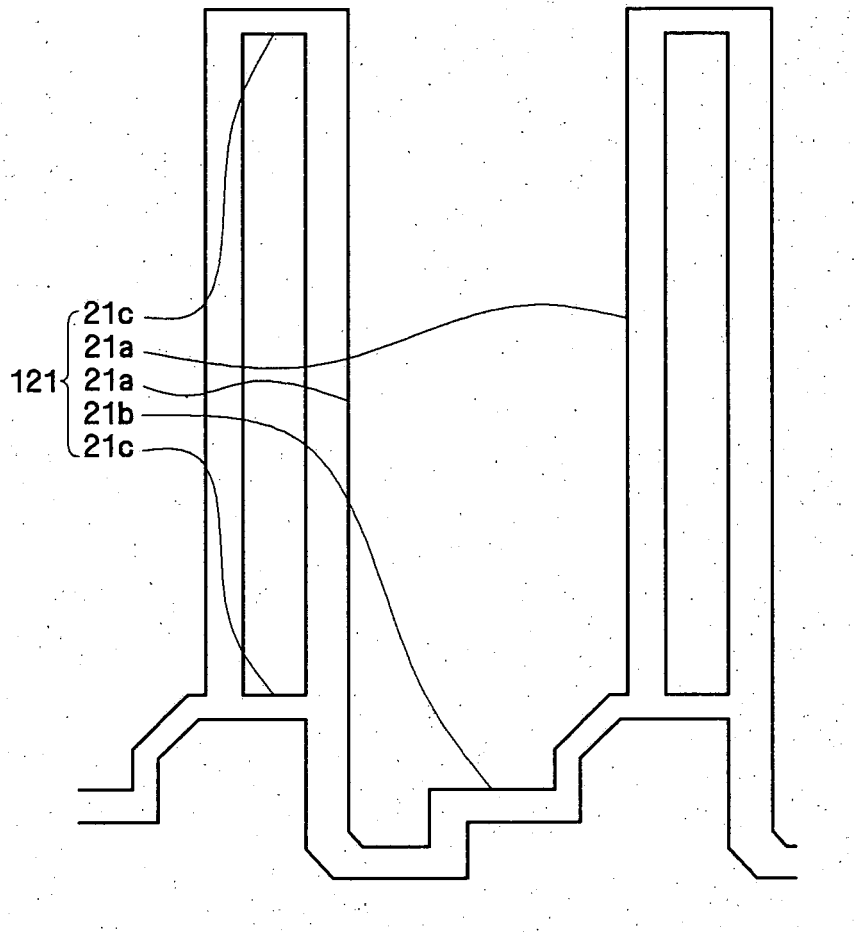


FIG. 6A

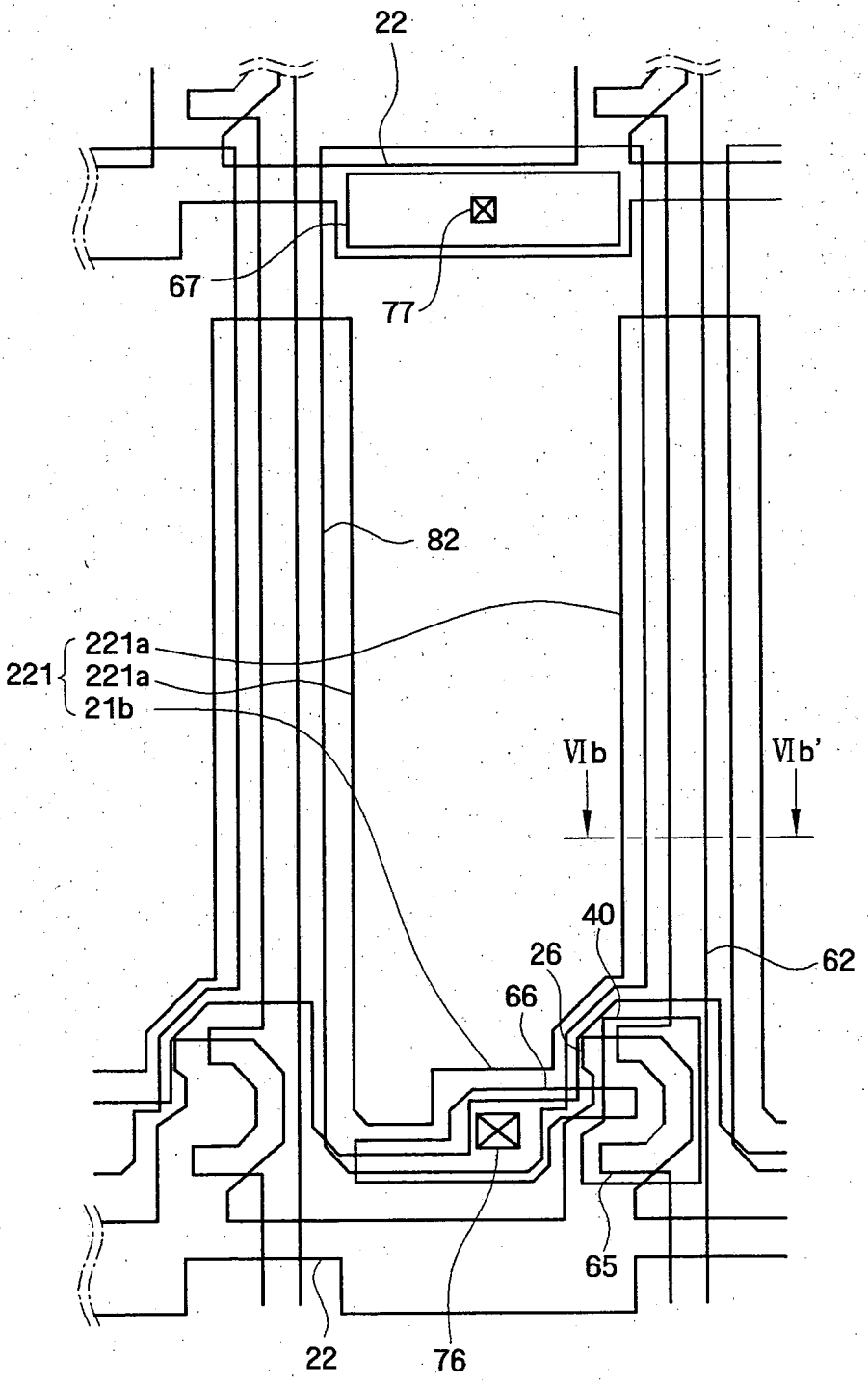


FIG. 6B

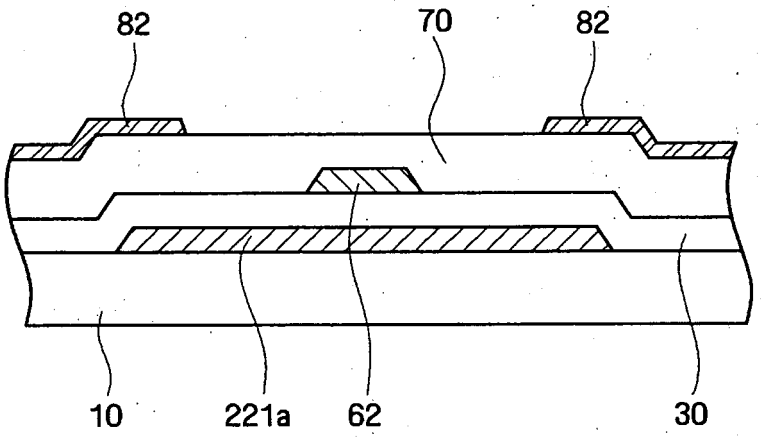


FIG. 6C

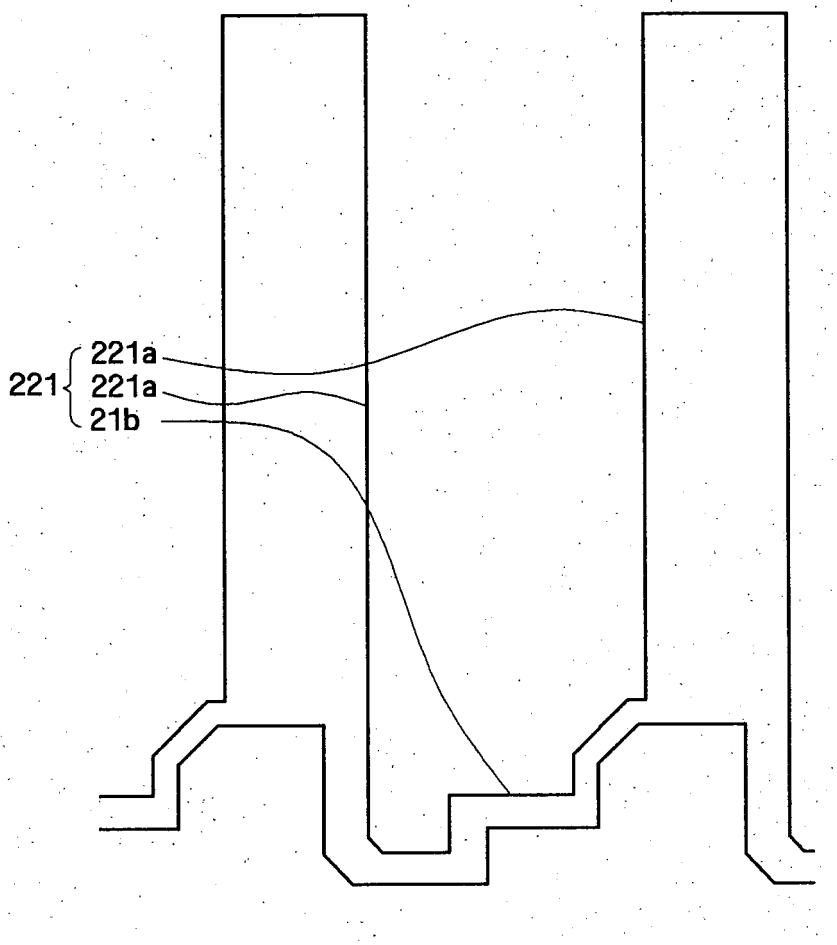


FIG. 7A

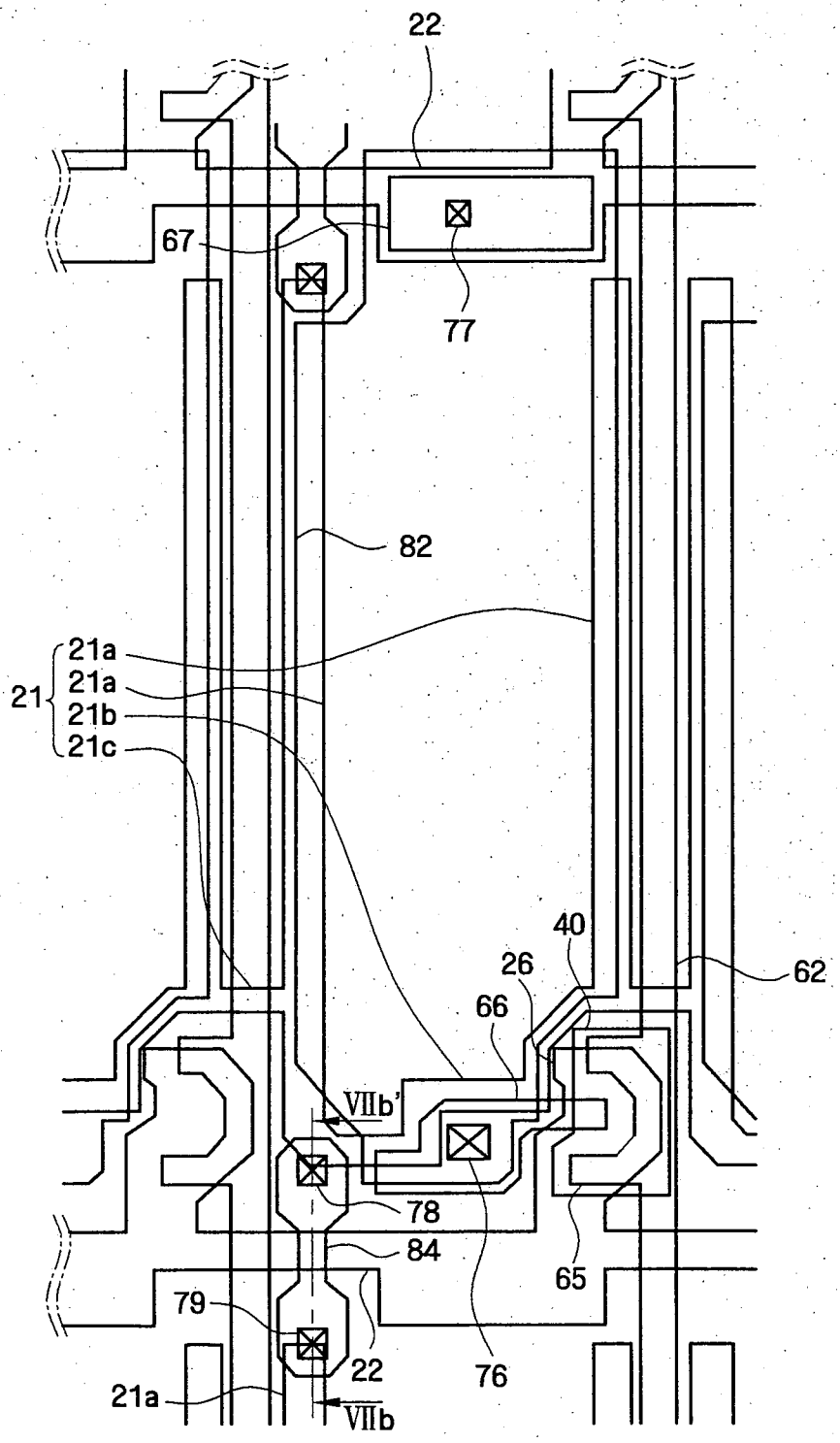

22
67
77
82
21a
21a
21
21b
21c
40
26
62
66
VIIb'
78
84
65
79
22
76
21a
VIIb

FIG. 7B

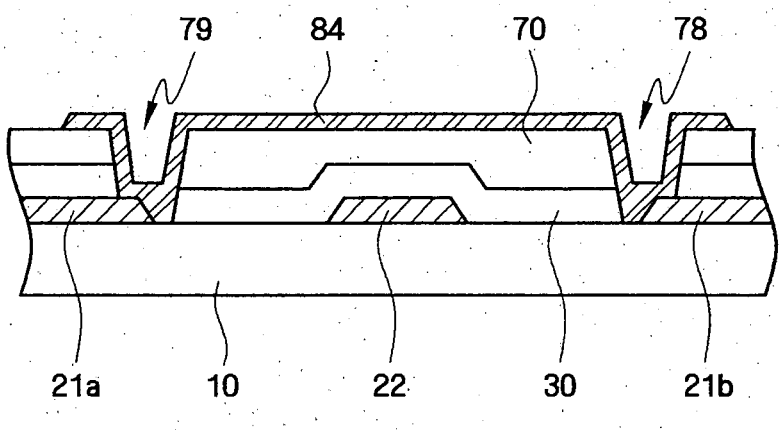


FIG. 7C

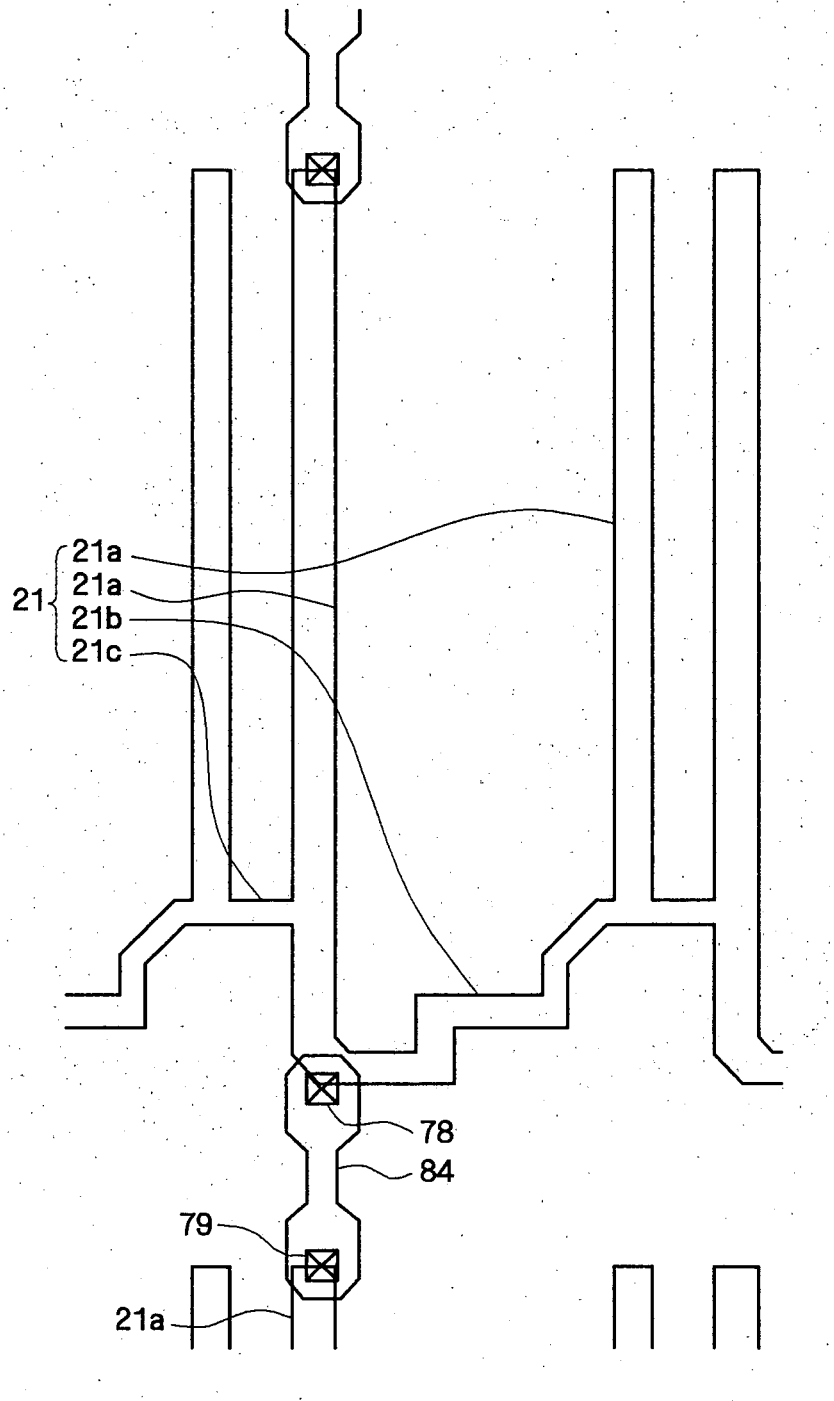


FIG. 7D

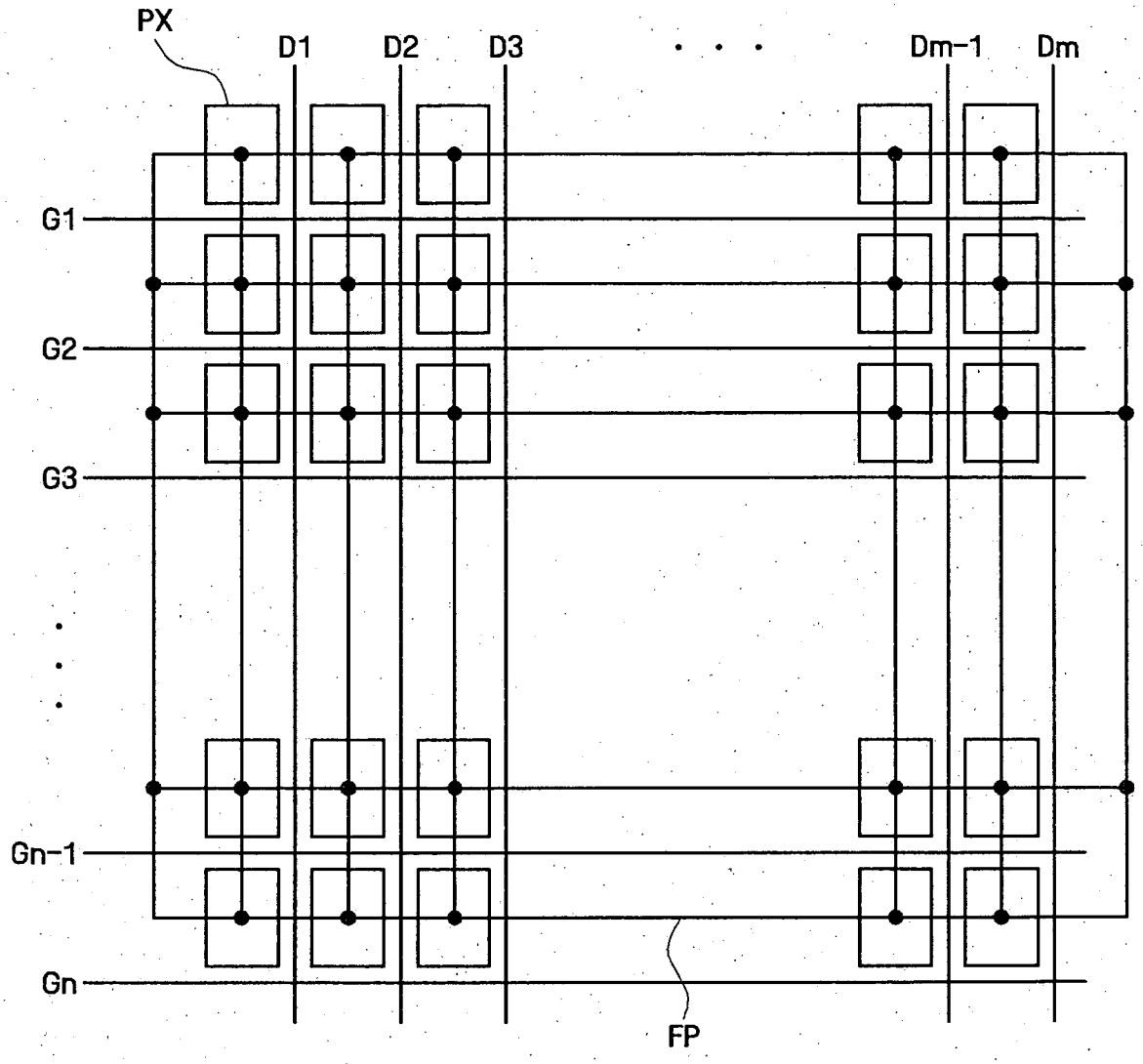


FIG. 8A

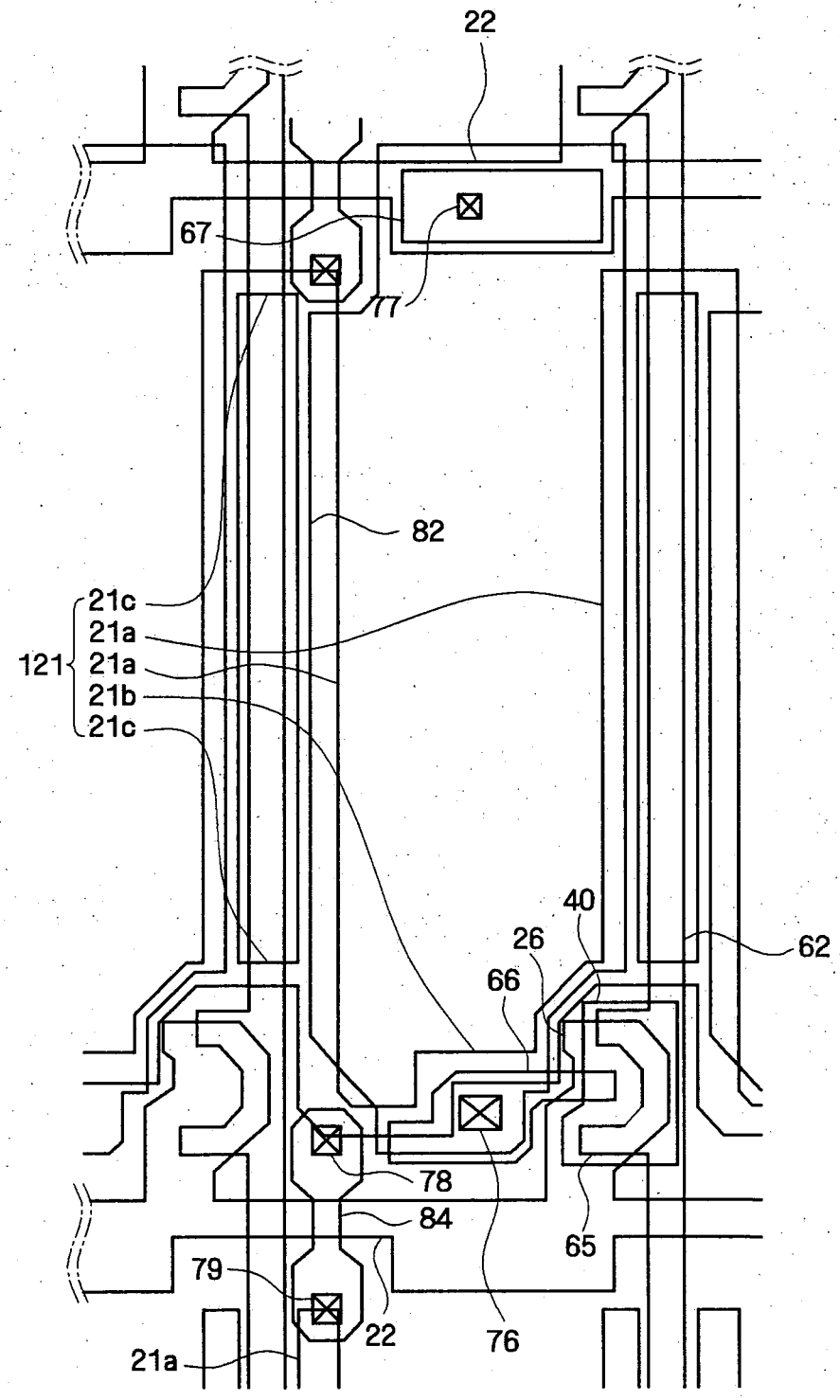


FIG. 8B

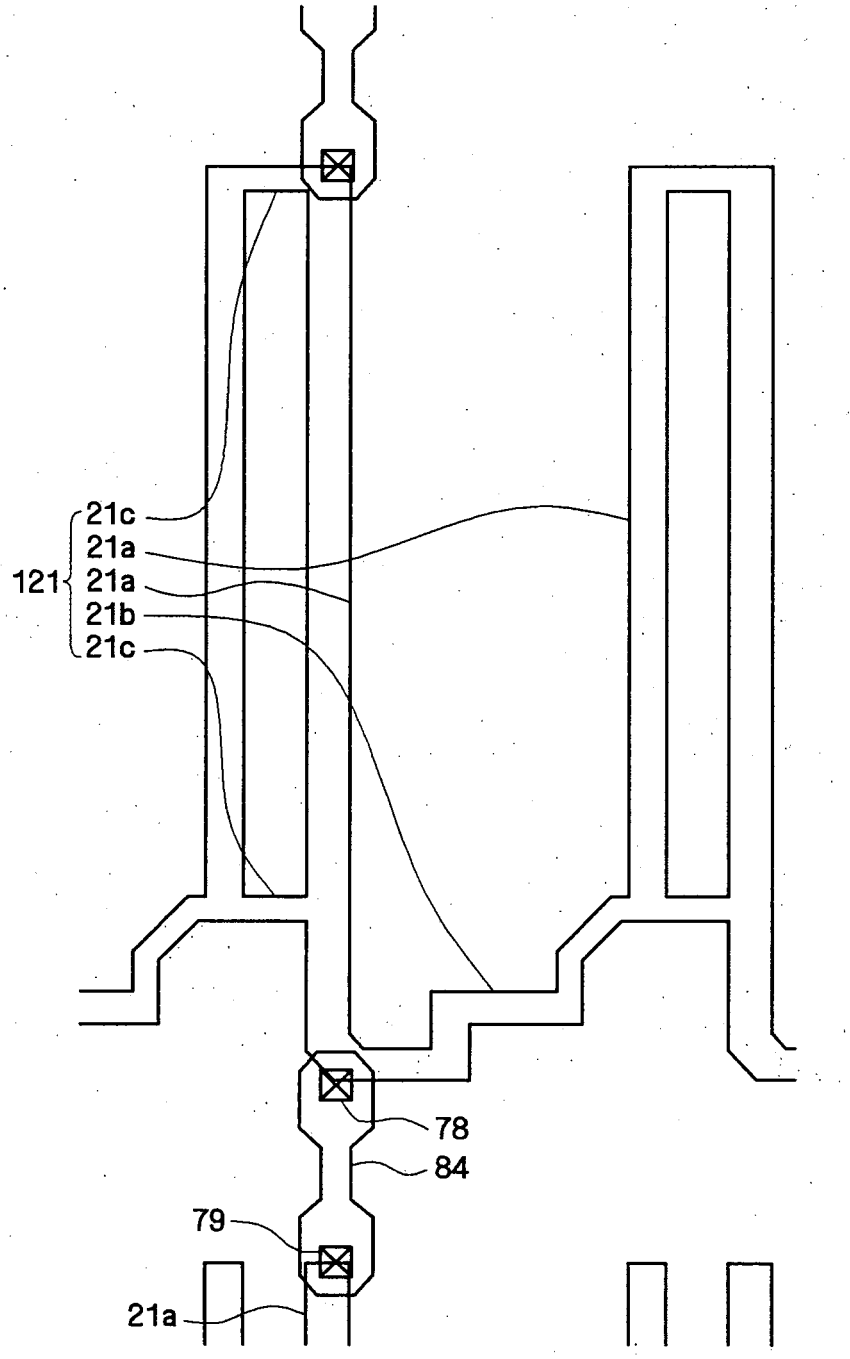


FIG. 9A

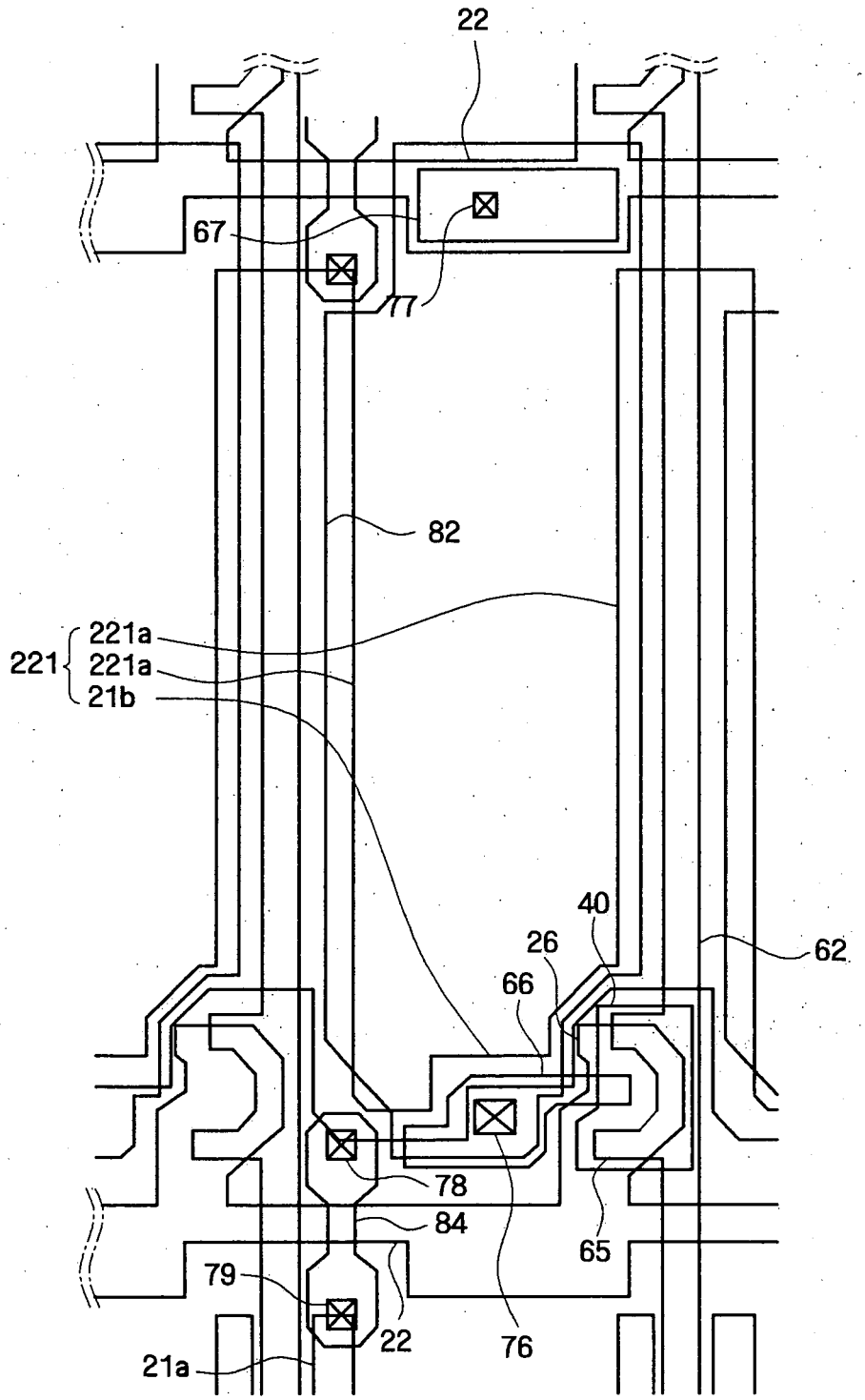
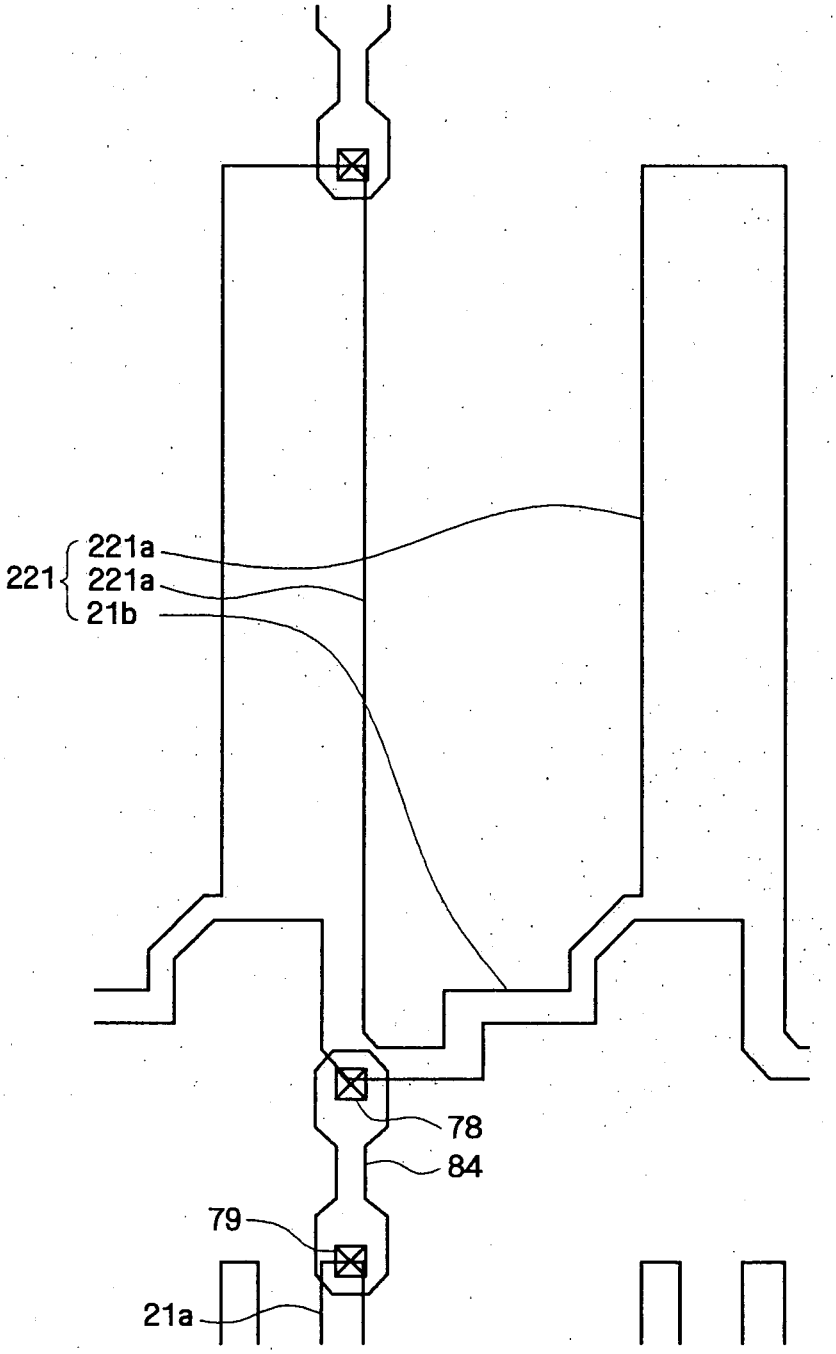


FIG. 9B



REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- KR 1020060077135 **[0001]**
- KR 1020060104553 **[0001]**
- US 6525788 B **[0009]**

专利名称(译)	具有浮动电极的液晶显示面板		
公开(公告)号	EP1890188B1	公开(公告)日	2018-10-24
申请号	EP2007015869	申请日	2007-08-13
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IPC分类号	G02F1/1362		
CPC分类号	G02F1/136209 G02F2001/136218		
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优先权	1020060077135 2006-08-16 KR 1020060104553 2006-10-26 KR		
其他公开文献	EP1890188A1		
外部链接	Espacenet		

摘要(译)

公开了一种具有增强图像质量的液晶显示面板。液晶显示面板具有多条栅极线，多条数据线，连接到栅极线和数据线的多个薄膜晶体管，多个像素电极和浮动电极。浮动电极沿数据线延伸，以防止漏光和垂直串扰。在整个液晶显示板中，浮动电极电互连以减少垂直串扰。