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(54) Liquid crystal display

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EP 1 882 977 B1

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Description

BACKGROUND OF THE INVENTION

(a) Field of the Invention

[0001] The present invention relates to a liquid crystal display. More particularly, the present invention relates to a liquid crystal display having fewer data driving circuits, and which prevents cross-talk generated during column inversion driving.

(b) Description of the Related Art

[0002] A liquid crystal display is one of the most widely used flat panel displays. The liquid crystal display includes two display panels each having field-generating electrodes such as a pixel electrode and a common electrode, and a liquid crystal layer interposed therebetween. The liquid crystal display induces an electric field in the liquid crystal layer by applying a voltage to the field generating electrodes, and determines the alignment of liquid crystal molecules of the liquid crystal layer to control polarization of incident light through the display panels, thereby displaying an image.

[0003] The liquid crystal display also includes a plurality of signal lines such as gate lines and data lines in order to supply a voltage to a respective pixel electrode by controlling a switching element connected to the respective pixel electrode. The gate line transfers a gate signal generated from a gate driving circuit, and the data line transfers a data voltage generated from a data driving circuit. The switching element transfers a data voltage to the respective pixel electrode according to the gate signal.

[0004] The gate driving circuit and data driving circuit are directly mounted on one of the two display panels in the form of a plurality of integrated circuit ("IC") chips. Alternatively, the gate driving circuit and data driving circuit are mounted on a flexible circuit layer and the flexible circuit layer is attached to one of the display panels. Such an IC chip is responsible for a large percentage of a manufacturing cost of a liquid crystal display. Particularly, since the data driver IC chip is much more expensive than a gate driving circuit IC chip, it is necessary to reduce the number of IC chips for a high resolution and large-sized liquid crystal display. The manufacturing cost of the gate driving circuit can be reduced by integrating the gate driving circuit with the display panel having the gate lines, data lines and switching elements. However, it is very difficult to integrate the data driving circuit with the display panel because the data driving circuit has a complicated structure. Therefore, a reduction of the number of data driver ICs is required.

[0005] US 2006/131585 A1 discloses a thin film transistor array panel using polysilicon as a semiconductor. A thin film transistor array panel includes a substrate; a plurality of semiconductor islands formed on the substrate, the plurality of semiconductor islands including a plurality of first and second extrinsic regions, and a plurality of intrinsic regions; a gate insulating layer covering the semiconductor islands; a plurality of gate lines including a plurality of gate electrodes overlapping the intrinsic region and formed on the gate insulating layer; a plurality of data lines connected to the first extrinsic regions and formed on the gate insulating layer; and a plurality of pixel electrodes connected to the second extrinsic regions, wherein a plurality of protrusions are formed on the surfaces of the semiconductor islands, and a length of a semiconductor island is a multiple of the a distance between at least two protrusions.

[0006] US 2005/167669 A1 discloses a thin film transistor array panel and a method of manufacturing the same, and more particularly, to a thin film transistor array panel used in a liquid crystal display device and a method of manufacturing the same. A plurality of gate lines having gate electrodes are formed on a substrate and a semiconductor layer is formed on a gate insulating layer covering the gate lines. A plurality of data lines intersecting the gate lines are formed on the gate insulating layer and a plurality of drain electrodes are formed extending parallel with and adjacent to the data lines. Furthermore, a plurality of storage capacitor conductors are formed to be connected to the drain electrodes and to overlap an adjacent gate line. A passivation layer made of an organic material is formed on the above structure and has a contact hole. Furthermore, a plurality of pixel electrodes are formed to be electrically connected to the drain electrodes through the contact hole.

[0007] EP 0 752 611 A2 discloses an active matrix liquid crystal display (AMLCD) having a high pixel aperture ratio. The display has an increased pixel aperture ratio because the pixel electrodes are formed over the insulating layer so as to overlap portions of the array address lines. Both the manufacturability and capacitive cross-talk of the TFT-based device are improved due to the use of a photo-imageable insulating layer between the pixel electrodes and the address lines. According to certain other embodiments, the insulating layer may be BCB (either photo-imageable or not) and/or have a dielectric constant less than about 3.0.

[0008] US 2003/043328 A1 discloses a plane display element having pixel electrodes arranged like a matrix. An electric field shielding wiring is provided in the gap between the pixel electrodes adjacent in parallel to the signal line, to minimize the inter-electrode parasitic capacity generated in the gap between the pixel electrodes, which is caused by the change in the pixel potential of the pixel electrode when the polarity of the signal line potential is changed, and prevent an increase in the pixel potential of the pixel electrode of the previous stage.

BRIEF SUMMARY OF THE INVENTION

[0009] The present invention has been made in an effort to provide a liquid crystal display having features,

aspects and advantages of reducing the number of data driving circuit IC chips and preventing cross-talk generated during column inversion driving.

[0010] The present invention provides a liquid crystal display including: a substrate, a plurality of gate lines, a plurality of data lines, a plurality of thin film transistors and a plurality of pixel electrodes. The gate lines are formed on the substrate, and the data lines cross the gate lines. The thin film transistors are connected to the gate lines and the data lines, and each thin film transistor includes a drain electrode. The pixel electrodes are connected to the thin film transistors and arranged in a matrix, and each of the pixel electrodes includes a first side disposed in parallel with the gate lines and a second side shorter than the first side. In the liquid crystal display, a predetermined portion of each the drain electrodes are disposed between adjacent pixel electrodes. A data driver is coupled to the data lines for applying a voltage having positive polarity or negative polarity to the pixel electrodes, wherein the data driver is able to drive the display in an mx1 inversion scheme with m being an integer greater than 2. The predetermined portion of the drain electrodes are overlapped with only one of the adjacent pixel electrodes if the polarities of the adjacent pixel electrodes are different, and the predetermined portion of the drain electrodes are overlapped with both of the adjacent pixel electrodes if the polarities of the adjacent pixel electrodes are the same.

[0011] The polarity of the pixel electrodes is driven in an m x 1 inversion-drive manner, wherein the voltage polarity of m pixel electrodes adjacent to each other in a row direction are positive and the voltage polarity of one pixel electrode adjacent to the first one of pixel electrodes is negative.

[0012] In exemplary embodiments, the m may be 3.

[0013] The liquid crystal display further includes a storage electrode line overlapped with respective pixel drain electrodes.

[0014] A predetermined portion of each of the drain electrodes and the storage electrode lines may be disposed between adjacent pixel electrodes in a column direction.

[0015] Each of the pixel electrodes may cover a previous gate line.

[0016] The liquid crystal display may further include an organic layer formed between the pixel electrodes and the data lines, and between the pixel electrodes and the gate lines.

[0017] The length of the first side may be three times longer than that of the second side.

[0018] The liquid crystal display may further include a gate driver connected to the gate lines, wherein the gate driver may be placed at the same layer as the gate lines, the data lines and the thin film transistors.

[0019] The plurality of pixel electrodes may comprise first, second and third pixel electrodes. The gate lines are formed on the substrate, and the data lines cross the gate lines. The thin film transistors are connected to the gate lines and the data lines. The first, second, and third pixel electrodes are connected to the thin film transistors, respectively, and are adjacent in a column direction. Each of the first to third pixel electrodes has a first side disposed in parallel with the gate lines and a second side shorter than the first side. Polarities of the second and third pixel electrodes are the same, and the polarity of the first pixel electrode is opposite to the polarity of the second and third pixel electrodes. A first drain electrode is disposed between the first and second pixel electrodes, and a second drain electrode is disposed between the second and third pixel electrodes. The first drain electrode is overlapped only with the first pixel electrode of the first, second and third pixel electrodes, and the second drain electrode is overlapped with both of the second and third pixel electrodes.

[0020] The liquid crystal display may further include a storage electrode line overlapped with corresponding pixel and drain electrodes.

[0021] Each of the pixel electrodes may cover a previous gate line.

[0022] The liquid crystal display may further include an organic layer formed between the pixel electrodes and the data lines, and between the pixel electrodes and the gate lines.

[0023] The length of the first side is three times longer than the length of the second side.

[0024] The liquid crystal display may further include a gate driver connected to the gate lines, and the gate driver may be placed at the same layer as the gate lines, the data lines and the thin film transistors.

BRIEF DESCRIPTION OF THE DRAWINGS

[0025] Features aspects and advantages of the present invention will be made apparent by describing exemplary embodiments of the present invention with reference to the accompanying drawings, in which:

FIG. 1 is a block diagram illustrating a liquid crystal display according to an exemplary embodiment of the present invention;

FIG. 2 is an equivalent circuit diagram of one pixel of a liquid crystal display according to an exemplary embodiment of the present invention;

FIG. 3 is a plan view layout of a liquid crystal display according to another exemplary embodiment of the present invention; and

FIG. 4 is a cross-sectional view of the liquid crystal display shown in FIG. 3 taken along line IX-IX.

DETAILED DESCRIPTION OF THE INVENTION

[0026] The present invention will be described more fully hereinafter with reference to the accompanying drawings, in which exemplary embodiments of the invention are shown.

[0027] In the drawings, the thickness of layers, films,

panels, regions, etc., are exaggerated for clarity. Like reference numerals designate like elements throughout the specification. It will be understood that when an element such as a layer, film, region, or substrate is referred to as being "on" another element, it can be directly on the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly on" another element, there are no intervening elements present. As used herein, the term "and/or" includes any and all combinations of one or more of the associated listed items.

[0028] It will be understood that, although the terms first, second, third etc. may be used herein to describe various elements, components, regions, layers and/or sections, these elements, components, regions, layers and/or sections should not be limited by these terms. These terms are only used to distinguish one element, component, region, layer or section from another element, component, region, layer or section. Thus, a first element, component, region, layer or section discussed below could be termed a second element, component, region, layer or section without departing from the teachings of the present invention.

[0029] The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the invention. As used herein, the singular forms "a", "an" and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "comprises" and/or "comprising," or "includes" and/or "including" when used in this specification, specify the presence of stated features, regions, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, regions, integers, steps, operations, elements, components, and/or groups thereof.

[0030] Spatially relative terms, such as "beneath", "below", "lower", "above", "upper" and the like, may be used herein for ease of description to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the figures. It will be understood that the spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. For example, if the device in the figures is turned over, elements described as "below" or "beneath" other elements or features would then be oriented "above" the other elements or features. Thus, the exemplary term "below" can encompass both an orientation of above and below. The device may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein interpreted accordingly.

[0031] Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which this invention belongs. It will be further understood that terms, such as those defined in commonly used dictionaries, should be interpreted as having a meaning that is consistent with their meaning in the context of the relevant art and the present disclosure, and will not be interpreted in an idealized or overly formal sense unless expressly so defined herein.

[0032] Embodiments of the present invention are described herein with reference to cross section illustrations that are schematic illustrations of idealized embodiments of the present invention. As such, variations from the shapes of the illustrations as a result, for example, of manufacturing techniques and/or tolerances, are to be expected. Thus, embodiments of the present invention should not be construed as limited to the particular shapes of regions illustrated herein but are to include deviations in shapes that result, for example, from manufacturing. For example, a region illustrated or described as flat may, typically, have rough and/or nonlinear features. Moreover, sharp angles that are illustrated may be rounded. Thus, the regions illustrated in the figures are schematic in nature and their shapes are not intended to illustrate the precise shape of a region and are not intended to limit the scope of the present invention.

[0033] Hereinafter, a liquid crystal display according to an exemplary embodiment of the present invention will be described with reference to FIG. 1 and FIG. 2.

[0034] FIG. 1 is a block diagram illustrating a liquid crystal display according to an exemplary embodiment of the present invention. FIG. 2 is an equivalent circuit diagram illustrating a pixel of a liquid crystal display according to an exemplary embodiment of the present invention.

[0035] Referring to FIG. 1 and FIG. 2, the liquid crystal display according to an exemplary embodiment of the present invention includes a liquid crystal panel assembly 300, a gate driver 400 and data driver 500 connected to the liquid crystal panel assembly 300, a gray voltage generator 800 connected to the data driver 500, and a signal controller 600 for controlling the drivers 400 and 500.

[0036] The liquid crystal panel assembly 300 includes a plurality of display signal lines and a plurality of pixels PX1, PX2 and PX3 connected to display signal lines and arranged in a matrix shape. Further, the liquid crystal panel assembly 300 includes a liquid crystal layer 3 interposed between lower and upper panels 100 and 200 facing each other as shown in FIG. 2.

[0037] The signal lines G_1-G_n, D_1-D_m include a plurality of gate lines G_1-G_n transferring a gate signal (or a scanning signal) and a plurality of data lines D_1-D_m transferring a data signal.

[0038] The gate lines G_1-G_n extend substantially in a row direction in parallel with each other, and the data lines D_1-D_m extend substantially in a column direction in parallel with each other, as illustrated in FIG. 1.

[0039] Each of the pixels PX1, PX2 and PX3 has a longitudinal structure in the row direction. For example, the pixels PX1, PX2, and PX3 connected to the gate line GL and the data line DL include a switching element Q connected to signal lines GL and DL, and a liquid crystal capacitor Clc and a storage capacitor Cst connected

thereto. However, the storage capacitor Cst can be omitted according to need in alternative exemplary embodiments.

[0040] The switching element Q is a three-terminal element such as a thin film transistor disposed at the lower panel 100. The switching element Q includes a control terminal connected to the gate line GL, an input terminal connected to a data line DL and an output terminal connected to a liquid crystal capacitor Clc and a storage capacitor Cst.

[0041] The liquid crystal capacitor Clc uses a pixel electrode 191 at the lower panel 100 and a common electrode 270 at the upper panel 200 as two terminals, and a liquid crystal layer 3 between two electrodes 191 and 270 functions as a dielectric material. The pixel electrode 191 is connected to the switching element Q. The common electrode 270 is formed on the entire surface of the upper panel 200 and receives a common voltage Vcom. Unlike FIG. 2, a common electrode 270 can be formed at the lower panel 100. In this case, at least one of the two electrodes 191 and 270 can be made in a line shape or a rod shape.

[0042] A storage capacitor Cst functioning as a subsidiary of the liquid crystal capacitor Clc is formed of a sustaining electrode line SL overlapping a pixel electrode 191 with an insulator interposed therebetween. A predetermined voltage such as a common voltage Vcom is applied to the additional signal line. The storage capacitor Cst can be formed of a pixel electrode 191 overlapping a previous gate line with an insulator as a medium.

[0043] In order to embody color display, each of the pixels PX1-PX3 displays a unique primary color (spatial division), or alternatively, each of the pixels PX1-PX3 displays different primary colors according to time (temporal division), thereby displaying desired colors through a spatial or temporal sum of these primary colors. For example, the primary colors are three primary colors, red, green and blue. FIG. 2 shows a color filter 230 displaying one of the primary colors on a region of an upper panel 200 corresponding to the pixel electrode 191 by each of the pixels PX1-PX3 as an example of spatial division. Unlike that shown in FIG. 2, a color filter 230 can be formed below a pixel electrode 191 of the lower panel 100. Color filters 230 for one primary color of pixels PX1-PX3 adjacent in a row direction extend in a row direction and are connected to one another, and color filters 230 for different colors are alternately arranged in a column direction.

[0044] It is assumed that each color filter 230 uniquely displays one of a red, green and blue color throughout the specification. A red pixel is a pixel with a red color filter 230, a green pixel is a pixel with a green color filter 230 and a blue pixel is a pixel with a blue color filter 230. The red pixel, blue pixel and green pixel are sequentially and alternately arranged in a column direction.

[0045] As described above, the pixels PX1- PX3 of three primary colors form one dot (DT) as a basic unit of an image (see FIG. 1).

[0046] Referring to FIG. 1 again, the gate driver 400 is integrated with the liquid crystal panel assembly 300 along with the signal lines G_1-G_n D_1-D_m and the thin film transistor switching elements Q. The gate driver 400 is formed at the left side and the right side of the liquid crystal panel assembly 300 (only the left side gate driver 400 shown in FIG. 1). The gate driver 400 applies a gate signal formed of a combination of a gate-on voltage Von and a gate-off voltage Voff. The gate driver 400 can be mounted directly on the liquid crystal assembly 300 as an IC chip. Alternatively, the gate driver 400 can be mounted on the liquid crystal panel assembly 300 in a tape carrier package ("TCP") type by being mounted on a flexible printed circuit film, or can be mounted on an additional printed circuit board ("PCB").

[0047] At least one polarizer (not shown) is attached at the outer surface of the liquid crystal panel assembly 300 for polarizing the light.

[0048] The gray voltage generator 800 generates two gray voltage sets (or reference gray voltage sets) related to a transmittance of a pixel PX. One of the two sets has a positive value and the other has a negative value relative to a common voltage Vcom.

[0049] The data driver 500 is connected to data lines D_1-D_m of the liquid crystal panel assembly 300, selects a gray voltage from the gray voltage generator 800, and supplies the selected gray voltage to the data lines D_1-D_m as a data signal. When the gray voltage generator 800 only provides a predetermined number of reference gray voltages instead of supplying gray voltages for all grays, the data driver 500 generates a gray voltage for all grays by dividing the reference gray voltage and selects one among them. The data driver 500 can be mounted directly on a liquid crystal panel assembly 300 as an IC chip. Alternatively, the data driver 500 can be attached on the liquid crystal panel assembly 300 as a TCP by being mounted on a flexible printed circuit film (not shown), or mounted on an additional PCB. However, the data driver 500 can be integrated with the liquid crystal panel assembly 300 with the signal lines G_1-G_n and D_1-D_m and the thin film transistor switching elements Q.

[0050] The signal controller 600 controls the gate driver 400 and the data driver 500.

[0051] Hereinafter, the operation of such a liquid crystal display according to the present exemplary embodiment will be described in more detail.

[0052] The signal controller 600 receives an input control signal from an external graphics controller (not shown) for controlling display of input image signals R, G and B. The input image signals R, G and B have information about luminance of each pixel PX. The luminance has a predetermined number of grays, for example, 1024 ($=2^{10}$), 256 ($=2^8$) or 64 ($=2^6$). For example, the input control signal includes a vertical synchronization signal Vsync, a horizontal synchronizing signal. Hsync, a main clock signal MCLK, a data enable signal DE, etc.

[0053] The signal controller 600 receives an input control signal from the external graphics controller (not

shown) for controlling the display of input image signals R, G and B, and processes the received input control signal to be suitable to an operating condition of the liquid crystal panel assembly 300. Then, the signal controller 600 generates a gate control signal CONT1 and a data control signal CONT2, and outputs them to the gate driver 400 and data driver 500, respectively. The image signal processing of the signal controller 600 includes an operation for rearranging the input image signals R, G and B according to the arrangement of the pixels.

[0054] The gate control signal CONT1 includes a scanning start signal STV for ordering start of scanning and at least one clock signal for controlling the output cycle of the gate-on voltage (Von). The gate control signal CONT1 can further include an output enable signal OE that limits a time duration of the gate-on voltage Von.

[0055] The data control signal CONT2 includes a horizontal synchronization start signal STH for notifying beginning of digital image signal DAT transmission to one column of pixels, and a load signal LOAD and a data clock signal HCLK for ordering load of an analog data signal to the data lines D_1-D_m. The data control signal CONT2 can further include an inversion signal RVS which inverts a voltage polarity of an analog data signal for a common voltage Vcom. Hereinafter, the data signal polarity denotes the voltage polarity of a data signal for a common voltage.

[0056] The data driver 500 receives a digital image signal DAT for a column of pixels, and converts the digital image signal DAT to an analog data signal by selecting a gray voltage corresponding to each digital image signal DAT according to the data control signal CONT2 from the signal controller 600. Then, the analog data signal is supplied to corresponding data lines D1-Dm.

[0057] The gate driver 400 supplies a gate-on voltage Von to gate lines G_1-G_n according to a gate control signal CONT1 from the signal controller 600, thereby turning on a switching element Q connected to the gate lines G_1-G_n. Then, the data signal supplied to the data lines D_1-D_m is supplied to a corresponding pixel PX through the turned-on switching element Q.

[0058] The difference between a voltage of a data signal supplied to a pixel PX and a common voltage Vcom is shown as a charge voltage of a liquid crystal capacitor Clc, that is, a pixel voltage. Liquid crystal molecules vary their arrangement according to the level of the pixel voltage, and vary the polarization of light passing through the liquid crystal layer 3 according to the variation of the liquid crystal molecule arrangement. Such a polarization variation is shown as a transmittance variation of light by a polarizer attached to the display panel assembly 300, and the pixel PX displays luminance expressing the gray of the image signal DAT.

[0059] By repeating the above described operation in a unit of 1 horizontal period ("1H") which is equivalent to one cycle of a horizontal synchronizing signal Hsync and a data enable signal DE, the gate-on voltage Von is sequentially provided to all of the gate lines G_1-G_n and an image of one frame is displayed by supplying the data signals to all of the pixels PX.

[0060] After displaying the image of one frame, the next frame starts and the state of the inversion signal RVS supplied to the data driver 500 is controlled to invert the polarity of the data signal from the previous frame ("frame inversion"). Herein, the polarity of a data signal flowing through a data line can be inverted according to a characteristic of the inversion signal RVS even within one frame (for example, row inversion, dot inversion), or the polarity of the data signal supplied to one pixel can be different (for example column inversion, dot inversion).

[0061] Hereinafter, a liquid crystal panel assembly according to an exemplary embodiment of the present invention will be described with reference to FIGS. 8 and 9.

[0062] FIG. 3 is a plan view layout illustrating a liquid crystal panel assembly according to another exemplary embodiment of the present invention. FIG. 4 is a cross-sectional view illustrating a liquid crystal panel assembly shown in FIG. 3 taken along line IX-IX.

[0063] The liquid crystal panel assembly according to the present alternative exemplary embodiment includes a thin film transistor array panel 100, a common electrode panel 200 facing the thin film transistor array panel 100 and a liquid crystal layer 3 interposed between the two display panels 100 and 200.

[0064] The layered structure of the liquid crystal panel assembly according to the present alternative exemplary embodiment is approximately identical to the layered structure of the liquid crystal panel assembly shown in FIGS. 3 to 6.

[0065] The lower panel 100 will be described hereinafter. A plurality of gate conductors having a plurality of gate lines 121 and storage electrode lines 131a and 131b are formed on an insulation substrate 110. Each gate line 121 includes a wide end 129 of the gate electrode 124, and each storage electrode line 131a and 131b includes a storage electrode 137a and 137b, respectively. A gate insulating layer 140 is formed on a gate conductor 121. A semiconductor island 154 is formed on the gate insulating layer 140, and a plurality of ohmic contacts 163 and 165 are formed thereon. A data conductor having a plurality of data lines 171 and a plurality of drain electrodes 175 is formed on the ohmic contacts 163 and 165 and gate insulating layer 140. Each data line 171 includes an end 179 of a plurality of source electrodes 173. A passivation layer 180 is formed on the data conductors 171 and 175 and the exposed region of the semiconductor 154, and a plurality of contact holes 181, 182 and 185 are formed on the passivation layer 180 and gate insulating layer 140. A plurality of pixel electrodes 191 and a plurality of contact assistants 81 and 82 are formed on the passivation layer. An alignment layer 11 is formed on the pixel electrode 191, the contact assistants 81 and 82, and the passivation layer 180.

[0066] Hereinafter, the upper panel will be described. A light blocking member 220, a plurality of color filters

230, an overcoat 250, a common electrode 270 and an alignment layer 21 are formed on an insulation substrate 210.

[0067] The liquid crystal panel assembly shown in FIG. 3 inversely drives a data voltage supplied from the data driver 500 to the data line 171 in a 3×1 manner. If three pixel electrodes adjacent in a row direction are the first pixel electrode 191a, the second pixel electrode 191b and the third pixel electrode 191c, and if a pixel electrode adjacent to the upper region of the first pixel electrode 191a is the fourth pixel electrode 191d, the voltage polarities of the first to third pixel electrodes 191a, 191b and 191c are positive (+) and the voltage polarity of the fourth pixel electrode 191d is negative (-).

[0068] A drain electrode 177a overlapping a storage electrode line 131a between the first pixel electrode 191a and the fourth pixel electrode 191d is overlapped with only one of the first and fourth pixel electrode 191a and 191d. That is, if the voltage polarities of the adjacent two pixel electrodes 191a and 191d are different, the drain electrode 177a is overlapped with only one of two pixel electrodes 191a and 191d.

[0069] On the contrary, the drain electrode 177b overlapping a storage electrode line 131b formed between the first pixel electrode 191a and the second pixel electrode 191b is overlapped with both of the first and second pixel electrodes 191a and 191b. A drain electrode 177c overlapping a storage electrode line 131c formed between the second pixel electrode 191b and the third pixel electrode 191c is also overlapped with both of the second and third pixel electrodes 191b and 191c. That is, if the voltage polarity of two adjacent pixel electrodes 191a and 191b, or 191b and 191c, are the same, the drain electrodes 177b and 177c are overlapped with both of two pixel electrodes (191a and 191b, or 191b and 191c).

[0070] When the voltage polarities of two adjacent pixel electrodes 191 are opposite, the voltage difference between two pixel electrodes 191 is large. If the drain electrode 177 is overlapped with both of two adjacent pixel electrodes 191, in this case, a parasitic capacitance is induced between each pixel electrode 191 and the drain electrode 177. The parasitic capacitance influences the voltages of the two adjacent pixel electrodes, thereby causing pixel quality deterioration. Accordingly, if the polarities of two adjacent pixel electrodes 191 are identical as in the present invention, an aperture ratio can be secured by overlapping the drain electrode 177 with two pixel electrodes 191. If polarities of two adjacent pixel electrodes 191 are opposite, the pixel quality deterioration can be prevented by overlapping the drain electrode 177 with one of the pixel electrodes 191.

[0071] The liquid crystal panel assembly according to the present alternative exemplary embodiment was described on a basis of a 3×1 inversion drive. However, the present invention is not limited thereto. The present invention can be applied to an mx1 inversion drive, where m is an integer greater than 2. That is, if the polarities of adjacent pixel electrodes 191 are opposite in the case of an mx1 inversion drive, the drain electrode 177 is overlapped with only one of the pixel electrodes 191. If the polarities of adjacent pixel electrodes 191 are the same, the drain electrode 177 is overlapped with both of two pixel electrodes 191.

[0072] According to the present invention, the number of data driving circuit chips disposed on the liquid crystal display can be reduced, cross-talk can be prevented and the aperture ratio can be secured.

Claims

1. A liquid crystal display (LCD) comprising:

a substrate (110);
a plurality of gate lines (121) formed on the substrate (110);
a plurality of data lines (171) crossing the gate lines (121);
a plurality of thin film transistors connected to the gate lines (121) and the data lines (171), and each thin film transistor including a drain electrode (175);
a plurality of pixel electrodes (191) connected to the thin film transistors, arranged in a matrix, and each pixel electrode (191) having a first side disposed in parallel with the gate lines (121) and a second side, disposed in parallel with the data lines (171), shorter than the first side, wherein a predetermined portion of each of the drain electrodes (175) is disposed between adjacent pixel electrodes (191), and
a data driver (500) coupled to the data lines (171) for applying a voltage having positive polarity or negative polarity to the pixel electrodes (191), wherein the data driver (500) is able to drive the display in an mx1 inversion scheme with m being an integer greater than 2;

wherein a predetermined portion of those of the drain electrodes (175), the respective adjacent pixel electrodes (191) of which are subject to different polarities in accordance with the mx1 inversion driving scheme, is overlapped with only one of their respective adjacent pixel electrodes (191), and wherein a predetermined portion of the other of the drain electrodes (175), the respective adjacent pixel electrodes (191) of which are subject to the same polarity in accordance with the mx1 inversion driving scheme, is overlapped with both of their respective adjacent pixel electrodes (191).

2. The liquid crystal display (LCD) of claim 1, wherein the data driver is adapted to drive the polarity of the pixel electrodes (191) in an m x 1 inversion-drive manner, wherein the voltage polarity of m pixel electrodes (191a, 191b, 191c) adjacent to each other in

a row direction are positive (+) and the voltage polarity of one pixel electrode (191d) adjacent to the first one of pixel electrodes (191a, 191b, 191c) is negative (-).

3. The liquid crystal display (LCD) of claim 2, wherein m is 3.

4. The liquid crystal display (LCD) of claim 1, further comprising a storage electrode line (131) overlapped with a respective pixel electrode (191) and the drain electrode (175).

5. The liquid crystal display (LCD) of claim 4, wherein predetermined portions of the drain electrode (175) and the storage electrode line (131) are disposed between adjacent pixel electrodes (191) in a column direction.

6. The liquid crystal display (LCD) of claim 1, wherein each pixel electrode (191) covers a previous gate line (121).

7. The liquid crystal display (LCD) of claim 1, further comprising an organic layer (180) formed between each pixel electrode (191) and the data lines (171), and between each pixel electrode (191) and the gate lines (121).

8. The liquid crystal display (LCD) of claim 1, wherein the length of the first side is three times longer than that of the second side.

9. The liquid crystal display (LCD) of claim 1, further comprising a gate driver (400) connected to the gate lines (121),
wherein the gate driver (400) is placed at the same layer as the gate lines (121), the data lines (171) and the thin film transistors.

10. The liquid crystal display (LCD) of claim 1, wherein the plurality of pixel electrodes (191) comprises first, second and third pixel electrodes (191 a, 191b, 191c), which are connected to the thin film transistors, respectively, each of the first, second and third pixel electrodes (191 a, 191b, 191 c) having a first side disposed in parallel with the gate lines (121) and a second side shorter than the first side, and are adjacent in a column direction,
wherein the driver is adapted to drive polarities of the second and third pixel electrodes (191b, 191c) so as to be the same, and so that the polarity of the first pixel electrode (191a) is opposite to the polarity of the second and third pixel electrodes (191b, 191c),
wherein a first drain electrode (177b) is disposed between the first and second pixel electrodes (191 a, 191 b), and a second drain electrode (177c) is disposed between the second and third pixel electrodes (191b, 191c), and
wherein the first drain electrode (177b) is overlapped only with the first pixel electrode (191a) of the first, second and third pixel electrodes (191a, 191b, 191c), and the second drain electrode (177c) is overlapped with both of the second and third pixel electrodes (191b, 191 c).

11. The liquid crystal display (LCD) of claim 10, further comprising a storage electrode line (131) overlapped with corresponding pixel and drain electrodes (191; 177).

12. The liquid crystal display (LCD) of claim 10, wherein each of the first, second and third pixel electrodes (191 a, 191 b, 191 c) covers a previous gate line (121).

13. The liquid crystal display (LCD) of claim 10, further comprising an organic layer formed between each of the first, second and third pixel electrodes (191 a, 191b, 191 c) and the data lines (171), and between each of the first, second and third pixel electrodes (191a, 191b, 191c) and the gate lines (121).

14. The liquid crystal display (LCD) of claim 10, wherein the length of the first side is three times longer than that of the second side.

15. The liquid crystal display (LCD) of claim 10, further comprising a gate driver (400) connected to the gate lines (121),
wherein the gate driver (400) is placed on the same layer of the gate lines (121), the data lines (171) and the thin film transistors.

Patentansprüche

1. Flüssigkristallanzeige (LCD), die Folgendes umfasst:

ein Substrat (110);
eine Mehrzahl von auf dem Substrat (110) ausgebildeten Gate-Leitungen (121);
eine Mehrzahl von Datenleitungen (171), welche die Gate-Leitungen (121) kreuzen;
eine Mehrzahl von Dünnschichttransistoren, die mit den Gate-Leitungen (121) und den Datenleitungen (171) verbunden sind, wobei jeder Dünnfilmtransistor eine Drain-Elektrode (175) umfasst;
eine Mehrzahl von mit den Dünnschichttransistoren verbundenen Pixel-Elektroden (191), die in einer Matrix angeordnet sind, wobei jede Pixel-Elektrode (191) eine erste Seite aufweist, die parallel zu den Gate-Leitungen (121) angeordnet ist, und eine zweite, parallel zu den Da-

tenleitungen (171) angeordnete Seite, die kürzer ist als die erste Seite,
wobei ein bestimmter Abschnitt jeder Drain-Elektrode (175) zwischen angrenzenden Pixel-Elektroden (191) angeordnet ist, und
einen mit den Datenleitungen (171) gekoppelten Datentreiber (500) zum Anlegen einer Spannung mit einer positiven Polarität oder einer negativen Polarität an die Pixel-Elektroden (191),
wobei der Datentreiber (500) geeignet ist, die Anzeige in einem mx1-Inversionsschema anzusteuern,
wobei m größer ist als 2;
wobei ein bestimmter Abschnitt jener der Drain-Elektroden (175), deren entsprechende angrenzende Pixel-Elektroden (191) unterschiedlichen Polaritäten gemäß dem mx1 Inversions-Ansteuerschema ausgesetzt sind, von nur einer ihrer jeweils angrenzenden Pixel-Elektroden (191) überlappt ist, und wobei ein bestimmter Abschnitt der anderen Drain-Elektroden (175), deren entsprechende angrenzende Pixel-Elektroden (191) der selben Polarität gemäß dem mx1 Inversions-Ansteuerschema ausgesetzt sind, von beiden ihrer jeweils angrenzenden Pixel-Elektroden (191) überlappt ist.

2. Flüssigkristallanzeige (LCD) gemäß Anspruch 1, wobei der Datentreiber so ausgeführt ist, dass er die Polarität der Pixel-Elektroden (191) per mx1 Inversions-Ansteuerung zu steuern vermag, wobei die Spannungspolarität von m Pixel-Elektroden (191a, 191b, 181c), die in einer Zeilenrichtung aneinander angrenzen, positiv (+) ist, und die Spannungspolarität einer Pixel-Elektrode (191d), die an die erste der Pixel-Elektroden (191a, 191b, 191 c) angrenzt, negativ (-) ist.

3. Flüssigkristallanzeige (LCD) gemäß Anspruch 2, wobei m gleich 3 ist.

4. Flüssigkristallanzeige (LCD) gemäß Anspruch 1, die ferner eine Speicherelektrodenleitung (131) umfasst, die von einer entsprechenden Pixel-Elektrode (191) und der Drain-Elektrode (175) überlappt ist.

5. Flüssigkristallanzeige (LCD) gemäß Anspruch 4, wobei bestimmte Abschnitte der Drain-Elektrode (175) und der Speicherelektrodenleitung (131) zwischen angrenzenden Pixel-Elektroden (191) in Spaltenrichtung angeordnet sind.

6. Flüssigkristallanzeige (LCD) gemäß Anspruch 1, wobei jede Pixel-Elektrode (191) eine vorhergehende Gate-Leitung (121) abdeckt.

7. Flüssigkristallanzeige (LCD) gemäß Anspruch 1, ferner umfassend eine organische Schicht (180), die zwischen jeder Pixel-Elektrode (191) und den Datenleitungen (171) und zwischen jeder Pixel-Elektrode (191) und den Gate-Leitungen (121) gebildet ist.

8. Flüssigkristallanzeige (LCD) gemäß Anspruch 1, wobei die Länge der ersten Seite dreimal größer ist als die der zweiten Seite.

9. Flüssigkristallanzeige (LCD) gemäß Anspruch 1, ferner umfassend einen Gate-Treiber (400), der mit den Gate-Leitungen (121) verbunden ist,
wobei der Gate-Treiber (400) auf der selben Schicht wie die Gate-Leitungen (121), die Datenleitungen (171) und die Dünnschichttransistoren platziert ist.

10. Flüssigkristallanzeige (LCD) gemäß Anspruch 1, wobei die Mehrzahl von Pixel-Elektroden (191) erste, zweite und dritte Pixel-Elektroden (191a, 191 b, 191 c) umfasst, die jeweils mit den Dünnschichttransistoren verbunden sind, wobei jede der ersten, zweiten und dritten Pixel-Elektroden (191a, 191b, 191c) eine erste Seite aufweist, die parallel zu den Gate-Leitungen (121) angeordnet ist, und eine zweite Seite, die kürzer als die erste Seite ist, und wobei diese in Spaltenrichtung angrenzend angeordnet sind,
wobei der Treiber geeignet ist, die Polaritäten der zweiten und dritten Pixel-Elektroden (191b, 181c) zu steuern, damit diese Identisch seien und damit die Polarität der ersten Pixel-Elektrode (191a) der Polarität der zweiten und dritten Pixel-Elektroden (191b, 191c) entgegengesetzt sei,
wobei eine erste Drain-Elektrode (177b) zwischen der ersten und der zweiten Pixel-Elektrode (191a, 191b) angeordnet ist und eine zweite Drain-Elektrode (177c) zwischen der zweiten und der dritten Pixel-Elektrode (191b, 191c) angeordnet ist, und
wobei die erste Drain-Elektrode (177b) nur von der ersten Pixel-Elektrode (191a) der ersten, zweiten und dritten Pixel-Elektroden (191a, 181b, 191c) überlappt ist und die zweite Drain-Elektrode (177c) von der zweiten und der dritten Pixel-Elektrode (191b, 191c) überlappt ist.

11. Flüssigkristallanzeige (LCD) gemäß Anspruch 10, ferner umfassend eine Speicherelektrodenleitung (131), die von den entsprechenden Pixel- und Drain-Elektroden (191; 177) überlappt ist.

12. Flüssigkristallanzeige (LCD) gemäß Anspruch 10, wobei jede der ersten, zweiten und dritten Pixel-Elektroden (191a, 191b, 191c) eine vorhergehende Gate-Leitung (121) abdeckt.

13. Flüssigkristallanzeige (LCD) gemäß Anspruch 10, ferner eine organische Schicht umfassend, die zwischen jeder der ersten, zweiten und dritten Pixel-Elektrode (191a, 191b, 191c) und den Datenleitun-

gen (171) und zwischen jeder der ersten, zweiten und dritten Pixel-Elektroden (191a, 191b, 191c) und den Gate-Leitungen (121) ausgebildet sind.

14. Flüssigkristallanzeige (LCD) gemäß Anspruch 10, wobei die Länge der ersten Seite dreimal größer ist als die der zweiten Seite.

15. Flüssigkristallanzeige (LCD) gemäß Anspruch 10, ferner einen mit den Gate-Leitungen (121) verbundenen Gate-Treiber (400) umfassend,
wobei der Gate-Treiber (400) auf der selben Schicht wie die Gate-Leitungen (121), der Datenleitungen (171) und der Dünnschichttransistoren platziert ist.

Revendications

1. Afficheur à cristaux liquides (LCD) comprenant :

un substrat (110) ;
une pluralité de lignes de grille (121) formées sur le substrat (110) ;
une pluralité de lignes de données (171) croisant les lignes de grille (121) ; une pluralité de transistors en couche mince connectés aux lignes de grille (121) et aux lignes de données (171), chaque transistor en couche mince comprenant une électrode de drain (175) ;
une pluralité d'électrodes de pixel (191) connectées aux transistors en couche mince, disposées sous forme de matrice, chaque électrode de pixel (191) ayant un premier côté disposé parallèlement aux lignes de grille (121) et un deuxième côté disposé parallèlement aux lignes de données (171) et
plus court que le premier côté, une partie prédéterminée de chacune des électrodes de drain (175) étant disposée entre des électrodes de pixel (181) adjacentes, et
un pilote de données (500) couplé aux lignes de données (171) pour appliquer une tension de polarité positive ou négative aux électrodes de pixel (191), lequel pilote de données (500) peut piloter l'afficheur selon un mode d'inversion m $\times$ 1 où m est un nombre entier supérieur à 2 ;

dans lequel une partie prédéterminée des électrodes de drain (175) dont les électrodes de pixel (191) adjacentes sont soumises à des polarités différentes selon le mode de pilotage en inversion m $\times$ 1 est recouverte par seulement une des électrodes de pixel (191) qui lui sont adjacentes, et dans lequel une partie prédéterminée des autres électrodes de drain (175) dont les électrodes de pixel (191) adjacentes sont soumises à la même polarité selon le mode de pilotage en inversion m $\times$ 1 est recouverte par les deux électrodes de pixel (191) qui leur sont adjacentes.

2. Afficheur à cristaux liquides (LCD) selon la revendication 1, dans lequel le pilote de données est adapté pour piloter la polarité des électrodes de pixel (191) selon un mode de pilotage en inversion m $\times$ 1, la polarité de tension de m électrodes de pixel (191a, 191b, 191c) adjacentes les unes aux autres dans le sens d'une rangée étant positive (+) et la polarité de tension d'une électrode de pixel (191d) adjacente à la première des électrodes de pixel (191a, 191b, 191c) étant négative (-).

3. Afficheur à cristaux liquides (LCD) selon la revendication 2, dans lequel m est 3.

4. Afficheur à cristaux liquides (LCD) selon la revendication 1, comprenant en outre une ligne d'électrodes de stockage (131) recouverte par une électrode de pixel (191) correspondante et par l'électrode de drain (175),

5. Afficheur à cristaux liquides (LCD) selon la revendication 4, dans lequel des parties prédéterminées de l'électrode de drain (175) et de la ligne d'électrodes de stockage (131) est disposée entre des électrodes de pixel (191) adjacentes dans le sens d'une colonne.

6. Afficheur à cristaux liquides (LCD) selon la revendication 1, dans lequel chaque électrode de pixel (191) recouvre une ligne de grille (121) qui la précède.

7. Afficheur à cristaux liquides (LCD) selon la revendication 1, comprenant en outre une couche organique (180) formée entre chaque électrode de pixel (191) et les lignes de données (171) et entre chaque électrode de pixel (191) et les lignes de grille (121).

8. Afficheur à cristaux liquides (LCD) selon la revendication 1, dans lequel la longueur du premier côté est trois fois plus grande que celle du deuxième côté.

9. Afficheur à cristaux liquides (LCD) selon la revendication 1, comprenant en outre un pilote de grille (400) connecté aux lignes de grille (121), lequel pilote de grille (400) est placé dans la même couche que les lignes de grille (121), les lignes de données (171) et les transistors en couche mince.

10. Afficheur à cristaux liquides (LCD) selon la revendication 1, dans lequel la pluralité d'électrodes de pixel (191) comprend des première, deuxième et troisième électrodes de pixel (181a, 181b, 191c), qui sont connectées respectivement aux transistors en couche mince, chacune des première, deuxième et troisième électrodes de pixel (191a, 191b, 191c) ayant un premier côté disposé parallèlement aux lignes de

grille (121) et un deuxième côté plus court que le premier côté et étant adjacentes dans le sens d'une colonne,
dans lequel le pilote est adapté pour piloter les polarités des deuxième et troisième électrodes de pixel (191b, 191c) de telle façon qu'elles soient identiques, et de telle façon que la polarité de la première électrode de pixel (191a) soit opposée à la polarité des deuxième et troisième électrodes de pixel (191b, 191c),
dans lequel une première électrode de drain (177b) est disposée entre les première et deuxième électrodes de pixel (191a, 191b), et une deuxième électrode de drain (177c) est disposée entre les deuxième et troisième électrodes de pixel (191b, 191c), et dans lequel la première électrode de drain (177b) n'est recouverte que par la première électrode de pixel (191a) des première, deuxième et troisième électrodes de pixel (191a, 191b, 191c), et la deuxième électrode de drain (177c) est recouverte à la fois par la deuxième électrode de pixel et par la troisième (191b, 191c).

11. Afficheur à cristaux liquides (LCD) selon la revendication 10, comprenant en outre une ligne d'électrodes de stockage (131) recouverte par les électrodes de pixel et de drain (191 ; 177) correspondantes.

12. Afficheur à cristaux liquides (LCD) selon la revendication 10, dans lequel chacune des première, deuxième et troisième électrodes de pixel (191a, 191b, 181c) couvre une ligne de grille (121) qui la précède.

13. Afficheur à cristaux liquides (LCD) selon la revendication 10, comprenant en outre une couche organique formée entre chacune des première, deuxième et troisième électrodes de pixel (191 a, 191 b, 191c) et les lignes de données (171), et entre chacune des première, deuxième et troisième électrodes de pixel (191a, 191b, 191c) et les lignes de grille (121).

14. Afficheur à cristaux liquides (LCD) selon la revendication 10, dans lequel la longueur du premier côté est trois fois plus grande que celle du deuxième côté.

15. Afficheur à cristaux liquides (LCD) selon la revendication 10, comprenant en outre un pilote de grille (400) connecté aux lignes de grille (121), lequel pilote de grille (400) est placé sur la même couche que les lignes de grille (121), les lignes de données (171) et les transistors en couche mince.

FIG.1

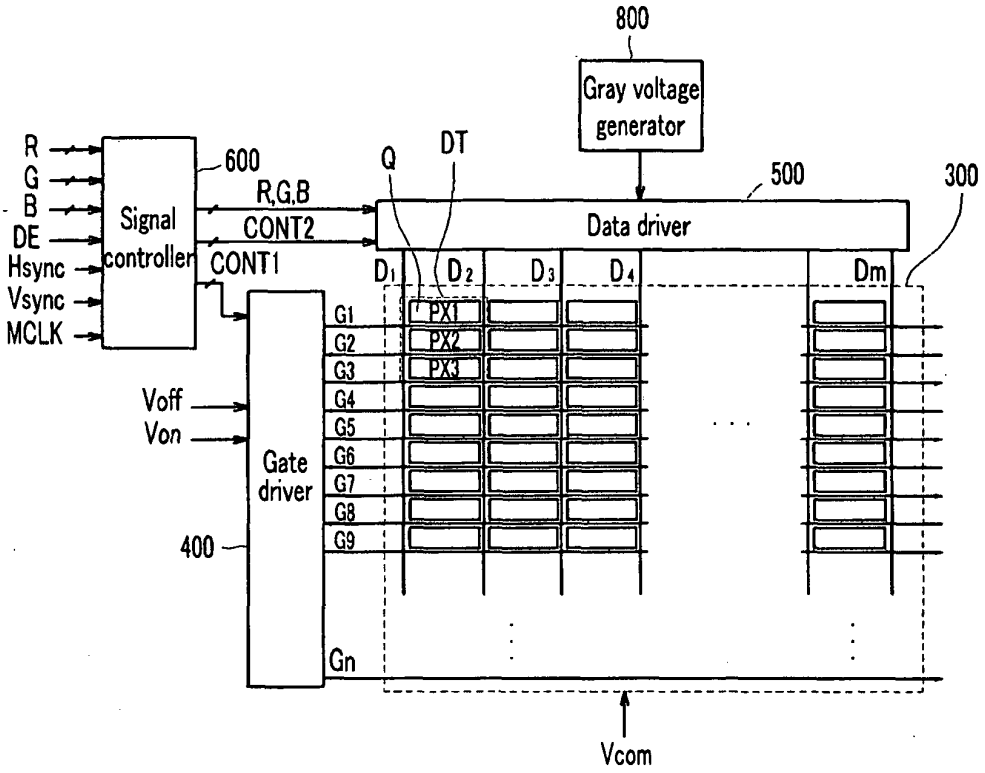

800
Gray voltage generator
R
G
B
DE
Hsync
Vsync
MCLK
Signal controller
600
R,G,B
CONT2
CONT1
Q
DT
500
Data driver
300
D1
D2
D3
D4
Dm
PX1
PX2
PX3
G1
G2
G3
G4
G5
G6
G7
G8
G9
Gn
Voff
Von
Gate driver
400
Vcom

FIG.2

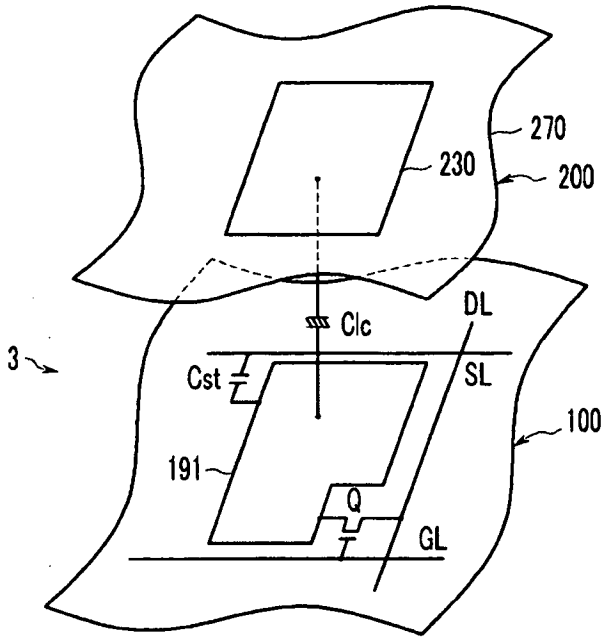


FIG.3

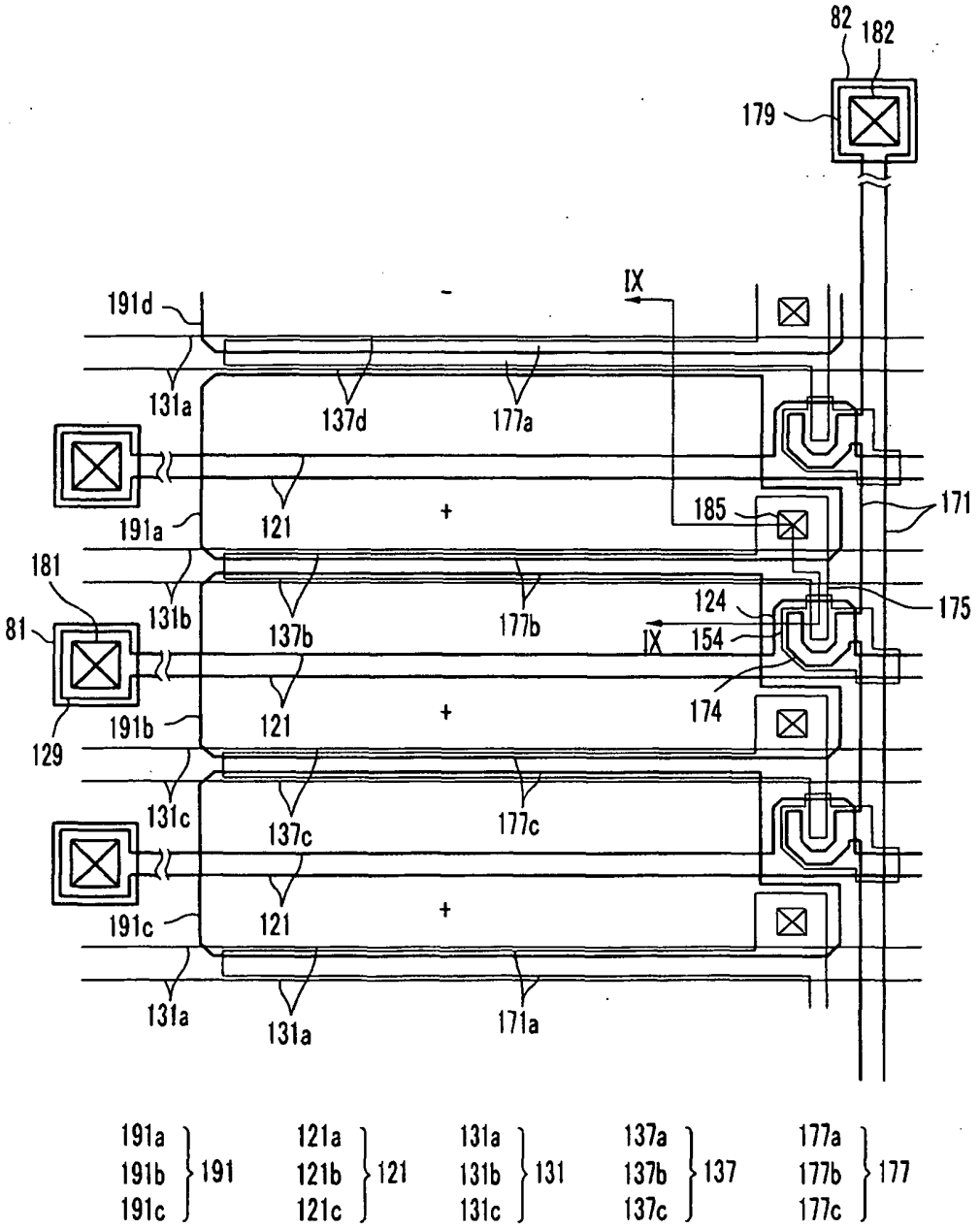
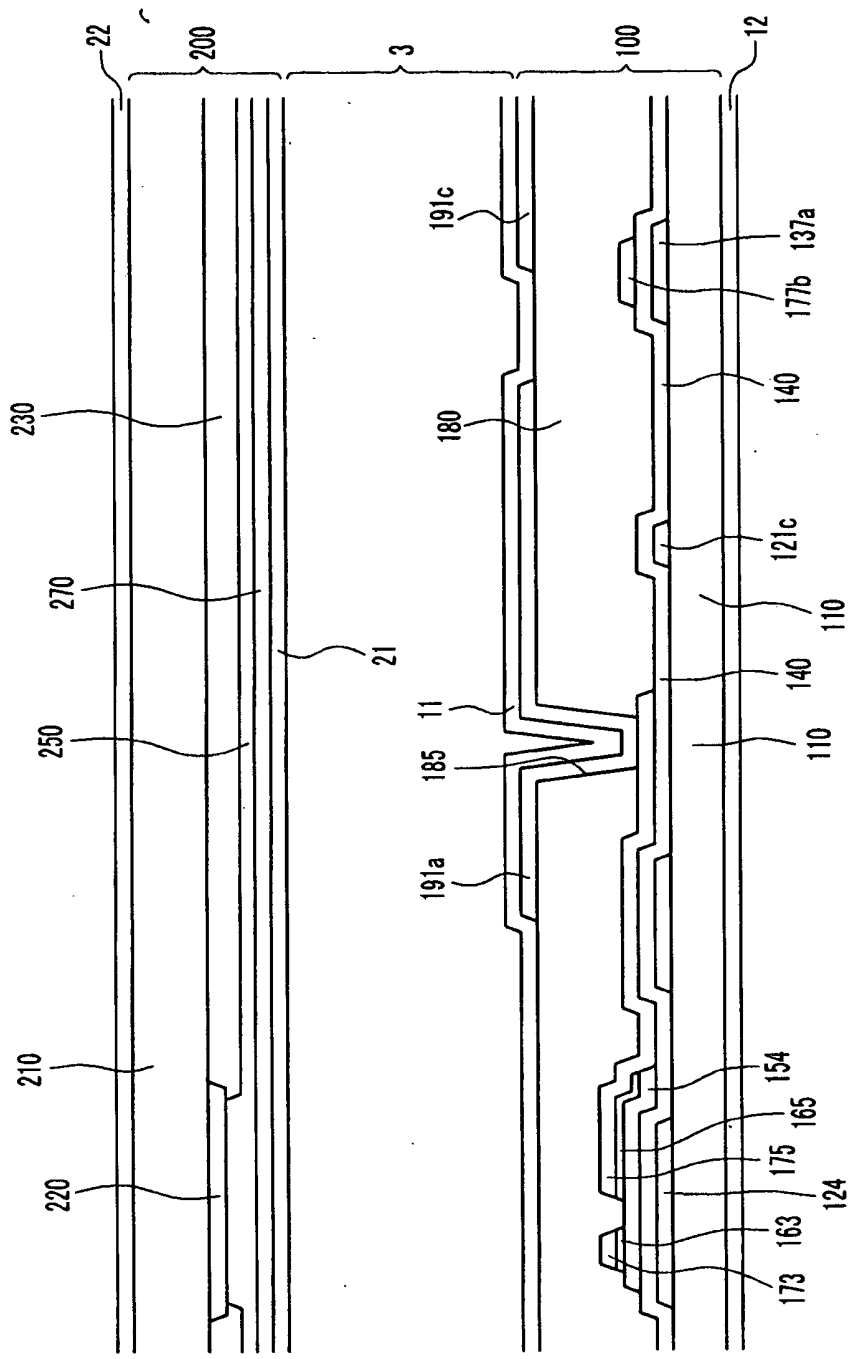

82
182
179
191d
131a
137d
177a
IX
191a
121
185
171
181
131b
137b
177b
124
175
81
IX
154
129
191b
121
174
131c
137c
177c
191c
121
131a
131a
171a
191a
191b
191c
191
121a
121b
121c
121
131a
131b
131c
131
137a
137b
137c
137
177a
177b
177c
177

FIG.4


22
200
3
100
12
191c
137a
177b
140
180
121c
230
270
110
21
140
11
250
185
110
191a
154
165
175
124
210
163
220
173

REFERENCES CITED IN THE DESCRIPTION

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- US 2005167669 A1 **[0006]**
- EP 0752611 A2 **[0007]**
- US 2003043328 A1 **[0008]**

专利名称(译)	液晶显示器		
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外部链接	Espacenet		

摘要(译)

液晶显示器（LCD）包括基板，栅极线（121），数据线（171），薄膜晶体管（174）和像素电极（191）。栅极线形成在基板上并与数据线交叉。薄膜晶体管连接到栅极线和数据线，并且每个薄膜晶体管包括漏电极。像素电极连接到薄膜晶体管并且布置成矩阵，并且每个像素电极具有与栅极线平行设置的第一侧和与第一侧相邻且比第一侧短的第二侧。在LCD中，如果相邻像素电极的极性不同，则漏电极的预定部分（137a，137d）仅与两个相邻像素电极中的一个重叠，并且漏电极的预定部分（137b，137c）如果极性相同，则与两个相邻的像素电极重叠。

FIG.1