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(54) **LCD panel array substrates**

Substrate für LCD-Anzeigetafelanordnungen

Substrats de réseau à panneau LCD

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Description

RELATED APPLICATIONS

[0001] This application claims priority of Korean Patent Application No. 2006-60413, filed June 30, 2006.

BACKGROUND

[0002] This disclosure relates to liquid crystal displays (LCDs), in general, and in particular, to array substrates for LCD panels that improve the image quality of display panels incorporating them.

[0003] LCDs typically include an LCD panel that displays an image using the optical characteristics of a liquid crystal material, and a backlight assembly disposed behind the panel for projecting light though the panel.

[0004] The LCD panel typically includes an array substrate, a color filter substrate facing the array substrate, and a layer of the liquid crystal material interposed between the two substrates.

[0005] The array substrate includes gate and data lines that are disposed substantially perpendicular to each other to define a plurality of rectangular unit pixels, along with thin film transistors that are electrically connected to the gate and data lines, pixel electrodes that are formed in the unit pixels and electrically connected to the thin film transistors, and storage lines that overlap the pixel electrodes. The storage lines are arranged to overlap the pixel electrodes so as to form storage capacitors that maintain the voltage applied to each pixel electrode during one image frame.

[0006] The elements of the array substrate are typically formed through a photolithography process. For example, the pixel electrodes may be formed through an entire-surface deposition, or by an exposure-by-mask and an etching process. Recently, as the size of array substrates has become large in comparison with that of the masks used to produce them, the exposure-by-mask process must be performed repetitively in order to expose a single substrate. That is, the mask must be moved by a predetermined distance between each of the multiple exposures of the substrate.

[0007] However, when the pixel electrodes are formed through such a multiple exposure process, the pixel electrodes may be slightly misaligned with respect to the gate lines, the data lines and the storage lines. When the pixel electrodes are misaligned with respect to the storage lines, the storage capacitors that are formed between the pixel electrodes and the storage lines can vary spatially, and as a result, generate varying kickback voltages that cause flicker defects that deteriorate the image quality of the display.

[0008] Document US 5 943 160 discloses a plurality of control and data bus lines formed on the surface of an insulating substrate. A pixel electrode and a switching element are formed at an area corresponding to each interconnection portion between the control and data bus lines. A plurality of capacitor bus lines are formed on the surface of the interlayer insulating substrate for forming an auxiliary capacitor between the pixel electrode and capacitor bus line. The capacitor bus line has an auxiliary capacitor pattern branching from the capacitor bus line and extending along the data bus line. This auxiliary capacitor pattern is constituted of a cutting portion and a remaining main portion. A space between the cutting portion and a corresponding data bus line is broader than that between the main portion and the corresponding data bus line.

BRIEF SUMMARY

[0009] In accordance with the exemplary embodiments thereof described herein, LCD panel array substrates are provided that improve display image quality by preventing the storage capacitors of the substrates from being adversely changed due to misalignment of the pixel electrodes thereof.

[0010] In one exemplary embodiment, an LCD panel array substrate includes a gate line, a data line, a thin film transistor, a pixel electrode and a storage line. The gate line is formed in a first direction. The data line is formed in a second direction that crosses the first direction. The thin film transistor is electrically connected to the gate line and the data line. The pixel electrode is formed in a unit pixel area defined by the gate line and the data line and is electrically connected to the thin film transistor.

[0011] The storage line includes a main storage line, a first sub storage line and a second sub storage line. The main storage line is formed in the second direction. The first sub storage line is connected to the main storage line and extends in the first direction. The first sub storage line overlaps a first edge portion of the pixel electrode by a first length. The second sub storage line is connected to the main storage line and extends in the first direction. The second sub storage line overlaps a second edge portion of the pixel electrode opposite to the first edge portion thereof by the first length. For example, the first sub storage line may extend in the first direction by the first length, and the second sub storage line may extend in the first direction by a second length that is longer than the first length.

[0012] When the second sub storage line includes an overlapping storage electrode that overlaps the second edge portion of the pixel electrode by the first length, and a non-overlapping storage electrode that is connected to the overlapping storage electrode that does not overlap the second edge portion of the pixel electrode, the overlapping storage electrode may be offset, or curved from, the non-overlapping storage electrode and toward the pixel electrode, and in one alternative embodiment, a width of the overlapping storage electrode may be wider than a width of the non-overlapping storage electrode.

[0013] The pixel electrode may include a main pixel electrode that does not overlap the second sub storage

line, and an overlapping electrode that extends from the main pixel electrode toward the second sub storage line so as to overlap the second sub storage line by the first length.

[0014] In another exemplary embodiment, an LCD display panel includes an array substrate, a counter substrate facing the array substrate, and a layer of a liquid crystal material disposed between the array substrate and the counter substrate.

[0015] The array substrate includes a gate line formed in a first direction, a data line formed in a second direction substantially perpendicular to the first direction, a thin film transistor electrically connected to the gate line and the data line, a pixel electrode that is formed in a unit pixel defined by the gate line and the data line to have a substantially rectangular shape and which is electrically connected to the thin film transistor, and a storage line comprising a main storage line formed in the second direction, a first sub storage line that is connected to the main storage line and that extends in the first direction, the first sub storage line overlapping a first edge portion of the pixel electrode by a first length, and a second sub storage line that is connected to the main storage line and that extends in the first direction, the first sub storage line overlapping a second edge portion of the pixel electrode opposite to the first edge portion by the first length.

[0016] In this exemplary embodiment, the length of the overlap between the first sub storage line and the first edge portion of the pixel electrode is substantially the same as the length of the overlap between the second sub storage line and the second edge portion of the pixel electrode so as to prevent the storage capacitor associated with the pixel electrode and storage line from varying due to a misalignment of the pixel electrode, thereby improving the image quality of the display panel.

[0017] A better understanding of the above and many other features and advantages of the novel LCD panel array substrates of the present invention may be obtained from a consideration of the detailed description of some exemplary embodiments thereof below, particularly if such consideration is made in conjunction with the appended drawings, wherein like reference numerals are used to identify like elements illustrated in one or more of the figures thereof.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018]

FIG. 1 is a cutaway perspective view of an exemplary embodiment of an LCD display panel in accordance with the present invention;

FIG. 2 is schematic partial plan view of a first exemplary embodiment of an array substrate of the exemplary display panel of FIG. 1;

FIG. 3 is an enlarged partial plan view of a portion of the exemplary array substrate of FIG. 2;

FIG. 4 is an enlarged plan view of the portion "A" of the array substrate outlined by phantom lines in FIG. 3;

FIG. 5 is a partial cross-sectional view of the array substrate as seen along the lines of the section I-I' taken in FIG. 4;

FIG. 6 is an enlarged partial plan view of a portion of a second exemplary embodiment of a display panel array substrate in accordance with the present invention;

FIG. 7 is a cross-sectional view of the second exemplary array substrate as seen along the lines of the section II-II' taken in FIG. 6;

FIG. 8 is a cross-sectional view of the second exemplary array substrate as seen along the lines of the section III-III' taken in FIG. 6;

FIG. 9 is an enlarged partial plan view of a portion of a third exemplary embodiment of a display panel array substrate in accordance with the present invention;

FIG. 10 is an enlarged partial plan view of a portion of a fourth exemplary embodiment of a display panel array substrate in accordance with the present invention; and,

FIG. 11 is an enlarged partial plan view of a portion of a fifth exemplary embodiment of a display panel array substrate in accordance with the present invention.

DETAILED DESCRIPTION

Embodiment 1 (Display Panel)

[0019] An exemplary embodiment of an LCD display panel 400 in accordance with the present invention is illustrated in the cutaway perspective view of FIG. 1. As illustrated in FIG. 1, the display panel 400 includes an array substrate 100, a counter substrate 200, and a layer of a liquid crystal material 300 interposed between the two substrates. As described above, the panel 400 is operable to display an image on the upper or front surface of the panel using light transmitted through the opposite lower or rear surface thereof.

[0020] The array substrate 100 includes a plurality of pixel electrodes arranged in a matrix form thereon, a plurality of thin film transistors that apply driving voltages to respective ones of the pixel electrodes, and a plurality of signal lines electrically connected to respective ones of the thin film transistors.

[0021] The counter substrate 200 is disposed in a spaced, facing opposition to the front side of the array substrate 100 and includes a transparent conductive common electrode and color filters that face the pixel electrodes. The color filters may include, for example, red, green, and blue (RGB) color filters.

[0022] The liquid crystal layer 300 is disposed between the array substrate 100 and the counter substrate 200, and is acted upon by an electric field generated between the pixel electrode and the common electrode such that

the molecules of the liquid crystal layer 300 are thereby controllably rearranged. The rearranged molecules of the liquid crystal layer 300 adjust the optical transmissivity of light passing though the panel, and the light passes through the color filters so as to display images.

[0023] FIG. 2 is schematic partial plan view of a first exemplary embodiment of an array substrate 100 of the exemplary LCD display panel of FIG. 1. As illustrated in FIG. 2, the exemplary array substrate 100 includes a plurality of gate lines 110, a plurality of data lines 120, and a plurality of pixel electrode 130. The gate lines 110 are formed to extend in a first direction, as indicated by the arrows in FIG. 2, and the data lines 120 are formed to extend in a second direction that is substantially perpendicular to the first direction, as indicated by the arrows. In the particular exemplary embodiment of FIG. 2, nine gate lines GL1 - GL9 and seven data lines DL1 - DL7 are shown for purposes of illustration, but these numbers can, of course, vary substantially.

[0024] The gate lines GL1 - GL9 are electrically connected to a gate driving part (not illustrated) to receive gate signals, and the data lines DL1- DL7 are electrically connected to a data driving part (not illustrated) to receive data signals. The gate driving part includes a left gate driving part (not illustrated) that is electrically connected to a left end portion of the odd-numbered gate lines, GL1 ... GL9, and a right gate driving part (not illustrated) that is electrically connected to a right end portion of even-numbered gate lines, GL2 ... GL8. Alternatively, the gate driving part may comprise a single part electrically connected to an end portion of all of the gate lines GL1-GL9.

[0025] As discussed above, the gate lines GL1 - GL9 are arranged substantially perpendicular to the data lines DL1- DL7 so as to define a rectangular array of unit pixels on the array substrate 100. Each pixel electrode 130 is formed in a respective one of the unit pixels, and thus, a plurality of pixel electrodes 130 is arranged in the form of a matrix on the array substrate 100.

[0026] In one exemplary embodiment, each unit pixel has a substantially rectangular shape, with a long side thereof extending in the first direction, and accordingly, the associated pixel electrode 130 formed therein likewise has a long side that extends in the first direction.

[0027] The gate lines GL1 -GL9, the data lines DL1 - DL7 and the pixel electrodes 130 are electrically interconnected in the following manner. Each of the gate lines GL1 - GL9 is electrically connected to all of the pixel electrodes 130 in a corresponding one of the rows of pixels. In contrast, data line DL1 of the data lines DL1- DL7, which is disposed leftmost in FIG. 2, is electrically connected to the pixel electrodes 130 of the odd numbered rows of pixels in the first column of pixels, at the left side thereof, and data line DL7, which is disposed rightmost in Fig. 2, is electrically connected to the pixel electrodes 130 of the even numbered rows of pixels in the sixth column of pixels, at the right side thereof. Each of the remaining data lines DL2 ... DL6 is electrically connected to the pixel electrodes 130 of the two pixel columns on either side thereof in an analogous manner, *i.e.,* on the left side of the data lines, to pixel electrodes 130 in the even numbered pixel rows, and on the right side, to pixel electrodes 130 in the odd numbered pixel rows, as illustrated schematically in FIG. 2.

[0028] In one exemplary embodiment, data signals adapted to effect "vertical inversion" of the panel may be applied to the data lines DL1 - DL7. Specifically, in one frame, a data signal having a positive voltage is applied to a selected data line, and a data signal having a negative voltage is applied to the data line adjacent to the selected data line. In the next frame, a data signal having a negative voltage is applied to the selected data line, and a data signal having a positive voltage is applied to the data line adjacent to the selected data line.

[0029] FIG. 3 is an enlarged partial plan view of a portion of the exemplary array substrate 100 of FIG. 2, FIG. 4 is an enlarged plan view of the portion "A" of the array substrate outlined by phantom lines in FIG. 3, and FIG. 5 is a partial cross-sectional view of the array substrate as seen along the lines of the section I-I' taken in FIG. 4.

[0030] As illustrated in FIGS. 3 - 5, the exemplary array substrate 100 includes a first optically transparent substrate 140, a gate line 110, a gate insulation layer 150, a data line 120, a storage line 160, a thin film transistor TFT, a first connection electrode 170, a second connection electrode 180, a protective layer 190 and a pixel electrode 130.

[0031] The first transparent substrate 140 has, for example, a plate shape, and is comprised of an optically transparent material. The gate line 110 is formed on the first transparent substrate 140. The gate insulation layer 150 is formed on the first transparent substrate 140 so as to cover the gate line 130. The data line 120, the storage line 160, the first connection electrode 170 and the second connection electrode 180 are all formed on the gate insulation layer 150.

[0032] As illustrated in FIGS. 4 and 5, the thin film transistor TFT includes a gate electrode "G", a source electrode "S", a drain electrode "D", an active layer "A" and an ohmic contact layer "O". The gate electrode G corresponds to a part of the gate line 110, and the active layer A is formed on the gate insulation layer 150 to correspond to the gate electrode G. The source electrode S overlaps the active layer A, and extends, for example, from the data line 120 to have an L-shape. The drain electrode D is spaced apart from the source electrode S by a selected distance, and partially overlaps the active layer A. As illustrated in FIG. 5, the ohmic contact layer O is respectively formed between the active layer A and the source electrode S, and between the active layer A and the drain electrode D.

[0033] The protective layer 190 is formed on the gate insulation layer 190 so as to cover the data line 120, the storage line 160, the first connection electrode 170, the second connection electrode 180 and the thin film transistor TFT. First and second contact holes 192 and 194

are formed through the protective layer 190 at locations respectively corresponding to the first and second connection electrodes 170 and 180. The pixel electrode 130 is formed on the protective layer 190, and is electrically connected to the first and second connection electrodes 170 and 180 through the first and second contact holes 192 and 194, respectively. As illustrated in the plan view of FIG. 3, the pixel electrode 130 may have a substantially rectangular shape.

[0034] As further illustrated in the plan view of FIG. 3, the exemplary display panel 400 includes a plurality of gate lines 110 extending in the first direction and a plurality of orthogonal data lines 120 extending in the second direction. Each of the pixel electrodes 130 is formed in a respective one of the unit pixels, which are defined by adjacent pairs of the gate lines 110 and the data lines 120.

[0035] For each pixel electrode 130, the associated gate line 110 may be formed at either one of an upper portion and a lower portion of the pixel electrode 130, and as illustrated in FIG. 3, may be formed at the lower portion of the pixel electrode 130. A data line 120 is formed at the left side and the right side of the pixel electrode 130, with the left data line 122 being formed at the left side of the pixel electrode 130 and the right data line 124 being formed at the right side of the pixel electrode 130.

[0036] The first and second connection electrodes 170 and 180 are formed in each unit pixel. As illustrated in FIGS. 3 and 4, the first connection electrode 170 is formed rightward and apart from the left data line 122, and the second connection electrode 180 is formed leftward and apart from the right data line 124. The first and second connection electrodes 170 and 180 are thus formed at opposite end portions of the unit pixels along the first direction thereof. The first and second connection electrodes 170 and 180 may be bilaterally symmetrical with respect to a virtual line passing through the center of each unit pixel and extending in the second direction.

[0037] A thin film transistor TFT is electrically connected to each of the first and second connection electrodes 170 and 180. In particular, a plurality of thin film transistors TFT is formed on the substrate. Each of the thin film transistors TFT corresponds to an associated one of the pixel electrodes 130, which are arranged in a matrix shape. Each of the thin film transistors TFT disposed in an odd-numbered row is electrically connected to the left data line 122 and the first connection electrode 170, and each of the thin film transistors TFT disposed in an even numbered row is electrically connected to the right data line 124 and the second connection electrode 180, as illustrated in FIG. 3. Optionally, the first and second connection electrodes 170 and 180 that are situated such that they are not electrically connected to a thin film transistor TFT can be omitted.

[0038] As illustrated in FIG. 3, each storage line 160 includes a main storage line 162, a first sub storage line 164 and a second sub storage line 166. The main storage line 162 extends in the second direction, and may pass through the center of each unit pixel in the column thereof.

[0039] The first sub storage line 164 is connected to the main storage line 162 and extends in the first direction. The first sub storage line 164 is arranged to overlap a first edge portion of an adjacent pixel electrode 130 by a first length L1. For example, the first sub storage line 164 may overlap an upper edge portion of a lower pixel electrode 130 by the first length L1.

[0040] In FIG. 3, the first sub storage line 164 extends in the first direction by the first length L1. Thus, the length of the overlap of the first sub storage line 164 and the pixel electrode 130 is substantially the same as the length of the first sub storage line 164. Alternatively, the length of the first sub storage line 164 may be greater than the length of the overlap of the first sub storage line 164 and the pixel electrode 130. In the particular exemplary embodiment of FIG. 3, the first sub storage line 164 extends bilaterally from the main storage line 162, i.e., away from opposite sides thereof, and has a length equal to the first length L1.

[0041] The second sub storage line 166 is connected to the main storage line 162 and also extends in the first direction. The second sub storage line 166 overlaps a second edge portion opposite to the first edge portion of the pixel electrode 130 by the first length L1. For example, the second sub storage line 166 is formed in each unit pixel to be opposite to the first sub storage line 164, and to overlap the pixel electrode 130 by substantially the same length as the overlap between the first sub storage line 164 and the pixel electrode 130.

[0042] In the exemplary embodiment of FIG. 3, the second sub storage line 166 extends in the first direction by a second length L2, which is longer than the first length L1. For example, the second sub storage line 166 has a length corresponding to the second edge portion of the pixel electrode 130. Thus, when a second sub storage line 166 formed between the pixel electrode 130 and the gate line 110 located below the pixel electrode 130 receives a reference voltage, it serves to prevent the gate signal on the gate line 110 from adversely affecting the driving voltage that is charged in the pixel electrode 130. As illustrated in FIG. 3, the second sub storage line 166 may extend bilaterally away from the main storage line 162, i.e., away from opposite sides thereof, and have a total length equal to the second length L2.

[0043] As further illustrated in FIG. 3, the second sub storage line 166 may include an overlapping storage electrode 166a that overlaps the second edge portion of the associated pixel electrode 130 by the first length L1, and a non-overlapping storage electrode 166b that is connected to the overlapping storage electrode 166a and that does not overlap the second edge portion of the associated pixel electrode 130. For example, as illustrated in FIG. 3, the second sub storage line 166 may have a shape such that the overlapping storage electrode 166a is curved away from the non-overlapping storage electrode 166b and toward the pixel electrode 130.

[0044] As illustrated in FIG. 5, the counter substrate

200 facing the array substrate 100 includes a second transparent substrate 210, a light-blocking layer 220, a plurality of color filters 230 and a common electrode 240. The second transparent substrate 210, for example, may be comprised of an optically transparent material and have a plate shape that is substantially the same as that of the first transparent substrate 140.

[0045] The light-blocking layer 220 is formed on the second transparent substrate 210 so as to face the array substrate 100. The light-blocking layer 220 may be formed on the second transparent substrate 210, for example, so as to cover the gate line 110, the data line 120, the thin film transistor TFT, the first connection electrode 170 and the second connection electrode 180.

[0046] The color filters 230 are formed on the second transparent substrate 210 so as to correspond to respective ones of the pixel electrodes 130. The color filters 230 may be formed so as to cover the light-blocking layer 220.

[0047] The common electrode 240 may be formed over substantially the entire surface of the color filters 230. The common electrode 240 may include a transparent conductive material that is substantially the same as the pixel electrode 130. Optionally, a planarizing layer (not illustrated) may be formed between the color filter 230 and the common electrode 240.

[0048] In the above exemplary embodiment, the length of the overlap between the first sub storage line 164 and the first edge portion of the pixel electrode 130 is substantially the same as the length of the overlap between the second sub storage line 166 and the second edge portion of the pixel electrode 130. Thus, although the pixel electrode 130 may be formed such that it is misaligned upwardly or downwardly with respect to the gate line 110, the area of the overlap between the storage line 160 and the pixel electrode 130 remains substantially constant, i.e., does not change. Therefore, the functional characteristics of the storage capacitor that is defined between the storage line 160 and the pixel electrode 130 also remain constant, even though the pixel electrode 130 may be slightly misaligned relative to the storage line 160.

Embodiment 2 (Display Panel)

[0049] FIG. 6 is an enlarged partial plan view of a portion of a second exemplary embodiment of a display panel array substrate 100 in accordance with the present invention. The second embodiment is substantially similar to the first exemplary embodiment described above, except for certain parts of the array substrate 100. Accordingly, the parts that are the same or substantially similar are represented by the same reference numerals and referred to by the same names, and further detailed description of these is omitted below for brevity.

[0050] Referring to FIGS. 2 and 6, the second exemplary array substrate 100 includes a gate line 110, a data line 120, a pixel electrode 130, a first connection electrode 170, a second connection electrode 180, a thin film transistor TFT and a storage line 160.

[0051] A plurality of gate lines 110 is formed on the substrate to extend in a first direction. A plurality of data lines 120 is formed to extend in a second direction substantially perpendicular to the first direction. The gate lines 110 and the data lines 120 cross each other to define a plurality of unit pixels, and each of a plurality of pixel electrodes 130 is formed in a respective one of the unit pixels. Each unit pixel may have, for example, a substantially rectangular shape, with long sides that extend in the first direction, as illustrated in Fig. 6.

[0052] As illustrated in FIG. 6, a domain-division portion 132 is formed in each pixel electrode 130 so as to divide each unit pixel into a plurality of domains. In FIG. 6, the domain-division portion 132 corresponds to an opening that is formed by partially removing the pixel electrode 130. Alternatively, the domain-division portion 132 may correspond to a protrusion that is formed on the pixel electrode 130.

[0053] A left data line 122 is formed at a left side of the pixel electrode 130, and a right data line 124 is formed at a right side of the pixel electrode 130. The left and right data lines 122 and 124 are alternately curved to the left and right sides in the second direction, and have, for example, a curvilinear, U-shaped form, as illustrated in Fig. 6.

[0054] The first and second connection electrodes 170 and 180 are formed in each unit pixel. The first connection electrode 170 is formed rightward and apart from the left data line 122, and is electrically connected to the associated pixel electrode 130 through a first contact hole 192. The second connection electrode 180 is formed leftward and apart from the right data line 124, and is electrically connected to the associated pixel electrode 130 through a second contact hole 194. The first and second connection electrodes 170 and 180 may be bilaterally symmetrical with respect to a virtual line passing through the center of the pixel electrode 130 and extending in the second direction.

[0055] More specifically, the first connection electrode 170 includes a first contact portion 172 that is electrically connected to the associated pixel electrode 130 through the first contact hole 192, and a first extension portion 174 that extends from the first contact portion 172 in the second direction. The second connection electrode 180 includes a second contact portion 182 that is electrically connected to the associated pixel electrode 130 through the second contact hole 194, and a second extension portion 184 that extends from the second contact portion 182 in the second direction.

[0056] The thin film transistor TFT includes a gate electrode G, an active layer A, a source electrode S, a drain electrode D and an ohmic contact layer (not illustrated). The gate electrode G corresponds to a part of the gate line 110, and the active layer A is formed over the gate electrode G. The source electrode S corresponds to a U-shaped curved portion of either the left data line 122 or the right data line 124 and partially overlaps the active

layer A. The drain electrode D is formed between the source electrode S of the U-shape, and partially overlaps the active layer A. The ohmic contact layer (not illustrated) is respectively formed between the active layer A and the source electrode S, and between the active layer A and the drain electrode D.

[0057] A plurality of thin film transistors TFT is formed that correspond respectively to the pixel electrodes 130. Each drain electrode D of the thin film transistors TFT that are disposed in odd numbered rows and each drain electrode D of the thin film transistors TFT that are disposed in even numbered rows are formed on one virtual line that is substantially parallel with the second direction, and may be formed on the longitudinal line of the data line 120.

[0058] Each drain electrode D of the thin film transistors TFT is electrically connected to one of the first and second connection electrodes 170 and 180 that are formed in the same unit pixel. In particular, each of the thin film transistors TFT disposed in the odd numbered rows is electrically connected to the first connection electrode 170 disposed in the odd numbered rows, and each of the thin film transistors TFT disposed in the even numbered rows is electrically connected to the second connection electrode 180 disposed in the even numbered rows.

[0059] FIG. 7 is a cross-sectional view of the second exemplary array substrate as seen along the lines of the section II-II' taken in FIG. 6, and FIG. 8 is a cross-sectional view of the second exemplary array substrate as seen along the lines of the section III-III' taken in FIG. 6.

[0060] Referring to FIGS. 6, 7 and 8, the array substrate includes a storage line 160 to which reference voltage is externally applied, and the storage line 160 includes a main storage line 162, a first sub storage line 164 and a second sub storage line 166.

[0061] The main storage line 162 extends in the second direction, and may pass through the center of each of the unit pixels of a pixel column so as to overlap the pixel electrodes 130 thereof.

[0062] The first sub storage line 164 is connected to the main storage line 162 and extends in the first direction by a first length L1. The first sub storage line 164 overlaps a first edge portion of the pixel electrode 130 by the first length L1. Thus, the length of the overlap between the first sub storage line 164 and the pixel electrode 130 is substantially the same as the length of the first sub storage line 164. Alternatively, the length of the first sub storage line 164 may be greater than the length of the overlap of the first sub storage line 164 and the pixel electrode 130. As illustrated in FIG. 6, the first sub storage line 164 may extend out from opposite sides of the main storage line 162, and have an overall length equal to the first length L1.

[0063] The second sub storage line 166 is connected to the main storage line 162 and extends in the first direction by a second length L2 that is longer than the first length L1. For example, the second sub storage line 166 may have a length corresponding to a second edge portion of the pixel electrode 130. The second sub storage line 166 may extend away from opposite sides of the main storage line 162 and have a length equal to the second length L2, as illustrated in FIG. 6. The second sub storage line 166 overlaps the second edge portion of the pixel electrode 130 opposite to the first edge portion thereof by the first length L1. For example, the second sub storage line 166 may overlap the pixel electrode 130 by substantially the same length as the length of the overlap between the first sub storage line 164 and the pixel electrode 130.

[0064] More particularly, the second sub storage line 166 includes an overlapping storage electrode 166a that overlaps the second edge portion of the pixel electrode 130 and a non-overlapping storage electrode 166b that is connected to the overlapping storage electrode 166a and is arranged such that it does not overlap the second edge portion of the pixel electrode 130.

[0065] For example, the second sub storage line 166 may be shaped such that the overlapping storage electrode 166a curves away from the non-overlapping storage electrode 166b and toward the pixel electrode 130. The overlapping storage electrode 166a thus overlaps the second edge portion of the pixel electrode 130 by the first length L1. The non-overlapping storage electrode 166b is disposed between the pixel electrode 130 and the associated gate line 110 when viewed in a plan view.

[0066] The second sub storage line 166 may be bilaterally symmetrical with respect to a virtual line passing through the center of each unit pixel of a column thereof and extending in the second direction. The storage line 160 may also be bilaterally symmetrical with respect to that line.

[0067] In accordance with the second exemplary embodiment above, the length of the overlap between the first sub storage line 164 and the first edge portion of the pixel electrode 130 is substantially the same as the length of the overlap between the second sub storage line 166 and the second edge portion of the pixel electrode 130. Therefore, although the pixel electrode 130 may be misaligned either upwardly or downwardly with respect to the gate line 110, the area of overlap between the storage line 160 and the pixel electrode 130 will remain constant, i. e., unchanging, regardless of any such misalignment of the pixel electrode.

Embodiment 3 (Display Panel)

[0068] FIG. 9 is an enlarged partial plan view of a portion of a third exemplary embodiment of a display panel array substrate in accordance with the present invention. The third exemplary array substrate is substantially similar to the second exemplary embodiment above, except for the storage lines thereof. Accordingly, in the description below, parts that are the same or substantially similar to those of the second embodiment are represented by the same reference numerals and referred to by the same

names and further detailed description of these is omitted.

[0069] Referring to FIG. 9, the third exemplary array substrate includes a storage line 160 to which a reference voltage is externally applied, and the storage line 160 includes a main storage line 162, a first sub storage line 164 and a second sub storage line 166. The main storage line 162 extends in the second direction, and may pass through the center of each unit pixel in a pixel column so as to overlap the pixel electrodes 130 thereof.

[0070] The first sub storage line 164 is connected to the main storage line 162 and extends in the first direction by a first length L1. The first sub storage line 164 overlaps a first edge portion of the pixel electrode 130 by the first length L1. Thus, as illustrated in Fig. 9, the first sub storage line 164 may extend away from opposite sides of the main storage line 162 in the first direction and have a length equal to the first length L1.

[0071] The second sub storage line 166 is connected to the main storage line 162 and extends in the first direction by a second length L2 that is longer than the first length L1. For example, the second sub storage line 166 may have a length corresponding to a second edge portion of the pixel electrode 130 opposite to the first edge portion thereof. Thus, as illustrated in FIG. 9, the second sub storage line 166 may extend out from opposite sides of the main storage line 162 in the first direction and have a length that is equal to the second length L2.

[0072] As further illustrated in FIG. 9, the second sub storage line 166 overlaps the second edge portion of the pixel electrode 130 by the first length L1. For example, the second sub storage line 166 may overlap the pixel electrode 130 by substantially the same length as the length of overlap between the first sub storage line 164 and the first edge portion of the pixel electrode 130.

[0073] More particularly, the second sub storage line 166 includes an overlapping storage electrode 166a that overlaps the second edge portion of the pixel electrode 130 and a non-overlapping storage electrode 166b that is connected to the overlapping storage electrode 166a, and that does not overlap the second edge portion of the pixel electrode 130. As illustrated in FIG. 9, the non-overlapping storage electrode 166b is disposed between the pixel electrode 130 and the gate line 110 when viewed in a plan view.

[0074] The overlapping storage electrode 166a has a width that is wider than that of the non-overlapping storage electrode 166b. In one particular exemplary embodiment, the width of the non-overlapping storage electrode 166b is in a range of from about 3 μm to about 4 μm, whereas, the width of the overlapping storage electrode 166a is in a range of from about 5 μm to about 7 μm (where 1 μm = 1 X 10^{-6} meters). Since the width of the overlapping storage electrode 166a is greater than that of the non-overlapping storage electrode 166b, the overlapping storage electrode 166a overlaps the second edge portion of the pixel electrode 130 by the first length L1.

[0075] In an alternative embodiment (not illustrated), the storage line 160 may be shaped such that the overlapping storage electrode 166a curves away from the non-overlapping storage electrode 166b and toward the pixel electrode 130.

[0076] In the particular exemplary embodiment illustrated in FIG. 9, the second sub storage line 166 is bilaterally symmetrical with respect to a virtual line passing through the center of each unit pixel of the column thereof and extending in the second direction. The storage line 160 may also be bilaterally symmetrical with respect to that same line.

[0077] In accordance with the third exemplary embodiment described above, the overlapping storage electrode 166a has a width greater than that of the non-overlapping storage electrode 166b, and overlaps the second edge portion of the pixel electrode 130 by the first length L1. Thus, although the pixel electrode 130 may be slightly misaligned either upwardly or downwardly with respect to the gate line 110 during the fabrication thereof, the area of overlap between the storage line 160 and the pixel electrode 130 remains substantially constant, regardless of any such misalignment of the pixel electrode 130.

Embodiment 4 (Display Panel)

[0078] FIG. 10 is an enlarged partial plan view of a portion of a fourth exemplary embodiment of a display panel array substrate in accordance with the present invention. The fourth exemplary array substrate is substantially similar to the second exemplary embodiment above, except for the storage lines and pixel electrodes thereof. Accordingly, in the description below, the parts that are the same or substantially similar to those of the second embodiment above are represented by the same reference numerals and are referred to by the same names and further detailed description thereof is omitted.

[0079] Referring to FIG. 10, the fourth exemplary embodiment includes a storage line 160 to which a reference voltage is externally applied, and the storage line 160 includes a main storage line 162, a first sub storage line 164 and a second sub storage line 166. The main storage line 162 extends in the second direction, and may pass through the center of each unit pixel of a pixel column to overlap the pixel electrodes 130 thereof.

[0080] The first sub storage line 164 is connected to the main storage line 162 and extends for a first length L1 in the first direction. The first sub storage line 164 is arranged to overlap a first edge portion of the pixel electrode 130 by the first length L1. As illustrated in FIG. 10, the first sub storage line 164 may extend outwardly from opposite sides of the main storage line 162 and have an overall length that is equal to the first length L1.

[0081] The second sub storage line 166 is connected to the main storage line 162 and extends in the first direction for a second length L2 that is longer than the first length L1. For example, the second sub storage line 166

has a length corresponding to the second edge portion of the pixel electrode 130. As illustrated in FIG. 10, the second sub storage line 166 may extend from opposite sides of the main storage line 162 and have an overall length that is equal to the second length L2.

[0082] As illustrated in FIG. 10, the second sub storage line 166 is arranged to overlap a second edge portion opposite to the first edge portion of the pixel electrode 130 by the first length L1. For example, the second sub storage line 166 may overlap the pixel electrode 130 by substantially the same length as the length of overlap between the first sub storage line 164 and the pixel electrode 130.

[0083] The second sub storage line 166 may be bilaterally symmetrical with respect to a virtual line passing through a center of each unit pixel and extending in the second direction. The storage line 160 may also be bilaterally symmetrical with respect to that same line.

[0084] Each of the pixel electrodes 130 is disposed in a respective one of the unit pixels, and includes a main pixel electrode 130a and an overlapping electrode 130b.

[0085] The main pixel electrode 130a corresponds to a larger portion of the pixel electrode 130 and is arranged such that it does not overlap the second sub storage line 166. The main pixel electrode 130a has, for example, a substantially rectangular shape, with a long side aligned in the first direction when viewed in plan view.

[0086] The overlapping electrode 130b extends down from the main pixel electrode 130a and toward the second sub storage line 166 so as to overlap the second sub storage line 166 by the first length L1.

[0087] A domain-division portion 132 is formed in each pixel electrode 130 so as to divide each unit pixel into a plurality of domains. In FIG. 10, the domain-division portion 132 corresponds to an opening that is formed by partially removing the pixel electrode 130, but in one possible alternative embodiment, the domain-division portion 132 may correspond to a protrusion formed on the pixel electrode 130.

[0088] In accordance with the fourth exemplary embodiment described above, the pixel electrode 130 includes an overlapping electrode 130b that overlaps the second sub storage line 166 by the first length L1. Thus, although the pixel electrode 130 may be misaligned either upwardly or downwardly with respect to the gate line 110 during its fabrication, the area of overlap between the storage line 160 and the pixel electrode 130 remains substantially constant, regardless of any such misalignment of the pixel electrode 130.

Embodiment 5 (Display Panel)

[0089] FIG. 11 is an enlarged partial plan view of a portion of a fifth exemplary embodiment of a display panel array substrate in accordance with the present invention. The fifth exemplary array substrate is substantially similar to the second exemplary embodiment above, except for the storage lines thereof. Accordingly, in the following description, parts that are the same or substantially similar to those of the second embodiment are represented by the same reference numerals and are referred to by the same names and further detailed description thereof is omitted.

[0090] Referring to FIG. 11, the fifth exemplary array substrate includes a storage line 160 to which a reference voltage is externally applied, and the storage line 160 includes a main storage line 162, a first sub storage line 164 and a second sub storage line 166. The main storage line 162 extends in the second direction, and may pass through the center of each unit pixel in a column thereof so as to overlap the pixel electrodes 130 thereof.

[0091] The first sub storage line 164 is connected to the main storage line 162 and extends in the first direction by a first length L1. The first sub storage line 164 is arranged to overlap a first edge portion of the pixel electrode 130 by the first length L1. As illustrated in FIG. 11, the first sub storage line 164 may extend out from opposite sides of the main storage line 162 and have an overall length equal to the first length L1.

[0092] The second sub storage line 166 is connected to the main storage line 162 and extends in the first direction by a second length L2 that is longer than the first length L1. For example, the second sub storage line 166 may have a length corresponding to a second edge portion of the pixel electrode 130 opposite to the first edge portion thereof. As illustrated in FIG. 11, the second sub storage line 166 may extend out from opposite sides of the main storage line 162 and have an overall length equal to the second length L2.

[0093] The second sub storage line 166 includes an overlapping storage electrode 166a that overlaps the second edge portion of the pixel electrode 130 by the first length L1 and a non-overlapping storage electrode 166b that is connected to the overlapping storage electrode 166a and that does not overlap the second edge portion of the pixel electrode 130. As illustrated in FIG. 11, the non-overlapping storage electrode 166b is disposed between the pixel electrode 130 and the associated gate line 110 when viewed in plan view.

[0094] As illustrated in FIG. 11, the overlapping storage electrode 166a has a shape that curves upward from the non-overlapping storage electrode 166b and toward the pixel electrode 130. The second sub storage line 166 may be bilaterally symmetrical with respect to a virtual line passing through a center of each unit pixel of a column thereof and extending in the second direction. The storage line 160 may also be bilaterally symmetrical with respect that same line.

[0095] Each pixel electrode 130 is disposed in a respective one of the unit pixels, and includes a main pixel electrode 130a and an overlapping electrode 130b.

[0096] The main pixel electrode 130a corresponds to a larger portion of the pixel electrode 130, and does not overlap the second sub storage line 166. The main pixel electrode 130a has, for example, a substantially rectangular shape with long sides that extend in the first direc-

tion when viewed in plan view.

[0097] The overlapping electrode 130b extends down from the main pixel electrode 130a and toward the second sub storage line 166 so as to overlap the second sub storage line 166 by the first length L1. For example, the overlapping electrode 130b may overlap the overlapping storage electrode 166a of the second sub storage line 166 by the first length L1.

[0098] A domain-division portion 132 is formed in each pixel electrode 130 so as to divide each unit pixel into a plurality of domains. In FIG. 11, the domain-division portion 132 corresponds to an opening that is formed by partially removing the pixel electrode 130, but in an alternative embodiment, the domain-division portion 132 may correspond to a protrusion formed on the pixel electrode 130.

[0099] In accordance with the fifth exemplary embodiment described above, the overlapping storage electrode 166a is curved toward the pixel electrode 130, and the pixel electrode 130 includes the overlapping electrode 130a that protrudes down toward the second sub storage line 166. Thus, although the pixel electrode 130 may be misaligned upwardly or downwardly with respect to the gate line 110 during fabrication thereof, the area of overlap between the storage line 160 and the pixel electrode 130, and hence, the storage capacitance defined thereby, remains constant, regardless of such misalignment of the pixel electrode 130.

[0100] According to the several exemplary embodiments disclosed herein, the length of overlap between the first sub storage line and the first edge portion of the pixel electrode is substantially the same as the length of overlap between the second sub storage line and the second edge portion of the pixel electrode. Thus, although the pixel electrode may be slightly misaligned either upwardly or downwardly with respect to the gate line during fabrication thereof, the storage capacitor defined by the area of overlap between the storage line and the pixel electrode remains substantially constant, regardless of such pixel electrode misalignment. Since the storage capacitor is substantially unaffected by pixel electrode misalignment, the kickback voltage provided by the storage capacitor remains substantially invariant, thereby improving the image quality of the display panel.

Claims

1. An array substrate (100), comprising:

a gate line (110) formed in a first direction;
a data line (120) formed in a second direction that crosses the first direction;
a thin film transistor (TFT) electrically connected to the gate line (110) and the data line (120);
a pixel electrode (130) formed in a unit pixel having a first side extending in
the first direction longer than a second side extending in the second direction and electrically connected to the thin film transistor (TFT); and,
a storage line (160), comprising:

a main storage line (162);
a first sub storage line (164) that is connected to the main storage line (162), the first sub storage line (164) extending in the first direction and overlapping a first edge portion of the pixel electrode (130) by a first length (L1); and,
a second sub storage line (166) that is connected to the main storage line (162);
wherein the second sub storage line (166) comprises:

an overlapping storage electrode (166a) that overlaps a second edge portion of the pixel electrode (130) opposite to the first edge portion thereof by the first length (L1); and,
a non-overlapping storage electrode (166b) that is connected to the overlapping storage electrode (166a) that does not overlap the second edge portion of the pixel electrode (130);
wherein the gate line (110) is located below the pixel electrode (130) in a plan view;
characterized in that
the second sub storage line (166) is formed between the pixel electrode (130) and the gate line (110) in a plan view;
the main storage line (162) extends in the second direction;
the first sub storage line (164) extends in the first direction by the first length (L1); and
the second sub storage line (166) extends in the first direction by a second length (L2) that is longer than the first length (L1).

2. The array substrate (100) of claim 1, wherein the second sub storage line (166) has a length corresponding to the length of the second edge portion of the pixel electrode (130).

3. The array substrate (100) of claim 1, wherein the overlapping storage electrode (166a) is curved away from the non-overlapping storage electrode (166b) and toward the pixel electrode (130).

4. The array substrate (100) of claim 1, wherein a width of the overlapping storage electrode (166a) is wider than a width of the non-overlapping storage electrode (166b).

5. The array substrate (100) of claim 4, wherein the width of the non-overlapping storage electrode (166b) is in a range of from about 3 μm to about 4 μm.

6. The array substrate (100) of claim 4, wherein the

width of the overlapping storage electrode (166a) is in a range of from about 5μm to about 7 μm.

7. The array substrate (100) of claim 1, wherein the pixel electrode (130) comprises:

a main pixel electrode (130a) that does not overlap the second sub storage line (166); and,
an overlapping electrode (130b) that extends from the main pixel electrode (130a) and toward the second sub storage line (166) so as to overlap the second sub storage line (166) by the first length (L1).

8. The array substrate (100) of claim 7, wherein the second sub storage line (166) comprises:

an overlapping storage electrode (166a) that overlaps the overlapping electrode (130b) by the first length (L1); and,
a non-overlapping storage electrode (166b) that is connected to the overlapping storage electrode (166a) and that does not overlap the main pixel electrode (130a).

9. The array substrate (100) of claim 8, wherein the overlapping storage electrode (166a) is curved away from the non-overlapping storage electrode (166b) and toward the pixel electrode (130).

10. The array substrate (100) of claim 9, wherein a width of the overlapping storage electrode (166a) is wider than a width of the non-overlapping storage electrode (166b).

11. The array substrate (100) of claim 1, wherein the main storage line (162) passes through the center of the unit pixel.

12. The array substrate (100) of claim 11, wherein the first and second i sub storage lines (164; 166) extend out from opposite sides of the main storage line (162).

13. The array substrate (100) of claim 12, wherein the storage line (160) is bilaterally symmetrical with respect to a virtual line passing through the center of the unit pixel and extending in the second direction.

14. The array substrate (100) of claim 1, wherein the storage line (160) and the data line (120) are formed in the same layer.

15. The array substrate (100) of claim 1, wherein the second direction is substantially perpendicular to the first direction, and wherein the unit pixel has a substantially rectangular shape.

16. The array substrate (100) of claim 15, further comprising first and second connection electrodes (170; 180) formed in a same layer as the data line (120) and at opposite end portions of the unit pixel so as to overlap the pixel electrode (130).

17. The array substrate (100) of claim 16, further comprising:

a protective layer (190) respectively disposed between the first connection electrode (170) and the pixel electrode (130), and between the second connection electrode (180) and the pixel electrode (130), wherein a first contact hole (192) is formed through the protective layer (190) to electrically connect the first connection electrode (170) to the pixel electrode (130), and a second contact hole (194) is formed through the protective layer (190) to electrically connect the second connection electrode (180) to the pixel electrode (130)

18. The array substrate (100) of claim 17, wherein a drain electrode (D) of the thin film transistor (TFT) is electrically connected to one of the first and the second connection electrodes (170; 180).

19. The array substrate (100) of claim 18, further comprising:

a plurality of pixel electrodes (130) arranged in a matrix shape, a plurality of first and second connection electrodes (170; 180) corresponding to the pixel electrodes (130), and a plurality of thin film transistors (TFT) corresponding to the pixel electrodes (130),wherein drain electrodes (D) of the thin film transistors (TFT) disposed in odd numbered rows of the matrix are electrically connected to the first connection electrodes (170) disposed in the odd numbered rows thereof, and drain electrodes (D) of the thin film transistors (TFT) disposed in even numbered rows of the matrix are electrically connected to the second connection electrodes (180) disposed in the even numbered rows thereof.

20. The array substrate (100) of claim 19, wherein the drain electrodes (D) of the thin film transistors (TFT) disposed in odd numbered rows of the matrix and the drain electrodes (D) of the thin film transistors (TFT) disposed in the even numbered rows of the matrix are formed on a longitudinal line of the data line (120).

21. A display panel (400), comprising:

an array substrate (100) according to claim 1;
a counter substrate (200) facing the array sub-

strate (100); and,
a liquid crystal layer (300) disposed between the array substrate (100) and the counter substrate (200).

22. The display panel (400) of claim 21, wherein the counter substrate (200) comprises:

a light-blocking layer (220) covering the first and second sub storage line (164; 166);
a color filter (230) covering the light-blocking layer (220); and,
a common electrode (240) formed on the color filter (230).

Patentansprüche

1. Array-Substrat (100), umfassend
eine in einer ersten Richtung gebildete Gate-Leitung (110),
eine Datenleitung (120), die in einer zweiten Richtung gebildet ist, welche die erste Richtung kreuzt,
einen Dünnfilmtransistor (TFT), der mit der Gate-Leitung (110) und der Datenleitung (120) elektrisch verbunden ist,
eine Pixelelektrode (130), die in einem Einheitspixel gebildet ist, mit einer in einer ersten Richtung verlaufenden ersten Seite, die länger als eine in der zweiten Richtung verlaufende zweite Seite ist, und die mit dem Dünnfilmtransistor (TFT) elektrisch verbunden ist, und
eine Speicherleitung (160), umfassend:

eine Hauptspeicherleitung (162),
eine erste Subspeicherleitung (164), die mit der Hauptspeicherleitung (162) verbunden ist, wobei die erste Subspeicherleitung (164) in der ersten Richtung verläuft und einen ersten Randabschnitt der Pixelelektrode (130) um eine erste Länge (L1) überlappt, und
eine zweite Subspeicherleitung (166), die mit der Hauptspeicherleitung (162) verbunden ist,
wobei die zweite Subspeicherleitung (166) folgendes umfasst:

eine überlappende Speicherelektrode (166a), die einen zweiten Randabschnitt der Pixelelektrode (130) gegenüber deren erstem Randabschnitt um die erste Länge (L1) überlappt, und
eine nicht-überlappende Speicherelektrode (166b), die mit der überlappenden Speicherelektrode (166a) verbunden ist und den zweiten Randabschnitt der Pixelelektrode (130) nicht überlappt;
wobei die Gate-Leitung (110) in Draufsicht unterhalb der Pixelelektrode (130) angeordnet ist,
dadurch gekennzeichnet, dass
die zweite Subspeicherleitung (166) in Draufsicht zwischen der Pixelelektrode (130) und der Gate-Leitung (110) gebildet ist,
die Hauptspeicherleitung (162) in der zweiten Richtung verläuft,
die erste Subspeicherleitung (164) sich in der ersten Richtung über die erste Länge (L1) erstreckt, und
die zweite Subspeicherleitung (166) sich in der ersten Richtung über eine zweite Länge (L2) erstreckt, die länger als die erste Länge (L1) ist.

2. Array-Substrat (100) nach Anspruch 1, wobei die zweite Subspeicherleitung (166) eine Länge aufweist, die der Länge des zweiten Randabschnitts der Pixelelektrode (130) entspricht.

3. Array-Substrat (100) nach Anspruch 1, wobei die überlappende Speicherelektrode (166a) von der nicht-überlappenden Speicherelektrode (166b) weg und zur Pixelelektrode (130) hin gekrümmt ist.

4. Array-Substrat (100) nach Anspruch 1, wobei eine Breite der überlappenden Speicherelektrode (166a) breiter als eine Breite der nicht-überlappenden Speicherelektrode (166b) ist.

5. Array-Substrat (100) nach Anspruch 4, wobei die Breite der nicht-überlappenden Speicherelektrode (166b) im Bereich von etwa 3 μm bis etwa 4 μm liegt.

6. Array-Substrat (100) nach Anspruch 4, wobei die Breite der überlappenden Speicherelektrode (166a) im Bereich von etwa 5 μm bis etwa 7 μm liegt.

7. Array-Substrat (100) nach Anspruch 1, wobei die Pixelelektrode (130) umfasst:

eine Hauptpixelelektrode (130a), welche die zweite Subspeicherleitung (166) nicht überlappt, und
eine überlappende Elektrode (130b), die von der Hauptelektrode (130a) weg und zur zweiten Subspeicherleitung (166) hin verläuft, um die zweite Subspeicherleitung (166) um die erste Länge (L1) zu überlappen.

8. Array-Substrat (100) nach Anspruch 7, wobei die zweite Subspeicherleitung (166) umfasst:

eine überlappende Speicherelektrode (166a), welche die überlappende Elektrode (130b) um die erste Länge (L1) überlappt, und
eine nicht-überlappende Speicherelektrode

(166b), die mit der überlappenden Speicherelektrode (166a) verbunden ist und die Hauptpixelelektrode (130a) nicht überlappt.

9. Array-Substrat (100) nach Anspruch 8, wobei die überlappende Speicherelektrode (166a) von der nicht-überlappenden Speicherelektrode (166b) weg und zur Pixelelektrode (130) hin gekrümmt ist.

10. Array-Substrat (100) nach Anspruch 9, wobei eine Breite der überlappenden Speicherelektrode (166a) breiter als eine Breite der nicht-überlappenden Speicherelektrode (166b) ist.

11. Array-Substrat (100) nach Anspruch 1, wobei die Hauptspeicherleitung (162) durch die Mitte des Einheitspixels läuft.

12. Array-Substrat (100) nach Anspruch 11, wobei die erste und die zweite Subspeicherleitung (164; 166) von gegenüberliegenden Seiten der Hauptspeicherleitung (162) herauslaufen.

13. Array-Substrat (100) nach Anspruch 12, wobei die Speicherleitung (160) in Bezug auf eine virtuelle Linie, die sich durch die Mitte des Einheitspixels und in der zweiten Richtung erstreckt, bilateral symmetrisch ist.

14. Array-Substrat (100) nach Anspruch 1, wobei die Speicherleitung (160) und die Datenleitung (120) in derselben Schicht gebildet sind.

15. Array-Substrat (100) nach Anspruch 1, wobei die zweite Richtung im Wesentlichen senkrecht zur ersten Richtung ist und wobei das Einheitspixel eine im Wesentlichen rechteckige Form aufweist.

16. Array-Substrat (100) nach Anspruch 15, ferner umfassend erste und zweite Anschlusselektroden (170; 180), die in derselben Schicht wie die Datenleitung (120) und an gegenüberliegenden Endabschnitten des Einheitspixels ausgebildet sind, so dass sie die Pixelelektrode (130) überlappen.

17. Array-Substrat (100) nach Anspruch 16, ferner umfassend:

Eine Schutzschicht (190), die zwischen der ersten Anschlusselektrode (170) und der Pixelelektrode (130) bzw. zwischen der zweiten Anschlusselektrode (180) und der Pixelelektrode (130) angeordnet ist,
wobei ein erstes Kontaktloch (192) durch die Schutzschicht (190) hindurch ausgebildet ist, um die erste Anschlusselektrode (170) mit der Pixelelektrode (130) elektrisch zu verbinden, und ein zweites Kontaktloch (194) durch die Schutzschicht (190) hindurch ausgebildet ist, um die zweite Anschlusselektrode (180) mit der Pixelelektrode (130) elektrisch zu verbinden.

18. Array-Substrat (100) nach Anspruch 17, wobei eine Drain-Elektrode (D) des Dünnfilmtransistors (TFT) mit einer der ersten und zweiten Anschlusselektroden (170; 180) elektrisch verbunden ist.

19. Array-Substrat (100) nach Anspruch 18, ferner umfassend:

Eine Vielzahl von Pixelelektroden (130), die matrixförmig angeordnet sind,
eine Vielzahl erster und zweiter Anschlusselektroden (170; 180),
entsprechend den Pixelelektroden (130), und eine Vielzahl von Dünnfilmtransistoren (TFT), entsprechend den Pixelelektroden (130),
wobei in ungeradzahligen Reihen der Matrix angeordnete Drain-Elektroden (D) der Dünnfilmtransistoren (TFT) mit den in deren ungeradzahligen Reihen angeordneten, ersten Anschlusselektroden (170) elektrisch verbunden sind, und in geradzahligen Reihen der Matrix angeordnete Drain-Elektroden (D) der Dünnfilmtransistoren (TFT) mit in deren geradzahligen Reihen angeordneten, zweiten Anschlusselektroden (180) elektrisch verbunden sind.

20. Array-Substrat (100) nach Anspruch 19, wobei die in ungeradzahligen Reihen der Matrix angeordneten Drain-Elektroden (D) der Dünnfilmtransistoren (TFT) und die in den geradzahligen Reihen der Matrix angeordneten Drain-Elektroden (D) der Dünnfilmtransistoren (TFT) auf einer Längslinie der Datenleitung (120) ausgebildet sind.

21. Anzeigefeld (400), umfassend:

Ein Array-Substrat (100) nach Anspruch 1,
ein Gegensubstrat (200), das dem Array-Substrat (100) zugewandt ist,
und
eine Flüssigkristallschicht (300), die zwischen dem Array-Substrat (100) und dem Gegensubstrat (200) angeordnet ist.

22. Anzeigefeld (400) nach Anspruch 21, wobei das Gegensubstrat (200) umfasst:

eine Lichtblockierschicht (220), welche die erste und zweite Subspeicherleitung (164; 166) bedeckt,
einen Farbfilter (230), der die Lichtblockierschicht (220) bedeckt, und
eine gemeinsame Elektrode (240), die auf dem Farbfilter (230) ausgebildet ist.

Revendications

1. Un substrat de réseau (100), comprenant :

une ligne de porte (110) formée dans une première direction ;
une ligne de données (120) formée dans une deuxième direction qui traverse la première direction ;
un transistor à couche mince (TFT) électriquement connecté à la ligne de porte (110) et la ligne de données (120) ;
une électrode à pixel (130) formée dans un pixel d'unité ayant un premier côté s'étendant dans la première direction plus long qu'un deuxième côté s'étendant dans la deuxième direction et connectée électriquement au transistor à couche mince (TFT) ; et,
une ligne de stockage (160), comprenant :

une ligne de stockage principale (162) ;
une première ligne de sous-stockage (164) qui est connectée à la ligne de stockage principale (162), la première ligne de sous-stockage (164) s'étendant dans la première direction et chevauchant une première partie de bord de l'électrode à pixel (130) par une première longueur (L1) ;
et,
une deuxième ligne de sous-stockage (166) qui est connectée à la ligne de stockage principale (162) ;
où la deuxième ligne de sous-stockage (166) comprend :

une électrode de stockage chevauchante (166a) qui chevauche une deuxième partie de bord de l'électrode à pixel (130) à l'opposé de la première partie de bord par la première longueur (L1) ; et
une électrode de stockage non-chevauchante (166b) qui est connectée à l'électrode de stockage chevauchante (166a) qui ne chevauche pas la deuxième partie de bord de l'électrode à pixel (130) ;
où la ligne de porte (110) se trouve sous l'électrode à pixel (130) dans une vue en plan ;
charactérisé en ce que
la deuxième ligne de sous-stockage (166) est formée entre l'électrode à pixel (130) et la ligne de porte (110) dans une vue en plan ;
la ligne de stockage principale (162) s'étend dans la deuxième direction ;
la première ligne de sous-stockage (164) s'étend dans la première direction par la première longueur (L1) ; et
la deuxième ligne de sous-stockage (166) s'étend dans la première direction par une deuxième longueur (L2) qui est plus longue que la première longueur (L1).

2. Le substrat de réseau (100) de la revendication 1, où la deuxième ligne de sous-stockage (166) possède une longueur correspondant à la longueur de la deuxième partie de bord de l'électrode à pixel (130).

3. Le substrat de réseau (100) de la revendication 1, où l'électrode de stockage chevauchante (166a) est incurvée à distance de l'électrode de stockage non-chevauchante (166b) et vers l'électrode à pixel (130).

4. Le substrat de réseau (100) de la revendication 1, où une largeur de l'électrode de stockage chevauchante (166a) est plus large qu'une largeur de l'électrode de stockage non-chevauchante (166b).

5. Le substrat de réseau (100) de la revendication 4, où la largeur de l'électrode de stockage non-chevauchante (166b) est dans une fourchette d'environ 3 μm à environ 4 μm.

6. Le substrat de réseau (100) de la revendication 4, où la largeur de l'électrode de stockage chevauchante (166a) est dans une fourchette d'environ 5 μm à environ 7 μm.

7. Le substrat de réseau (100) de la revendication 1, où l'électrode à pixel (130) comprend :

une électrode à pixel principale (130a) qui ne chevauche pas la deuxième ligne de sous-stockage (166) et ;
une électrode chevauchante (130b) qui s'étend de l'électrode à pixel principale (130a) et vers la deuxième ligne de sous-sltockage (166) afin de faire chevaucher la deuxième ligne de sous-stockage (166) par la première longueur (L1).

8. Le substrat de réseau (100) de la revendication 7, où la deuxième ligne de sous-stockage (166) comprend :

une électrode de stockage chevauchante (166a) qui chevauche l'électrode chevauchante (130b) de la première longueur (L1) ; et
un électrode de stockage non-chevauchante (166b) qui est connectée à l'électrode de stockage chevauchante (166a) et qui ne chevauche pas l'électrode à pixel principale (130a).

9. Le substrat de réseau (100) de la revendication 8, où l'électrode de stockage chevauchante (166a) est incurvée à distance de l'électrode de stockage non-chevauchante (166b) et vers l'électrode à pixel (130).

10. Le substrat de réseau (100) de la revendication 9, où une largeur de l'électrode de stockage chevauchante (166a) est plus large qu'une largeur de l'électrode de stockage non-chevauchante (166b).

11. Le substrat de réseau (100) de la revendication 1, où la ligne de stockage principale (162) passe au travers du centre du pixel d'unité.

12. Le substrat de réseau (100) de la revendication 11, où les première et deuxième lignes de sous-stockage (164 ; 166) s'étendent de côtés opposés de la ligne de stockage principale (162).

13. Le substrat de réseau (100) de la revendication 12, où la ligne de stockage (160) est bilatéralement symétrique par rapport à une ligne virtuelle passant au travers du centre du pixel d'unité et s'étendant dans la deuxième direction.

14. Le substrat de réseau (100) de la revendication 1, où la ligne de stockage (160) et la ligne de données (120) sont formées dans la même couche.

15. Le substrat de réseau (100) de la revendication 1, où la deuxième direction est substantiellement perpendiculaire à la première direction, et où le pixel d'unité présente une forme substantiellement rectangulaire.

16. Le substrat de réseau (100) de la revendication 15, comprenant de plus les première et deuxième électrodes de connexion (170 ; 180) formées dans une même couche que la ligne de données (120) et à des parties de bord opposées du pixel d'unité afin de chevaucher l'électrode à pixel (130).

17. Le substrat de réseau (100) de la revendication 16, comprenant de plus :

une couche de protection (190) disposée respectivement entre la première électrode de connexion (170) et l'électrode à pixel (130), et entre la deuxième électrode de connexion (180) et l'électrode à pixel (130), où un premier trou de contact (192) est formé au travers de la couche de protection (190) pour connecter électriquement la première électrode de connexion (170) à l'électrode à pixel (130), et un deuxième trou de contact (194) est formé au travers de la couche de protection (190) pour connecter électriquement la deuxième électrode de connexion (180) à l'électrode à pixel (130).

18. Le substrat de réseau (100) de la revendication 17, où une électrode déversoir (D) du transistor à couche mince (TFT) est connectée électriquement à une des première et deuxième électrodes de connexion (170 ; 180).

19. Le substrat de réseau (100) de la revendication 18, comprenant de plus :

une pluralité d'électrodes de pixel (130) disposées en forme de matrice,
une pluralité des première et deuxième électrodes de connexion (170 ; 180) correspondant aux électrodes à pixel (130), et une pluralité de transistors à couche mince (TFT) correspondant aux électrodes à pixel (130), où des électrodes déversoirs (D) des transistors à couche mince (TFT) disposées en rangées de la matrice numérotées de façon impaire sont connectées électriquement aux premières électrodes de connexion (170) disposées en rangées numérotées de façon impaire, et des électrodes déversoirs (D) des transistors à couche mince (TFT) disposées en rangées de la matrice numérotées de façon paire sont électriquement connectées aux deuxièmes électrodes de connexion (180) disposées dans les rangées numérotées de façon paire.

20. Le substrat de réseau (100) de la revendication 19, où les électrodes déversoirs (D) des transistors à couche mince (TFT) disposées en rangées de la matrice numérotées de façon impaire et les électrodes déversoirs (D) des transistors à couche mince (TFT) disposées en rangées de la matrice numérotées de façon paire sont formées sur une ligne longitudinale de la ligne de données (120).

21. Un panneau d'affichage (400), comprenant :

un substrat de réseau (100) selon la revendication 1 ;
un contre-substrat (200) faisant face au substrat de réseau (100) ; et
une couche à cristaux liquides (300) disposée entre le substrat de réseau (100) et le contre-substrat (200).

22. Le panneau d'affichage (400) de la revendication 21, où le contre-substrat (200) comprend :

une couche bloquant la lumière (220) couvrant la première et la deuxième lignes de sous-stockage (164 ; 166) ;
un filtre de couleur (230) couvrant la couche bloquant la lumière (220) ; et

une électrode commune (240) formée sur le filtre de couleur (230).

FIG. 1

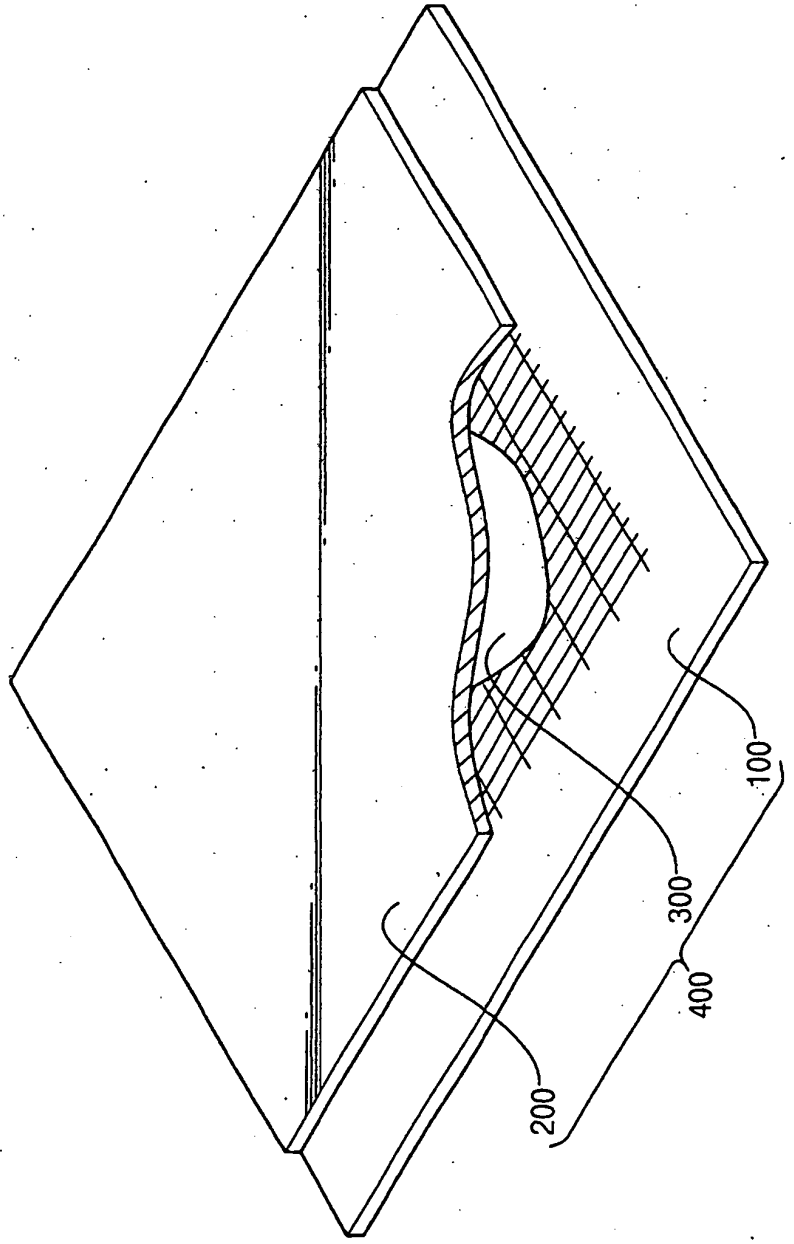


FIG. 2

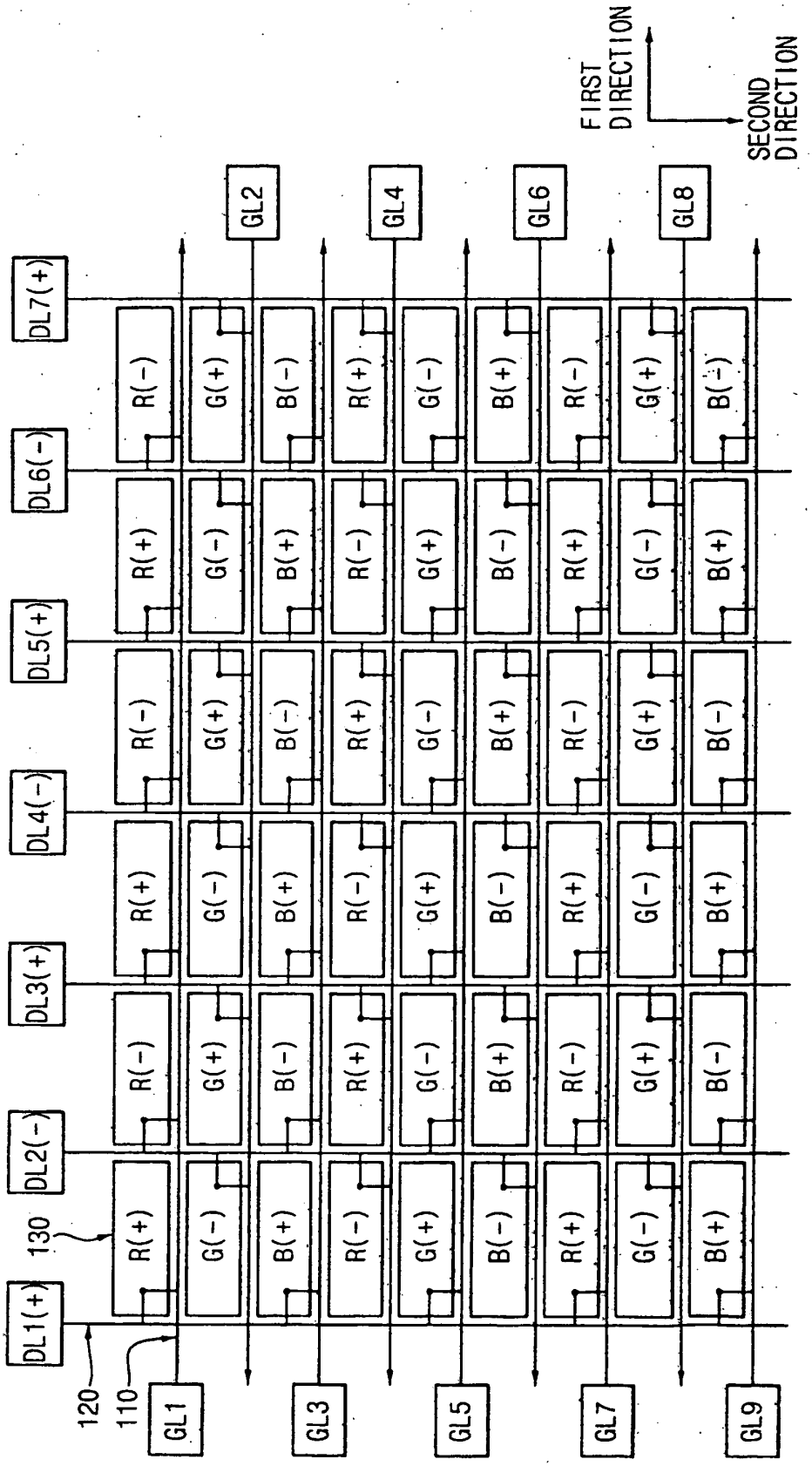

FIRST DIRECTION
SECOND DIRECTION
DL1(+)
DL2(-)
DL3(+)
DL4(-)
DL5(+)
DL6(-)
DL7(+)
GL1
GL2
GL3
GL4
GL5
GL6
GL7
GL8
GL9
120
110
130
R(+)
G(-)
B(+)
R(-)
G(+)
B(-)

FIG. 3

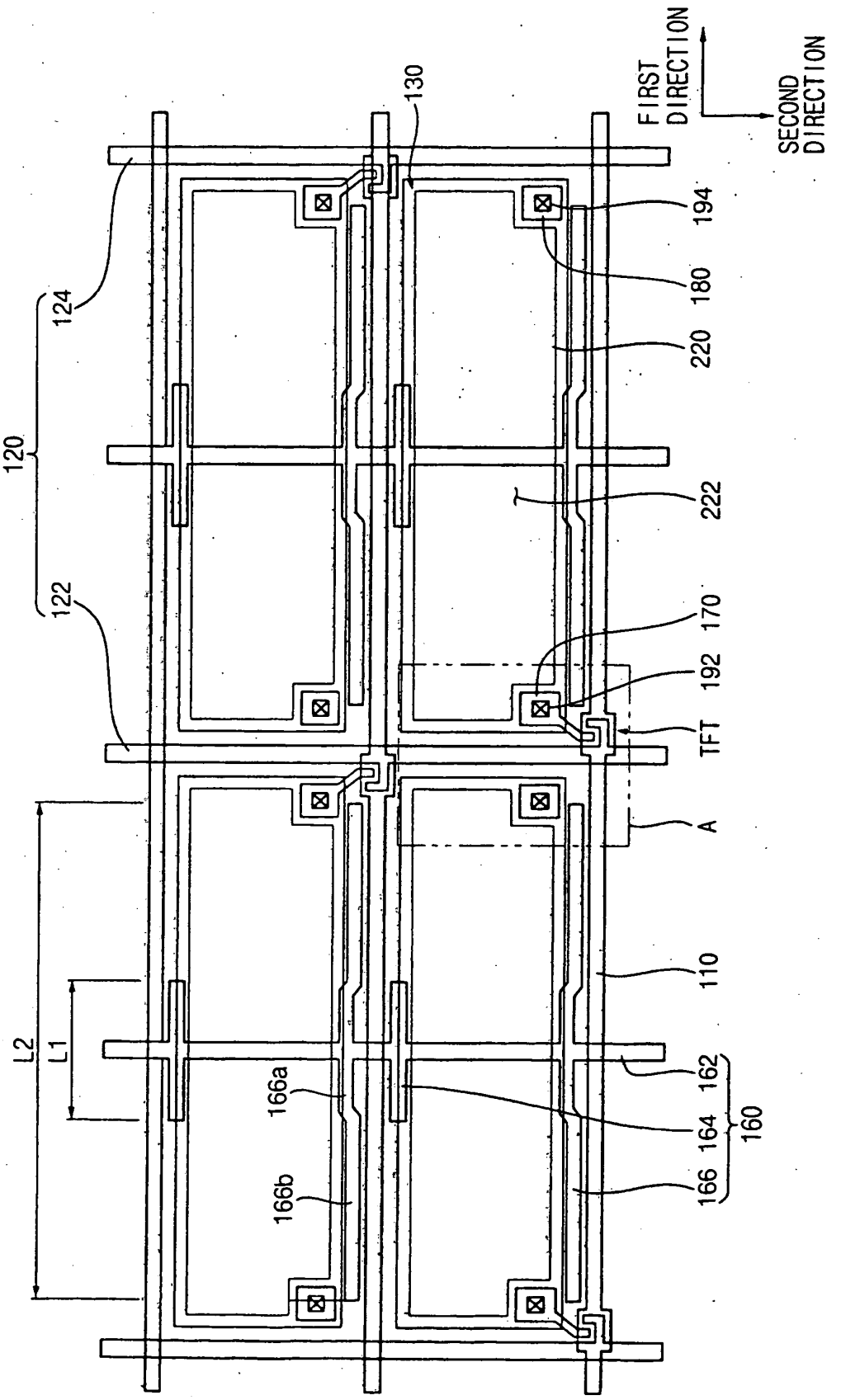

FIRST DIRECTION
SECOND DIRECTION
130
194
180
220
222
170
192
TFT
A
110
162
164
160
166
166a
166b
124
120
122
L1
L2

FIG. 4

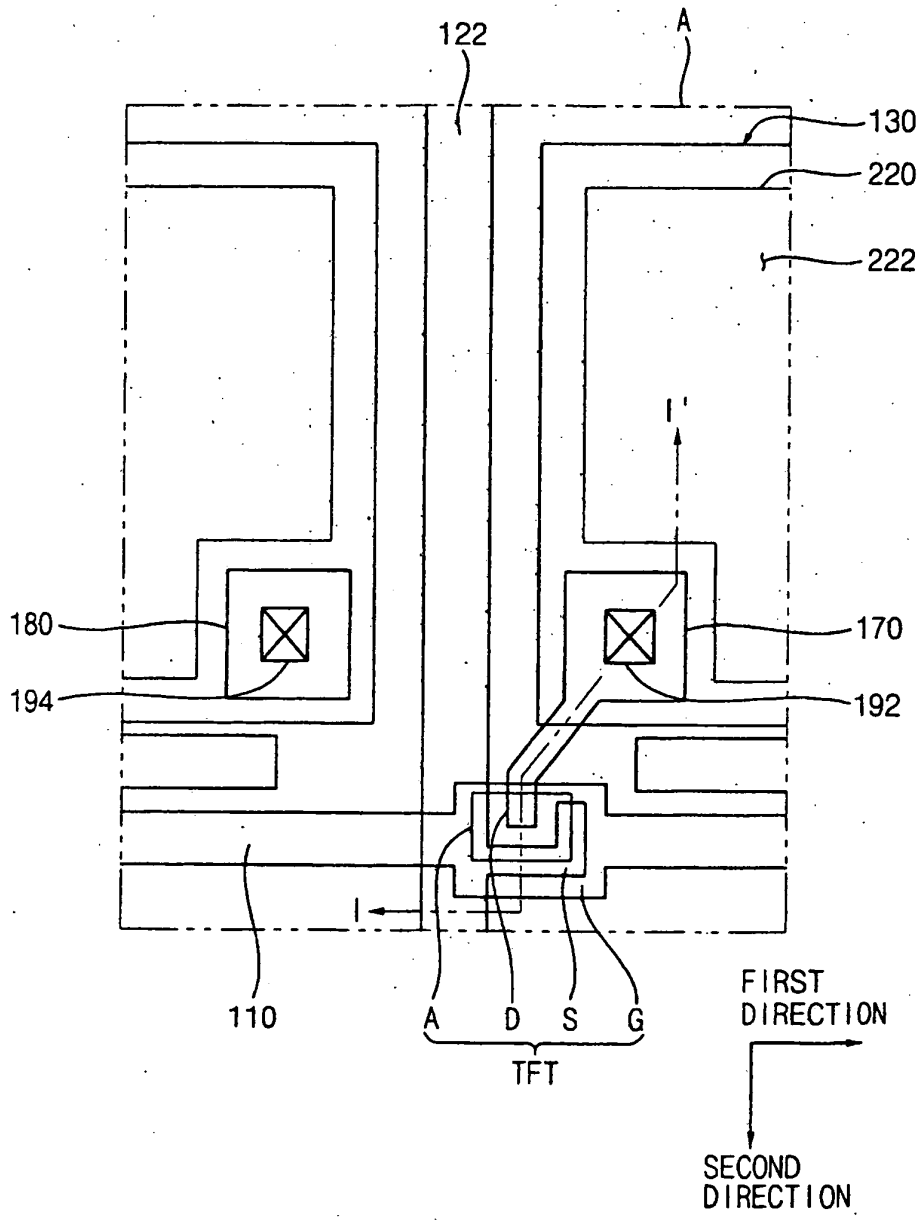

122
A
130
220
222
I'
180
170
194
192
I
110
A
D
S
G
TFT
FIRST DIRECTION
SECOND DIRECTION

FIG. 5

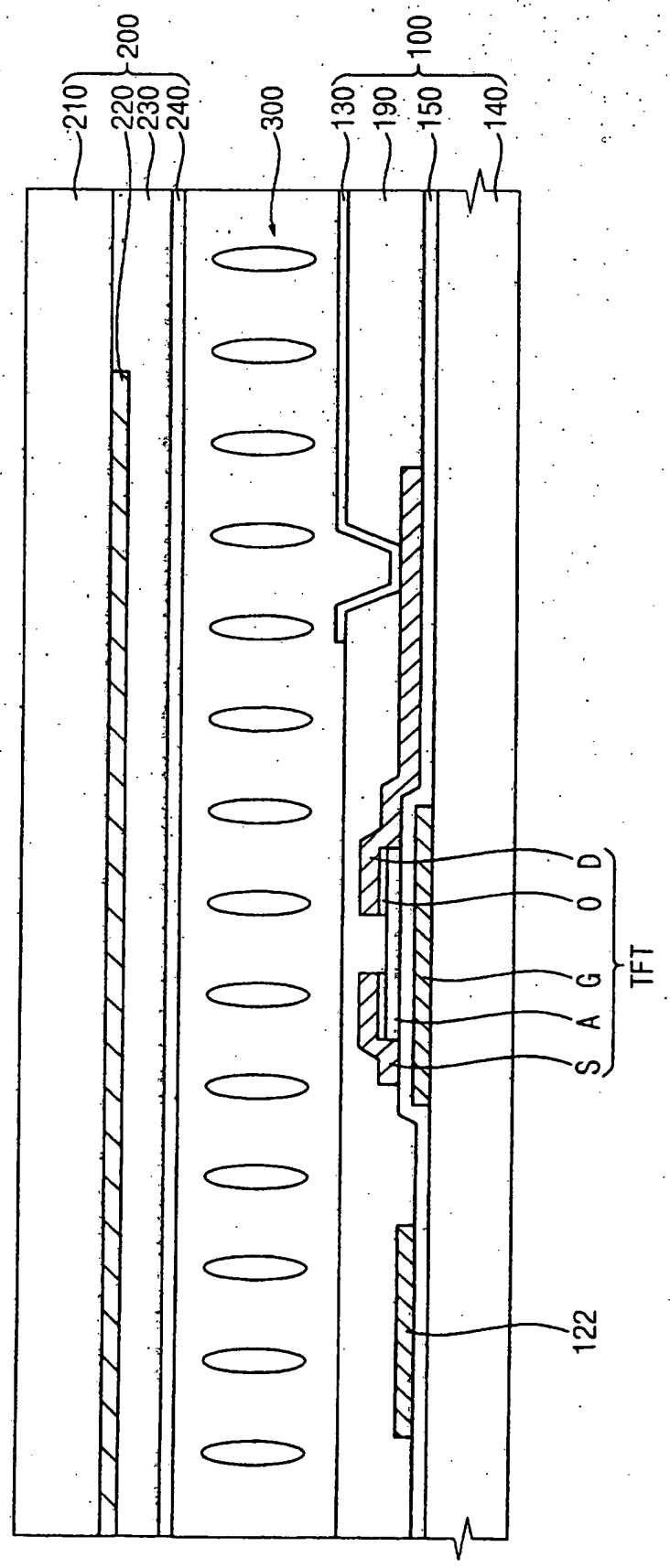


FIG. 6

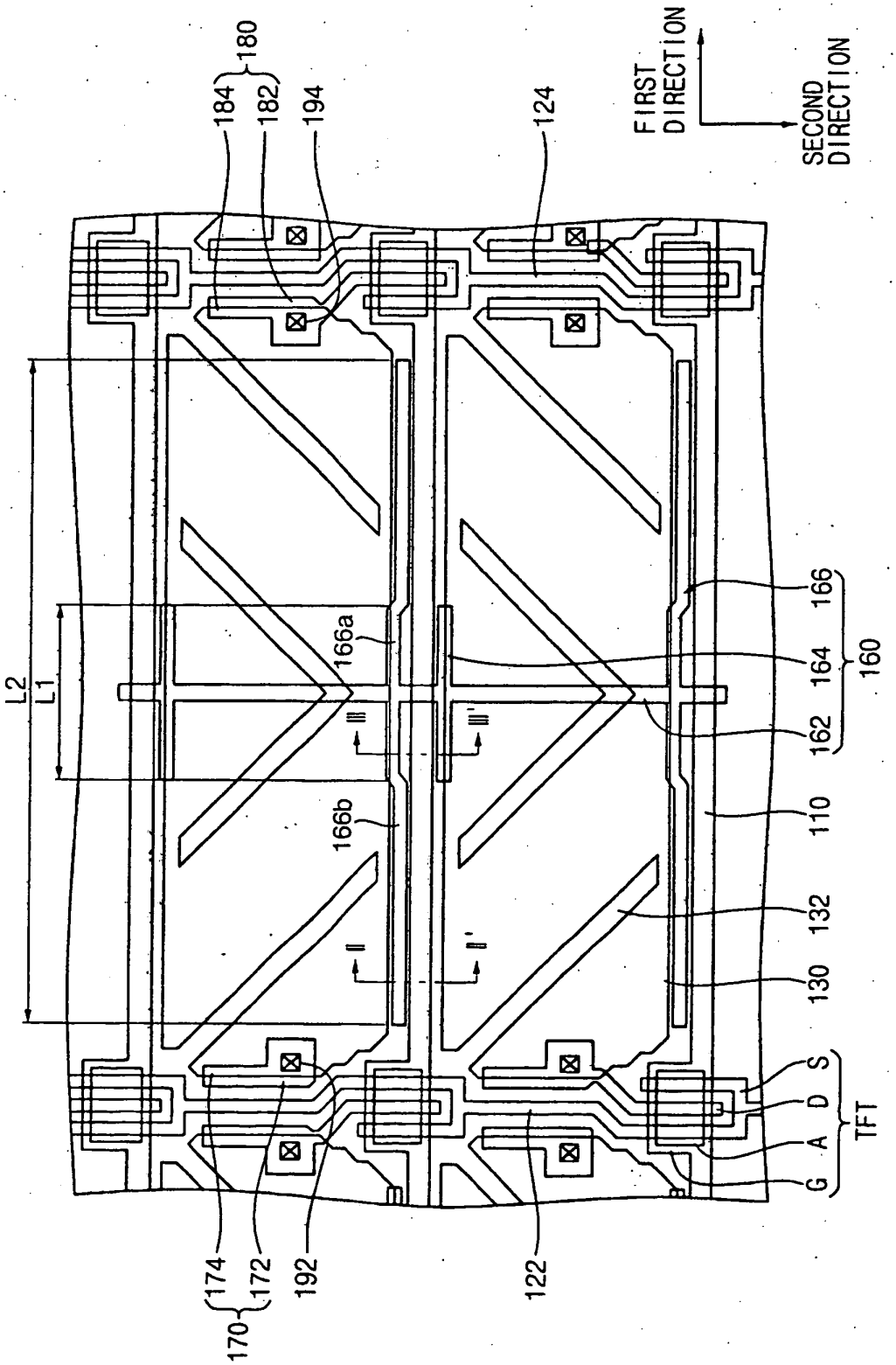

FIRST DIRECTION
SECOND DIRECTION
180
184
182
194
124
L2
L1
166a
166b
166
164
162
160
110
132
130
III
III'
II
II'
S
D
A
G
TFT
174
172
170
192
122

FIG. 7

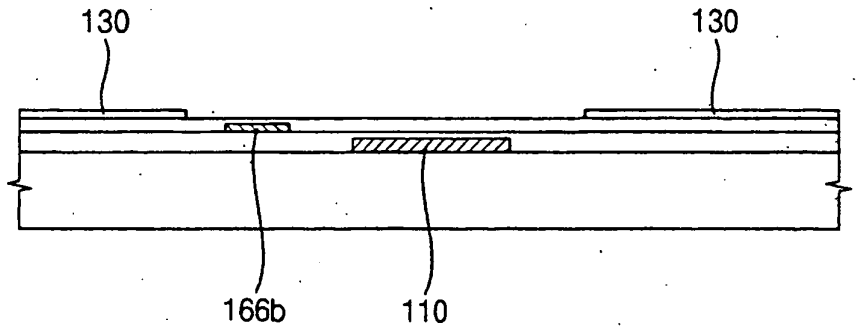


FIG. 8

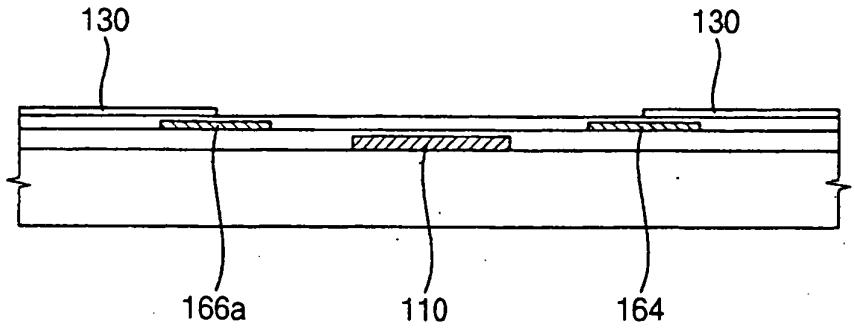


FIG. 9

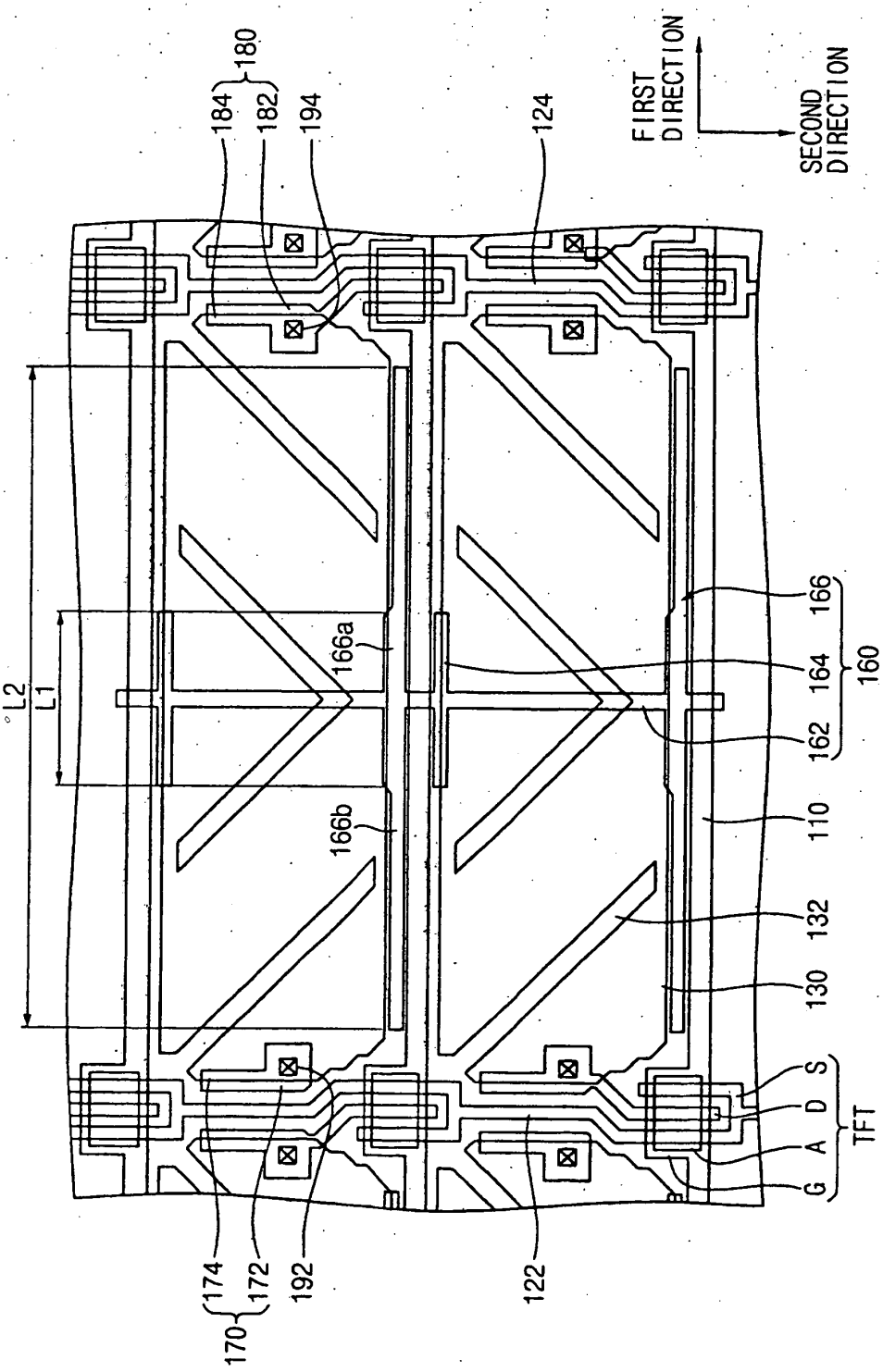

FIRST DIRECTION
SECOND DIRECTION
180
184
182
194
124
166
166a
164
160
162
L2
L1
166b
110
132
130
S
D
A
G
TFT
174
172
170
192
122

FIG. 10

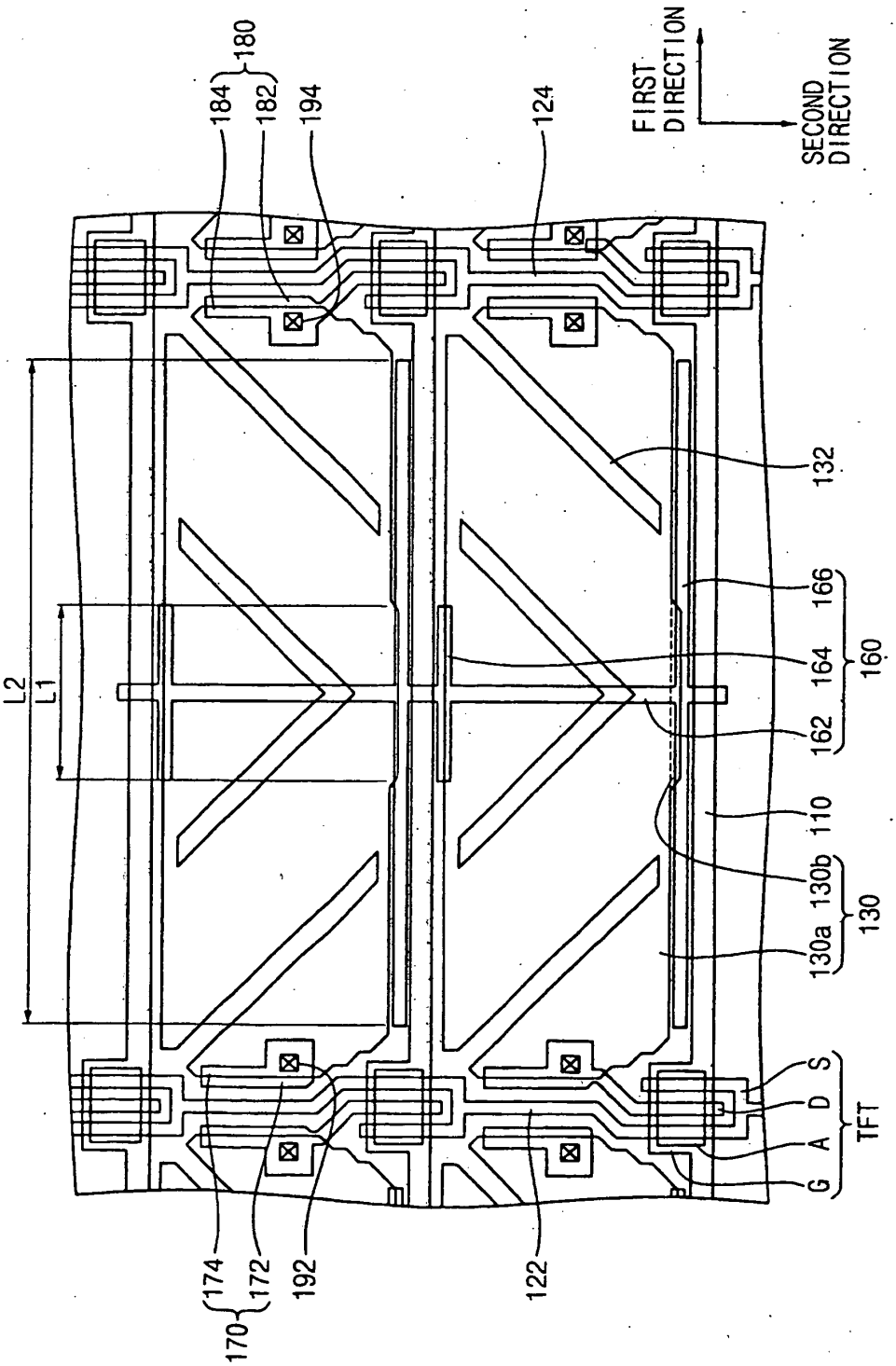
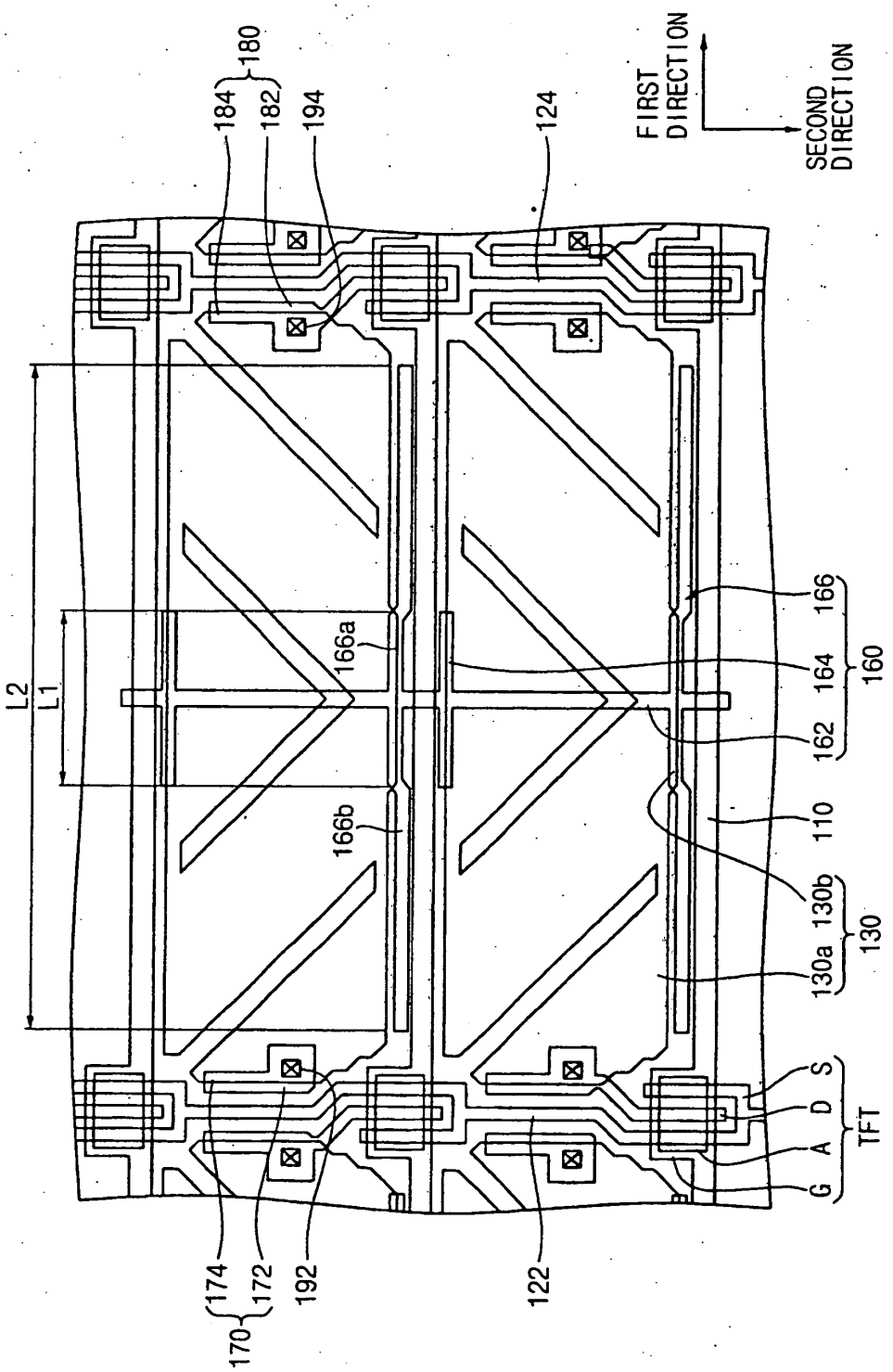

FIRST DIRECTION
SECOND DIRECTION
180
184
182
194
124
132
166
164
160
162
110
130b
130a
130
S
D
A
G
TFT
L2
L1
174
172
170
192
122

FIG. 11


FIRST DIRECTION
SECOND DIRECTION
180
184
182
194
124
166
166a
164
160
162
L2
L1
166b
110
130b
130
130a
S
D
A
G
TFT
174
172
170
192
122

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- KR 200660413 **[0001]**
- US 5943160 A **[0008]**

专利名称(译)	LCD面板阵列基板		
公开(公告)号	EP1873582B1	公开(公告)日	2013-01-16
申请号	EP2007012431	申请日	2007-06-26
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发明人	KIM, DONG-GYU BAEK, SEUNG-SOO		
IPC分类号	G02F1/1362		
CPC分类号	G02F1/136213		
代理机构(译)	DR.威猛和合作伙伴		
优先权	1020060060413 2006-06-30 KR		
其他公开文献	EP1873582A1		
外部链接	Espacenet		

摘要(译)

LCD阵列基板包括栅极线（110），数据线（120），薄膜晶体管，像素电极（130）和存储线（160）。像素电极（130）形成在由栅极线（110）和数据线（120）限定的单位像素中，并且电连接到薄膜晶体管。存储线（160）包括主存储线（162），第一子存储线（164）和第二子存储线（166）。第一子存储线（164）与像素电极（130）的第一边缘部分重叠第一长度。第二子存储线（166）与像素电极（130）的与第一边缘部分相对的第二边缘部分重叠第一长度。这种布置防止了像素电极（130）的未对准引起反冲电压的变化，从而提高了显示图像质量。