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(54) **Thin film transistor array panel and liquid crystal display including the panel**

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(73) Proprietor: **Samsung Electronics Co., Ltd.**
Suwon-si, Gyeonggi-Do (KR)

(72) Inventors:
- **Chai, Chong-Chul**
  Seoul (KR)
- **Choi, Jeong-Ye**
  203-1102 Sanghyeonmaeul
  Gyeonggi-do (KR)
- **Kwag, Jin-Oh**
  Suwon-si
  Gyeonggi-do (KR)
- **Kim, Jin-Hong**
  Gyeonggi-do (KR)
- **Kim, Sang-Il**
  Giheung-eup
  Yongin-si
  Gyeonggi-do (KR)
- **Hong, Mun-Pyo**
  Bundang-gu
  Seongnam-si
  Gyeonggi-do (KR)
- **Roh, Nam-Seok**
  Bundang-gu
  Seongnam-si
  Gyeonggi-do (KR)
- **Yang, Young-Chol**
  Bundang-gu
  Seongnam-si
  Gyeonggi-do (KR)

(74) Representative: **Greene, Simon Kenneth**
Elkington and Fife LLP
Prospect House
8 Pembroke Road
Sevenoaks,
Kent TN13 1XR (GB)

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Description

BACKGROUND OF THE INVENTION

[0001] The present invention relates to a thin film transistor (TFT) array panel and a liquid crystal display (LCD) having the TFT array panel, particularly to a transmissive-reflective LCD and a TFT array panel thereof.

[0002] LCDs are one of the most widely used flat panel displays. An LCD includes a liquid crystal (LC) layer interposed between two panels provided with field-generating electrodes. The LCD displays images by applying voltages to the field-generating electrodes to generate an electric field in the LC layer that determines orientations of LC molecules in the LC layer to adjust polarization of incident light. The light having adjusted polarization is either intercepted or allowed to pass by a polarizing film, thereby displaying images.

[0003] Depending on their light sources, LCDs are classified into a transmissive LCD and a reflective LCD. The light source of the transmissive LCD is a backlight. The light source of the reflective LCD is an external light. The reflective type LCD is usually applied to a small or middle size display device.

[0004] A transmissive-reflective LCD has been under development. The transmissive-reflective LCD uses both a backlight and an external light as the light sources depending on circumstances, and usually applied to small or middle size display devices. The trans-reflective LCD includes a transmissive region and a reflective region in a pixel. While light passes through an LC layer only once in the transmissive region, light passes through the LC layer twice in the reflective region. Accordingly, gamma curves of the transmissive region and the reflective region are not coincident, and images are displayed in different ways between the transmissive region and the reflective region.

[0005] To solve the problem, the LC layer may be formed to have different thicknesses (cell gaps) between the transmissive region and the reflective region. Alternatively, the trans-reflective LCD may be driven by two different driving voltages depending on whether the LCD is in a transmissive mode or a reflective mode.

[0006] However, when the two cell gap structure is applied, a thicker layer is required to be formed on the reflective region, thereby complicating the manufacturing process. Furthermore, since a high step is formed between the transmissive region and the reflective region, the LC molecules are aligned in a disorderly manner around the high step, thereby causing disclination in an image. Also, brightness reversion may occur in a high voltage range. On the other hand, when the two different driving voltages method is applied, gamma curves can not be coincident due to the inconsistency between critical voltages for transmissive brightness and reflective brightness.

[0007] WO 2004/057411 describes a transmissive/reflective LCD array substrate where the pixel region has first and second regions, one reflective, one transmissive. The preamble of claim 1 is based on this document.

[0008] EP 562120 describes an LCD panel with multiple sub-pixels to deliver a greyscale image.

SUMMARY OF THE INVENTION

[0009] The present invention provides an LCD having gamma curves for the reflective mode and the transmissive mode coinciding with each other while achieving a substantially uniform cell gap.

[0010] According to an aspect of the present invention a TFT array panel according to claim 1 or 17 is realised.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] The accompanying drawings are included to provide further understanding of the invention and are incorporated in and constitute a part of this specification.

Fig. 1 is an equivalent circuit diagram of an LCD according to an embodiment of the present invention.
Fig. 2 is a conceptual diagram of an LCD according to an embodiment of the present invention.
Fig. 3 is a sectional view of an LCD according to an embodiment of the present invention.
Figs. 4 and 5 are sectional views of LCDs according to embodiments of the present invention.
Figs. 6A to 6F are graphs illustrating a voltage-transmissive curve and voltage-reflective curves according to area ratios and voltage ratios of the first and second reflective electrodes.
Fig. 7 is a layout view of the LCD illustrated in Fig. 4.
Fig. 8 is a sectional view taken along the line VIII-VIII' of Fig.7.
Fig. 9 is another layout view of the LCD illustrated in Fig. 4.
Fig. 10 is a sectional view taken along the line X-X' of Fig.9.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0012] Preferred embodiments of the present invention will now be described more fully hereinafter with reference to

the accompanying drawings, in which preferred embodiments of the invention are shown. The present invention may, however, be embodied in different forms and should not be construed as being limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art.

[0013] In the drawings, the thickness of layers, films, and regions are exaggerated for clarity. Like numerals refer to like elements throughout. It will be understood that when an element such as a layer, film, region, or substrate is referred to as being "on" another element, it can be directly on the other element or intervening elements may also be present.

[0014] Referring to Figs. 1 and 2, an LCD according to an embodiment of the present application has a TFT array panel 100, a common electrode panel 200 facing the TFT array panel 100, and a liquid crystal layer 3 interposed between the two panels 100 and 200 and having LC molecules aligned in parallel or perpendicular to the two panels 100 and 200. The display signal lines GL and DL are provided on the lower panel 100 and include a plurality of gate lines GL for transmitting gate signals (also referred to as "scanning signals"), and a plurality of data lines DL for transmitting data signals. The gate lines GL extend substantially in a row direction and substantially parallel to each other, while the data lines DL extend substantially in a column direction and substantially parallel to each other.

[0015] Each pixel includes a switching element Q connected to the gate lines GL and the data lines DL, a transmissive LC capacitance C_{LC0}, the first reflective LC capacitance C_{LC1}, an auxiliary capacitance C_{AUX}, a storage capacitance C_{ST}, and the second reflective LC capacitance C_{LC2} connected to the auxiliary capacitance C_{AUX}. The storage capacitance C_{ST} may be omitted. The switching element Q, such as a TFT, is provided on the lower panel 100 and has three terminals: a control terminal connected to one of the gate lines GL; an input terminal connected to one of the data lines DL; and an output terminal connected to the transmissive LC capacitance C_{LC0}, the first reflective LC capacitance C_{LC1}, the auxiliary capacitance C_{AUX}, and the storage capacitance C_{ST}.

[0016] Referring to Fig. 2, the transmissive LC capacitance C_{LC0} is formed between a transmissive electrode 192 provided on the lower panel 100 and a common electrode 270 provided on the upper panel 200. The transmissive electrode 192 is connected to the switching element Q, and the common electrode 270 is supplied with a common voltage V_{com}, and covers the entire surface of the upper panel 200. Altematively, the common electrode 270 may be provided on the lower panel 100. In this case, at least one of the transmissive electrode 192 and the common electrode 270 may be shaped as a bar or a stripe.

[0017] The first reflective LC capacitance C_{LC1} is formed between a first reflective electrode 194 provided on the lower panel 100 and the common electrode 270. The first reflective electrode 194 is connected to the switching element Q via the transmissive electrode 192. The second reflective LC capacitance C_{LC2} is formed between the second reflective electrode 196 provided on the lower panel 100 and the common electrode 270. The second reflective electrode 196 is connected to the auxiliary capacitance C_{AUX} but is electrically separated from the transmissive electrode 192 and the first reflective electrode 194.

[0018] The auxiliary capacitance C_{AUX} is formed between the second reflective electrode 196 or a conductor connected to the second reflective electrode 196 and one of the transmissive electrode 192, the first reflective electrode 194, and a conductor connected thereto. The auxiliary capacitance C_{AUX} divides the voltage applied between the common electrode 270 and the first reflective electrode 194 or the transmissive electrode 192 along with the second reflective LC capacitance C_{LC2}. Accordingly, the voltage applied to the second reflective LC capacitance C_{LC2} is smaller than the voltage applied to the first reflective LC capacitance C_{LC1}.

[0019] In a transmissive region TA defined by the transmissive electrode 192, light from a backlight unit (not illustrated) disposed under the lower panel 100 passes through the liquid crystal layer 3 to display an image. In the first and second reflective region RA1 and RA2 defined by the first and second reflective electrodes 194 and 196, external light such as sun light incidents through the upper panel 200 and passes through the liquid crystal layer 3 to reach the first and second reflective electrodes 194 and 196. Then, the external light is reflected by the first and second reflective electrodes 194 and 196 and passes through the liquid crystal layer 3 again.

[0020] The storage capacitance C_{ST} is an auxiliary capacitance for the LC capacitances C_{LC0}, $C_{LC1}$and C_{LC2}. When the transmissive electrode 192 or the first reflective electrode 194 and a separate signal line (not shown), which is provided on the lower panel 100, are overlapped with each other with an insulator formed therebetween, the overlap portion becomes the storage capacitance C_{ST}. Alternatively, the storage capacitance C_{ST} may be formed by overlapping the transmissive electrode 192 or the first reflective electrode 194 with a previous gate line with an insulator formed therebetween.

[0021] Figs. 3 to 5 depict sectional views of LCDs according to embodiments of the present invention. Referring to Fig. 3, a lower panel 100 has an insulating substrate 110, a storage electrode 133 formed on the insulating substrate 110, a gate insulating layer 140 covering the storage electrode 133, and an output electrode 170 of a switching element Q formed on the gate insulating layer 140. A storage capacitance C_{ST} is formed between the storage electrode 133 and the output electrode 170, which are overlapping each other. The first insulating layer 801 is formed on the output electrode 170 and has a contact hole 183.

[0022] A transmissive electrode 192 is formed on the first insulating layer 801 and is physically and electrically con-

nected to the output electrode 170 through the contact hole 183. The second insulating layer 802 is formed on the transmissive electrode 192 and is disposed on the first and second reflective regions RA1 and RA2. The second insulation layer may have an embossed surface. The first and second reflective electrodes 194 and 196 are formed on the second insulating layer 802. The first reflective electrode 194 is connected to the transmissive electrode 192 and is separated from the second reflective electrode 196. An auxiliary capacitance C_{AUX} is formed between the transmissive electrode 192 and the second reflective electrode 196. The second insulating layer 802 is interposed between the transmissive electrode 192 and the second reflective electrode 196.

[0023] An upper panel 200 has an insulating substrate 210, a color filter 230 formed on the insulating substrate 210, and a common electrode 270 formed on the color filter 230. The transmissive LC capacitance C_{LC0} is formed between the common electrode 270 and the transmissive electrode 192. The first and second reflective LC capacitances C_{LC1} and C_{LC2} are respectively formed between the first and second reflective electrodes 194 and 196 and the common electrode 270. A step is formed between the transmissive region TA and the first and second reflective regions RA1 and RA2 mainly due to the second insulating layer 802, and the step is at least as tall as the thickness of the second insulating layer 802.

[0024] Referring to Fig. 4, a lower panel 100 has an insulating substrate 110, a storage electrode 133 and an auxiliary electrode 120 formed on the insulating substrate 110, a gate insulating layer 140 covering the storage electrode 133 and the auxiliary electrode 120. An output electrode 170 of a switching element Q is formed on the gate insulating layer 140. A storage capacitance C_{ST} is formed between the storage electrode 133 and the output electrode 170, which are overlapping each other, and an auxiliary capacitance C_{AUX} is formed between the auxiliary electrode 120 and the output electrode 170, which are overlapping each other. The gate insulating layer 140 is interposed between the storage electrode 133 and auxiliary electrode 120 and the output electrode 170. An insulating layer 801 is formed on the output electrode 170. The insulating layer 801 may have an embossed surface. A contact holes 183 is formed via the insulating layer 801. A contact hole 184 is formed via the gate insulating layer 140 and the insulating layer 801.

[0025] On the insulating layer 801, a transmissive electrode 192 and the first and second reflective electrodes 194 and 196 are formed. The first reflective electrode 194 is physically and electrically connected to the output electrode 170 through the contact hole 183 and the first reflective electrode 194 is also connected to the transmissive electrode 192. The second reflective electrode 196 is physically and electrically connected to the auxiliary electrode 120 through the contact hole 184 but is separated from the first reflective electrode 194.

[0026] An upper panel 200 has an insulating substrate 210, a color filter 230 formed on the insulating layer 210 and a common electrode 270 formed on the color filter 230. The transmissive LC capacitance C_{LC0} is formed between the common electrode 270 and the transmissive electrode 192. The first and second reflective LC capacitances C_{LC1} and C_{LC2} are respectively formed between the first and second reflective electrodes 194 and 196 and the common electrode 270. It is one of different features from the LCD of Fig. 3 that cell gap is substantially uniform throughout the transmissive region TA and the first and second reflective regions RA1 and RA2.

[0027] Referring to Fig. 5, a lower panel 100 has an insulating substrate 110, a storage electrode 133 formed on the insulating substrate 110, and a gate insulating layer 140 covering the storage electrode 133. An output electrode 170 of a switching element Q is formed on the gate insulating layer 140. A storage capacitance C_{ST} is formed between the storage electrode 133 and the output electrode 170, which are overlapping each other. An insulating layer 801 is formed on the output electrode 170 and has a contact hole 183. The insulating layer may have an embossed surface. On the insulating layer 801, a transmissive electrode 192 and the first and second reflective electrodes 194 and 196 are formed. The first reflective electrode 194 is physically and electrically connected to the output electrode 170 through the contact hole 183. The first reflective electrode 192 is also connected to the transmissive electrode 192 but is separated from the second reflective electrode 196. An auxiliary capacitance C_{AUX} is formed between the second reflective electrode 196 and the output electrode 170. The insulating layer 801 is interposed between the second reflective electrode 196, which are overlapping each other.

[0028] An upper panel 200 has an insulating substrate 210, a color filter 230 formed on the insulating substrate 210 and a common electrode 270 formed on the color filter 230. The transmissive LC capacitance C_{LC0} is formed between the common electrode 270 and the transmissive electrode 192. The first and second reflective LC capacitances C_{LC1} and C_{LC2} are respectively formed between the first and second reflective electrodes 194 and 196 and the common electrode 270. The cell gap is substantially uniform throughout the transmissive region TA and the first and second reflective regions RA1 and RA2.

[0029] Methods of making a voltage-reflective curve coincident with a voltage-transmissive curve will be described with reference to Figs. 6A to 6F, which illustrate a voltage-transmissive curve and voltage-reflective curves according to area ratios and voltage ratios of the first and second reflective electrodes.

[0030] When a data voltage corresponding to an image signal is applied to the transmissive electrode 192 and the first reflective electrode through the switching element Q, a voltage difference V (e.g. a pixel voltage) between the data voltage and the common voltage V_{com} is formed between the two terminals of the transmissive LC capacitance C_{LC0} and the first reflective LC capacitance C_{LC1}. However, a voltage difference V2 smaller than the pixel voltage V is formed

between the two terminals of the second reflective LC capacitance C_{LC2} due to the auxiliary capacitance C_{AUX} and is described by following Equation 1.

[Equation 1]

$$V2 = \frac{C_{AUX}}{(C_{AUX} + C_{LC2})} V$$

[0031] The voltage-transmissive curves VT shown in Figs. 6A to 6F represent variation of brightness in the transmissive region TA with respect to variation of the pixel voltage V. The first voltage-reflective curves VR1 represent variation of brightness in the reflective region RA with respect to variation of the pixel voltage V. The voltage-transmissive curves VT and the first voltage-reflective curves VR1 are obtained based on measured data from test panels. The test panels are manufactured to have the transmissive electrode 192 and the first reflective electrode 194 but does not have the second reflective electrode 196. The second voltage-reflective curves VR2 are obtained based on calculated data by Equation 1 and the first voltage-reflective curve VR1. The third voltage-reflective curves VR3 are obtained by composing the first voltage-reflective curves VR1 and second voltage-reflective curve VR2. The resulting curves in Figs. 6A to 6F are differentiated by area ratios of the first reflective region RA1 and the reflective region RA2.

[0032] When the first voltage-reflective curves VR1, second voltage-reflective curves VR2, and third voltage-reflective curves VR3 are respectively represented by functions R1 (V), R2(V), and R3(V), following Equation 2 is provided.

[Equation 2]

$$R3(v) = (1 - AR) \cdot RA1(V) + AR \cdot RA2(V)$$

$$= (1 - AR) \cdot RA1(V) + AR \cdot RA1(kV)$$

[0033] Here, $AR = \frac{A2}{(A1 + A2)}$, $k = \frac{C_{AUX}}{(C_{AUX} + C_{LC2})}$ and A1 and A2 respectively represent areas of the first and second reflective regions RA1 and RA2. That is, AR represent an area ratio between the whole reflective region and the second reflective region RA2, k represents a voltage ratio between the pixel voltage V and the voltage V2 applied to the second reflective LC capacitance C_{LC2}.

[0034] A simulation was performed by varying the area ratio AR and the voltage ratio k to achieve a third voltage-reflective curve VR3, which is most similar to the voltage-transmissive curve VT. Initially, while the area ratio AR was fixed at a certain value and the voltage ratio was varied, the shape of the third voltage-reflective curve VR3 and the voltage-transmissive curve VT was checked. Then, the area ratio was changed to a different value and the same processes were repeated. Simulations were performed with respect to the area ratios AR of 0.4, 0.5, 0.6, and 0.7. The best third voltage-reflective curve VR3 is provided when the area ratio AR is 0.6 and the voltage ratio k is 0.82. Fig. 6A illustrates the best third voltage-reflective curve VR3, which is almost coincident with the voltage-transmissive curve VT.

[0035] Figs. 6B, 6C, and 6D respectively illustrate the third voltage-reflective curves VR3 with respect to the area ratios AR 0.4, 0.5, and 0.7. The voltage ratio k of each case is adjusted to have the third voltage-reflective curve VR3 approach to the voltage-transmissive curve VT. The most appropriate voltage ratios k for the respective area ratios AR 0.4, 0.5, and 0.7 are 0.78, 0.80, and 0.84. The third voltage-reflective curves VR3 of Figs. 6B, 6C, and 6D deviate a little from the voltage-transmissive curve VT but are still satisfactory.

[0036] Figs. 6E and 6F illustrate the third voltage-reflective curves VR3 provided when the area ratio AR is 0.6 and the voltage ratios k are respectively 0.78 and 0.86. As shown therein, inconsistency between the third voltage-reflective curves VR3 and the voltage-transmissive curve VT is increased.

[0037] Referring to the result of the simulation, when the area ratio AR has a value ranging from 0.4 to 0.7 and the voltage ratio k has a value ranging from 0.78 to 0.86, the third voltage-reflective curve VR3 close to the voltage-transmissive curve VT is provided.

[0038] A value of the auxiliary capacitance C_{AUX} for making the voltage ratio k to be 0.82 is calculated by the following Equation 3.

[Equation 3]

$$0.82 = \frac{C_{AUX}}{(C_{AUX} + C_{LC2})}$$

$$C_{AUX} = 4.56 * C_{LC2}$$

[0039] That is, the auxiliary capacitance C_{AUX} is required to be 4.56 times the capacitance of the second reflective LC capacitance C_{LC2}.

[0040] A capacitance C of a flat capacitor is calculated by the following Equation 4.

$$C = \varepsilon \frac{A}{d}$$

where A is the electrode area, d is a distance between the two electrodes, and ε is a dielectric constant.

[0041] Since silicon nitride (SiNx), which is a commonly used insulating material, has a dielectric constant ε_{SiNx} similar with that ε_{LC} of a liquid crystal layer, when the electrodes of the second reflective LC capacitance C_{LC2} and the auxiliary capacitance C_{AUX} have the same area, the thickness d_{SiNx} of the insulating layer which works as a dielectric of the auxiliary capacitance C_{AUX} is calculated by the following Equation 5.

[Equation 5]

$$\frac{\varepsilon_{SiNx}}{d_{SiNx}} = 4.56 \frac{\varepsilon_{LC}}{d_{LC}}$$

$$d_{SiNx} = \frac{1}{4.56} \frac{\varepsilon_{SiNx}}{\varepsilon_{LC}} d_{LC}$$

$$d_{SiNx} = \frac{1}{4.56} d_{LC}$$

[0042] Here, d_{LC} represents a thickness of the liquid crystal layer of the second reflective LC capacitance C_{LC2}. When the thickness d_{LC} of the liquid crystal layer is 3 μm, the thickness of the insulating layer is 0.66 μm. Such thickness of the insulating layer may be unreasonable in a view from manufacturing process. Accordingly, when the insulating layer is required to thinner, the electrode area of the auxiliary capacitance C_{AUX} may be reduced to provide an auxiliary capacitance appropriate to Equation 3. For example, as shown in Fig. 4, a required auxiliary capacitance C_{AUX} may be provided by adjusting the overlapping area between the output electrode 170 and the auxiliary electrode 120.

[0043] Henceforth, a structure of an LCD according to an embodiment of the present invention will be described in detail. Fig. 7 is a layout view of the LCD illustrated in Fig. 4. Fig. 8 is a sectional view taken along the line VIII-VIII' of Fig.7. The LCD has a TFT array panel 100, a common electrode panel 200 facing the TFT array panel 100, and a liquid crystal layer 3 interposed between the two panels 100 and 200 and having LC molecules aligned in parallel or perpendicular to the two panels 100 and 200.

[0044] Referring to Figs. 7 and 8, a plurality of gate lines 121, storage electrode lines 131, and auxiliary electrodes 126 are formed on an insulating substrate 110. The gate lines 121 are extended in the horizontal direction and transmitting gate signals. A plurality of gate electrodes 124 are extended from the gate lines 121. An end portion 129 of the gate line 121 is expanded to form a contact with an external device such as a driving circuit.

[0045] The storage electrode lines 131 are extended in the horizontal direction and expanded at certain portions to form the storage electrodes 133. The storage electrode lines 131 are applied with a predetermined voltage such as a

common voltage that is applied to a common electrode 270 of the common electrode panel 200 or a storage voltage that is different from the common voltage. Each auxiliary electrode 126 is disposed between the gate line 121 and the storage electrode line 131 and separated from the gate line 121 and the storage electrode line 131 with predetermined distances.

[0046] The gate lines 121, the auxiliary electrode 126, and the storage electrode line 131 are preferably made of one of an Al based metal such as pure Al and an Al alloy, an Ag based metal such as pure Ag and an Ag alloy, a Cu based metal such as Cu and a Cu alloy, a Mo based metal such as Mo and a Mo alloy, Cr, Ti, and Ta. The gate lines 121, the auxiliary electrode 126, and the storage electrode lines 131 may be formed of two films having different physical characteristics, a lower film and an upper film. The upper film is preferably made of a low resistivity metal including Al, such as Al and Al alloy, for reducing signal delay or voltage drop in the gate lines 121, the auxiliary electrode 126, and the storage electrode lines 131. On the other hand, the lower film is preferably made of a material such as Cr, Mo, and Mo alloy such as MoW, which has good physical, chemical and electrical contact characteristics with other materials such as indium tin oxide (ITO) and indium zinc oxide (IZO). An example of combination of the lower film material and the upper film material is Cr and Al-Nd alloy. The gate lines 121, the auxiliary electrode 126, and the storage electrode lines 131 may have multi-layers more than or equal to three.

[0047] The lateral sides of the gate lines 121, the auxiliary electrode 126, and the storage electrode lines 131 may be inclined with respect to a surface of the substrate 110 at an angle ranging between about 30 degrees to about 80 degrees. A gate insulating layer 140 made of a dielectric, such as SiNx, is formed on the gate lines 121 and the storage electrode lines 131. A plurality of semiconductor stripes 151 preferably made of hydrogenated amorphous silicon (abbreviated to "a-Si") are formed on the gate insulating layer 140. Each semiconductor stripe 151 extends substantially in the longitudinal direction and has a plurality of projections 154 branched out toward the gate electrodes 124. The semiconductor stripe 151 becomes wider at portions intersecting the gate lines 121 to cover a wide area of the gate line 121.

[0048] A plurality of ohmic contact stripes 161 and islands 165, preferably made of silicide or n+ hydrogenated a-Si heavily doped with an n type impurity, are formed on the semiconductor stripes 151. Each ohmic contact stripe 161 has a plurality of projections 163, and the projections 163 and the ohmic contact islands 165 are located in pairs on the projections 154 of the semiconductor stripes 151. The lateral sides of the semiconductors 151 and the ohmic contacts 161 and 165 are inclined with respect to a surface of the substrate 110 at an angle ranging between about 30 degrees to about 80 degrees.

[0049] A plurality of data lines 171 and a plurality of drain electrodes 175 are formed on the ohmic contacts 161 and 165 and the gate insulating layer 140. The data lines 171 for transmitting data voltages extend substantially in the longitudinal direction and intersect the gate lines 121. Each data line 171 includes an expended area 179 for contacting with another layer or an external device. Each drain electrode 175 has an expansion 177 overlapping the storage electrode 133 and the auxiliary electrode 126. The expansion 177 has an opening 178 exposing the auxiliary electrode 126.

[0050] A plurality of branches of each data line 171, which face the drain electrodes 175, form a plurality of source electrodes 173. Each pair of the source electrodes 173 and the drain electrodes 175 are separated from each other and opposite each other with respect to a gate electrode 124. The gate electrode 124, the source electrode 173, and the drain electrode 175 along with the projection 154 of the semiconductor stripe 151 form a TFT having a channel formed in the projection 154 disposed between the source electrode 173 and the drain electrode 175.

[0051] The data lines 171 and the drain electrodes 175 are preferably made of a material having high resistance against chemicals, such as Cr, Mo based metal, Ta, and Ti. The data lines 171 and the drain electrodes 175 may have a multi-layered structure including a lower film made of Mo, a Mo alloy, or Cr and an upper film located thereon and made of an Al containing metal or an Ag containing metal. Similar to the gate lines 121 and the storage electrode lines 131, the data lines 171 and the drain electrodes 175 have inclined lateral sides with respect to the surface of the substrate 110 at an angle ranging between about 30 degrees to about 80 degrees.

[0052] The ohmic contacts 161 and 165 are interposed only between the underlying semiconductors 151 and 154 and the overlying data lines 171 and drain electrodes 175 and reduce the contact resistance therebetween. The semiconductor stripes 151 has a plurality of exposed portions, which are not covered with the data lines 171 and the drain electrodes 175, such as portions located between the source electrodes 173 and the drain electrodes 175.

[0053] A passivation layer 180 made of an inorganic material, such as silicon nitride and silicon oxide, is formed on the data lines 171, the drain electrodes 175, and the exposed portions of the semiconductor stripes 151, which are not covered with the data lines 171 and the drain electrodes 175. An organic insulating layer 187 is formed on the passivation layer 180. The organic insulating layer 187 is formed from a photosensitive organic material having good planarization characteristics, and has an embossed surface. The organic insulating layer 187 is removed at on expansions 129 and 179 of the gate lines 121 and the data lines 171, thereby exposing the passivation layer 180.

[0054] The passivation layer 180 has contact holes 182 exposing the expansions 179 of the data lines 171. The passivation layer 180 and the gate insulting layer 140 have contact holes 181 exposing the expansions 129 of the gate lines 121. The passivation layer 180 and the organic insulating layer 187 have contact holes 185 exposing the expansions

177 of the drain electrodes 175. The passivation layer 180, the organic insulating layer 187, and the gate insulating layer 140 have contact holes 186 exposing the auxiliary electrodes 126. The contact holes 186 are formed through the openings 178 of the expansions 177 and are separated from the boundaries of the openings 178 with a sufficient gap therebetween. The contact holes 181, 182, 185, and 186 may have various shapes, such as polygonal or circular shape, and may have lateral surfaces inclined with respect to a surface of the substrate 110 at an angle ranging between about 30 degrees to about 85 degrees.

[0055] A plurality of transmissive electrodes 192 and 193 are formed on the organic insulating layer 187 and a plurality of first and second reflective electrodes 194 and 196 are respectively formed on the transmissive electrodes 192 and 193. The transmissive electrodes 192 and 193 are made of a transparent conductive material, such as ITO or IZO, and the reflective electrodes 194 and 196 are made of a metal having high reflectance, such as Al, an Al alloy, Ag, or an Al alloy. The reflective electrodes 194 and 196 have embossed surfaces due to the embossed surface of the organic insulating layer 187, thereby enhancing reflective characteristics.

[0056] A contact assistant layer (not illustrated) made of Mo, a Mo alloy, Cr, Ti, or Ta may be interposed between the transmissive electrodes 192 and 193 and the reflective electrodes 194 and 196. The contact assistant layer enhances contact characteristics between the transmissive electrode 192 and 193 and the reflective electrode 194 and 196, thereby preventing the reflective electrodes 194 and 196 from being corroded due to the transmissive electrodes 192 and 193.

[0057] A pixel has a transmissive region TA and a first and second reflective regions RA1 and RA2. The transmissive region TA is a region where the first reflective electrode 194 is eliminated to expose the transmissive electrode 192. The first reflective region RA1 is a region where the first reflective electrode 194 is disposed, and the second reflective region RA2 is a region where the second reflective electrode 196 is disposed. The cell gap is substantially uniform in the whole region of a pixel throughout the transmissive region TA and the first and second reflective regions RA1 and RA2.

[0058] The transmissive electrodes 192 and the first reflective electrodes 194 are physically and electrically connected to the expansions 177 of the drain electrodes 175 through the contact holes 185 such that the transmissive electrodes 192 receive the data voltages from the drain electrodes 175. The transmissive electrodes 192 supplied with the data voltages generate electric fields in cooperation with the common electrode 270 of the common electrode panel 200. The electric fields reorient the liquid crystal molecules in the liquid crystal layer 3 disposed therebetween.

[0059] The transmissive LC capacitance C_{LC0} is formed between the exposed transmissive electrodes 192 and the common electrode 270, and the first reflective LC capacitance C_{LC1} is formed between the first reflective electrodes 194 and the common electrode 270. The storage capacitance C_{ST}, which stores applied voltages after turn-off of the TFT is connected in parallel to the LC capacitances C_{LC0} and C_{LC1}. The storage capacitances C_{ST} are implemented by overlapping the expansions 177 of the drain electrodes 175 with the storage electrodes 133. The storage capacitances C_{ST} may be implemented by overlapping of the transmissive electrode 192 and previous gate lines 121. In this case, the storage electrode lines 131 may be omitted.

[0060] The auxiliary capacitances C_{AUX} are formed by overlapping the expansions 177 of the drain electrodes 175 with the auxiliary electrodes 126 and by overlapping the expansions 177 of the drain electrodes 175 with the second reflective electrodes 196. The second reflective electrodes 196 receive voltage lower than the data voltage of the drain electrode 175 due to the auxiliary capacitances C_{AUX}.

[0061] The transmissive electrodes 193 and the second reflective electrodes 196 are connected to the auxiliary electrodes 126 through the contact holes 186. The second reflective electrode 196 supplied with the voltages lower than the data voltages generate electric fields in cooperation with a common electrode 270. The electric fields reorient the LC molecules in the liquid crystal layer 3 disposed therebetween.

[0062] The second reflective LC capacitances C_{LC2} is formed between the second reflective electrodes 196 and the common electrode 270. The second reflective LC capacitances C_{LC2} are connected with the auxiliary capacitances C_{AUX} in series. Optionally, the second reflective electrodes 196 may overlap the gate lines 121 to increase a reflective ratio. Contrarily, the transmissive electrodes 192 and the first and second reflective electrodes 194 and 196 do not overlap the adjacent data lines 171 but they may overlap the adjacent data lines 171 to increase an aperture ratio and a reflective ratio.

[0063] A plurality of contact assistants 81 and 82 are formed on the passivation layer 180. The contact assistants 81 and 82 are connected to the exposed expansions 129 of the gate lines 121 and the exposed expansions 179 of the data lines 171 through the contact holes 182 and 183, respectively. The contact assistants 81 and 82 protect the expansions 129 and 179 and complement the adhesion between the expansions 129 and 179 and external devices. The contact assistants 81 and 82 are not essential components and may be formed of the same material as one of the transmissive electrodes 192 and 193 or the reflective electrodes 194 and 196.

[0064] The common electrode panel 200 facing the TFT array panel 100 includes an insulating substrate 210 formed of a transparent material such as a glass and a light blocking member 220 called as a black matrix. The light blocking member 220 prevents light leakage between the pixel electrodes and defines aperture regions corresponding to the pixel electrodes. In this invention, the pixel electrode is composed of the transmissive electrodes 192 and the reflective electrodes 194 and 196.

[0065] A plurality of color filters 230 are formed on the substrate 210 and the light blocking member 220 to fill the aperture regions defined by the light blocking member 220. The color filters 230 disposed between two adjacent data lines 171 and aligned in a column may be connected to each other to form a stripe. The color filters 230 may filter one of the three primary colors such as red, green, and blue.

[0066] Each color filter 230 has a substantially uniform thickness in the whole pixel region throughout the transmissive region TA and the first and second reflective region RA1 and RA2. The color filters 230 have light holes 240 disposed in the reflective regions RA1 and RA2. Hence, a difference in color tone between the two regions TA and RA due to number difference of transmitting the color filter 230, is compensated. As another way to compensate the difference of color tone, the thickness of the color filters 230 may be differentiated between the transmissive regions TA and the reflective regions RA1 and RA2. Fillers are formed in the light holes 240 for planarization of surfaces of the color filters 230, thereby reducing step difference due to the light holes 240. A common electrode 270 made of ITO or IZO is formed on the light blocking member 220 and the color filters 230.

[0067] An LCD according to another embodiment of the present invention will be described with reference to Figs. 9 and 10. Fig. 9 is another layout view of the LCD illustrated in Fig. 4. Fig. 10 is a sectional view taken along the line X-X' of Fig. 9. The LCD has a TFT array panel 100, a common electrode panel 200 facing the TFT array panel 100, and a liquid crystal layer 3 interposed between the two panels 100 and 200 and having LC molecules aligned in parallel or perpendicular to the two panels100 and 200.

[0068] The TFT array panel 100 has a plurality of gate lines 121 including gate electrodes 124, a plurality of storage electrode lines 131 including storage electrodes 133, and a first auxiliary electrode 127, which are formed on a substrate 110. The storage electrodes 133 are disposed adjacent to the gate lines 121 but are spaced apart from the first auxiliary electrodes 127. The first auxiliary electrodes 127 are disposed adjacent to the previous gate lines 121. The first auxiliary electrodes 127 are made of the same material as the gate lines 121 and storage electrode lines 131 and may have a single-layered or a multi-layered structure. A gate insulting layer 140, a plurality of semiconductor stripes 151 including protrusions 154, and a plurality of ohmic contact stripes 161 having protrusions 163 and ohmic contact island 165 are sequentially formed on the gate lines 121, first auxiliary electrodes 127, and the storage electrode lines 131.

[0069] A plurality of data lines 171 having source electrodes 173 and a plurality of drain electrodes 175 are formed on the ohmic contacts 161 and 165 and the gate insulating layer 140. A plurality of second auxiliary electrodes 176 are formed on the gate insulating layer 140, and the second auxiliary electrodes 176 have openings 174. The second auxiliary electrodes 176 are separated from the data lines 171 and the drain electrodes 175. The second auxiliary electrodes 176 have almost the same planar shape as the first auxiliary electrodes 127 and overlap the first auxiliary electrodes 127. The second auxiliary electrodes 176 are made of the same material as the data lines 171 and the drain electrodes 175 and may have a multi-layered structure.

[0070] A passivation layer 180 and an organic insulating layer 187 having an embossed surface are sequentially formed on the data lines 171, the drain electrodes 175, and the second auxiliary electrodes 176. The passivation layer has a plurality of contact holes 181 and 182. The passivation layer 180 and the organic insulating layer 187 have a plurality of contact holes 185 and 188 respectively exposing expansions 177 of the drain electrodes 175 and the second auxiliary electrodes 176. The passivation layer 180, the organic insulating layer 187, and the gate insulating layer 140 have a plurality of contact holes 189 exposing the first auxiliary electrodes 127. The contact holes 189 are formed through the openings 174 of the second auxiliary electrodes 176 and are separated from the boundaries of the openings 174 with a sufficient gap therebetween. The contact holes 181, 182, 185, 188, and 189 may have various shapes such as polygonal or circular shape and may have lateral surfaces inclined with respect to a surface of the substrate 110 at an angle ranging between about 30 to about 85 degrees.

[0071] A plurality of transmissive electrodes 192 and 193 are formed on the organic insulating layer 187 and a plurality of first and second electrodes 194 and 196 are respectively formed on the transmissive electrodes 192 and 193. A pixel has a transmissive region TA and a first and second reflective regions RA1 and RA2. The transmissive region TA is a region where the first reflective electrode 194 is eliminated to expose the transmissive electrode 192. The first reflective region RA1 is a region where the first reflective electrode 194 is disposed, and the second reflective region RA2 is a region where the second reflective electrode 196 is disposed. In this embodiment, the transmissive region TA is arranged between the first reflective region RA1 and the second reflective region RA2.

[0072] The transmissive electrodes 192 and the first reflective electrodes 194 are physically and electrically connected to the expansions 177 of the drain electrodes 175 through the contact holes 185 such that the transmissive electrodes 192 receive the data voltages from the drain electrodes 175. The exposed transmissive electrodes 192 and the common electrode 270 form a transmissive LC capacitance C_{LC0} and the first reflective electrodes 194 and the common electrode 270 form a first reflective LC capacitance C_{LC1}, which store applied voltages after turn-off of the TFT.

[0073] The transmissive electrodes 192 have protrusions protruding toward the second reflective regions RA2. The protrusions are physically and electrically connected to the second auxiliary electrodes 176 through the contact holes 188, thereby transmitting the data voltage to the second auxiliary electrodes 176. The first auxiliary electrodes 127 overlap the second auxiliary electrodes 176 to form the auxiliary capacitances C_{AUX}. The first auxiliary electrodes 127

receive voltages lower than the data voltages applied to the second auxiliary electrode 176 due to the auxiliary capacitances C_{AUX}.

[0074] The transmissive electrodes 193 and the second reflective electrodes 196 are physically and electrically connected to the first auxiliary electrodes 127 through the contact holes 189 and receive voltages lower than the data voltages. The second reflective electrode 196 supplied with the voltages lower than the data voltages generate electric fields in cooperation with a common electrode 270. The electric fields reorient LC molecules in the liquid crystal layer 3 disposed therebetween. The second reflective electrodes 196 and the common electrode 270 form the second reflective LC capacitances C_{LC2}. The second reflective LC capacitances C_{LC2} are connected with the auxiliary capacitances C_{AUX} in series.

[0075] The common electrode panel 200 facing the TFT array panel 100 includes the insulating substrate 210 formed of a transparent material such as a glass and the light blocking member 220, a plurality of color filters 230, and the common electrode 270 formed on the insulating substrate 210. The color filters 230 have light holes 240.

[0076] In the present invention, each reflective region is divided into two sub-regions. A data voltage is applied to one of the two sub-regions and a voltage lower than the data voltage is applied to the other sub-region. Hereby, an LCD having gamma curves of the reflective mode and the transmissive mode coinciding with each other and having a substantially uniform cell gap is provided.

[0077] Although preferred embodiments of the present invention have been described in detail hereinabove, it should be clearly understood that many variations, which may appear to those skilled in the present art, will still fall within the scope of the appended claims.

Claims

1. A thin film transistor,TFT, array panel, comprising:

a substrate (110);
a plurality of pixel electrodes, each of the pixel electrodes including:

a transmissive electrode (192) formed in a transmissive region;
a first reflective electrode (194) in a reflective region and connected to the transmissive electrodes; and
a first conductor (170) electrically connected to at least one of the transmissive electrode and the first reflective electrode;
characterized in that it further comprises:

a second reflective electrode (196) in the reflective region and electrically separated from the transmissive electrode and the first reflective electrode; and
a second conductor (120) electrically connected to the second reflective electrode,
such that the first conductor (170) overlaps at least one of the second reflective electrode (196) and the second conductor (120) so as to form a capacitative coupling.

2. The TFT array panel of any preceding claim, further comprising a first insulating layer (140) interposed between the first conductor (170) and the second conductor (120).

3. The TFT array panel of claim 2, further comprising a second insulating layer (801) interposed between the first and second reflective electrodes (194, 196) and the first conductor (170).

4. The TFT array panel of claim 3, further comprising a switching element having the first conductor (170) as output element, wherein the first reflective electrode (194) is connected to the first conductor (170).

5. The TFT array panel of claim 4, wherein the first and second insulating layers (140, 801) have a first contact hole (184) exposing the second conductor (120) and the second insulating layer (801) has a second contact hole (183) exposing the first conductor (170), wherein the second reflective electrode.(196) is connected to the second conductor (120) through the first contact hole (184) and the first reflective electrode (194) is connected to the first conductor (170) through the second contact hole (183).

6. A thin film transistor array panel according to claim 1 further comprising:

a gate line (121) formed on the substrate;

a first insulating layer (140) formed on the gate line;
a semiconductor layer (151) formed on the first insulating layer (140);
a data line (171) having at least a portion formed on the semiconductor layer;
a drain electrode (175) having at least a portion formed on the semiconductor layer (151) and electrically separated from the data line (171); and
a second insulating layer (180) formed on the data line and the drain electrode and having a first contact hole (185) exposing the drain electrode (175);
wherein the transmissive electrode (192) is formed on the second insulating layer (180) and electrically connected to the drain electrode (175) through the first contact hole (185);
the first conductor (170) is a first auxiliary electrode (127) and the second conductor (120) is a second auxiliary electrode (126).

7. The TFT array panel of claim 6, wherein the second auxiliary electrode (120) is disposed under the first insulating layer (140).

8. The TFT array panel of claim 7, wherein the first and second insulating layers (140, 180) have a second contact hole (186) exposing the second auxiliary electrode (126), and the second reflective electrode is connected to the auxiliary electrode through the second contact hole.

9. The TFT array panel of claim 8, wherein the drain electrode (175) has an opening and the second contact hole is formed through the opening.

10. The TFT array panel of claim 8, wherein the first auxiliary electrode (127) is interposed between the first insulating layer and the second insulating layer

11. The TFT array panel of claim 10, wherein the first auxiliary electrode (127) has an opening and the second contact hole is formed through the opening.

12. The TFT array panel of any of claims 6 to 11, wherein the second insulating layer comprises a passivation layer (180) and an organic insulating layer (187) formed on the passivation layer,

13. The TFT array panel of claim 12, wherein the organic insulating layer (187) has an embossed surface.

14. The TFT array panel of any of claims 6 to 13, wherein the first reflective electrode (194) is disposed on the transmissive electrode (192).

15. The TFT array panel of any of claims 6 to 14, wherein the second reflective electrode (196) comprises a transmissive conductor and a reflective conductor formed on the transmissive conductor.

16. The TFT array panel of claim 6, further comprising a storage electrode (133) overlapping the drain electrode.

17. A thin film transistor, TFT, array panel, comprising:

a substrate (110);
a plurality of pixel electrodes, each of the pixel electrodes including:

a transmissive electrode (192) formed in a transmissive region;
a first reflective electrode (194) in a reflective region and connected to the transmissive electrode; and
a first conductor (170) electrically connected to at least one of the transmissive electrode and the first reflective electrode;
characterized in that it further comprises:

a second reflective electrode (196) in the reflective region and electrically separated from the transmissive electrode and the first reflective electrode;
such that at least one of the transmissive electrode (192), and the first conductor (170) overlaps the second reflective electrode (196) for obtaining a capacitative coupling.

18. The TFT array panel of claim 17, further comprising an insulating layer (802) interposed between the transmissive

electrode (192) and the second reflective electrode (196).

19. The TFT array panel of claim 18, further comprising a switching element having the first conductor as an output electrode (170) connected to the transmissive electrode (192).

20. The TFT array panel of any preceding claim, further comprising a first insulating layer (801) interposed between the first conductor (170) and the second conductor (120).

21. The TFT array panel of any preceding claim, further comprising an insulating layer (801) interposed between the first conductor and the second reflective electrode.

22. The TFT array panel of claim 8, further comprising a switching element having the first conductor as an output electrode (170) connected to the first conductor (170), wherein the first reflective electrode (194) is connected to the first conductor (170).

Patentansprüche

1. Dünnschichttransistor(TFT)-Matrixpanel, umfassend:

ein Substrat (110),
eine Mehrzahl von Pixelelektroden, wobei jede der Pixelelektroden beinhaltet:

eine Transmissionselektrode (192), die in einem Transmissionsbereich gebildet ist,
eine erste Reflexionselektrode (194) in einem Reflexionsbereich, die mit der Transmissionselektrode verbunden ist, und
einen ersten Leiter (170), der mit der Transmissionselektrode und/oder der ersten Reflexionselektrode elektrisch verbunden ist,
dadurch gekennzeichnet, dass sie ferner umfasst:

eine zweite Reflexionselektrode (196) im Reflexionsbereich, die von der Transmissionselektrode und der ersten Reflexionselektrode elektrisch getrennt ist, und
einen zweiten Leiter (120), der mit der zweiten Reflexionselektrode elektrisch verbunden ist,
so dass der erste Leiter (170) die zweite Reflexionselektrode (196) und/oder den zweiten Leiter (120) überlappt, um eine kapazitive Kopplung zu bilden.

2. TFT-Matrixpanel nach einem der vorhergehenden Ansprüche, ferner umfassend eine erste Isolierschicht (140), die zwischen den ersten Leiter (170) und den zweiten Leiter (120) eingesetzt ist.

3. TFT-Matrixpanel nach Anspruch 2, ferner umfassend eine zweite Isolierschicht (801), die zwischen die erste und zweite Reflexionselektrode (194, 196) und den ersten Leiter (170) eingesetzt ist.

4. TFT-Matrixpanel nach Anspruch 3, ferner umfassend ein Schaltelement mit dem ersten Leiter (170) als Ausgabeelement, wobei die erste Reflexionselektrode (194) mit dem ersten Leiter (170) verbunden ist.

5. TFT-Matrixpanel nach Anspruch 4, wobei die erste und zweite Isolierschicht (140, 801) ein erstes Kontaktloch (184) aufweisen, das den zweiten Leiter (120) freilegt, und die zweite Isolierschicht (801) ein zweites Kontaktloch (183) aufweist, das den ersten Leiter (170) freilegt, wobei die zweite Reflexionselektrode (196) mit dem zweiten Leiter (120) durch das erste Kontaktloch (184) verbunden ist und die erste Reflexionselektrode (194) mit dem ersten Leiter (170) durch das zweite Kontaktloch (183) verbunden ist.

6. Dünnschichttransistor-Matrixpanel nach Anspruch 1, ferner umfassend:

eine auf dem Substrat gebildete Gateleitung (121),
eine auf der Gateleitung gebildete erste Isolierschicht (140),
eine auf der ersten Isolierschicht (140) gebildete Halbleiterschicht (151),
eine Datenleitung (171), die mindestens einen auf der Halbleiterschicht gebildeten Abschnitt aufweist,
eine Drainelektrode (175), von der mindestens ein Teil auf der Halbleiterschicht gebildet ist und die von der

Datenleitung (171) elektrisch getrennt ist, und
eine auf der Datenleitung und der Drainelektrode gebildete zweite Isolierschicht (180), die ein erstes Kontaktloch (185) aufweist, das die Drainelektrode (175) freilegt,
wobei die Transmissionselektrode (192) auf der zweiten Isolierschicht (180) gebildet und durch das erste Kontaktloch (185) mit der Drainelektrode (115) elektrisch verbunden ist,
der erste Leiter (170) eine erste Hilfselektrode (127) ist und der zweite Leiter (120) eine zweite Hilfselektrode (126) ist.

7. TFT-Matrixpanel nach Anspruch 6, wobei die zweite Hilfselektrode (120) unter der ersten Isolierschicht (140) angeordnet ist.

8. TFT-Matrixpanel nach Anspruch 7, wobei die erste und zweite Isolierschicht (140, 180) ein zweites Kontaktloch (186) aufweisen, das die zweite Hilfselektrode (126) freilegt, und die zweite Reflexionselektrode mit der Hilfselektrode durch das zweite Kontaktloch verbunden ist.

9. TFT-Matrixpanel nach Anspruch 8, wobei die Drainelektrode (175) eine Öffnung aufweist und das zweite Kontaktloch durch die Öffnung gebildet ist.

10. TFT-Matrixpanel nach Anspruch 8, wobei die erste Hilfselektrode (127) zwischen die erste Isolierschicht und die zweite Isolierschicht eingesetzt ist.

11. TFT-Matrixpanel nach Anspruch 10, wobei die erste Hilfselektrode (127) eine Öffnung aufweist und das zweite Kontaktloch durch die Öffnung gebildet ist.

12. TFT-Matrixpanel nach einem der Ansprüche 6 bis 11, wobei die zweite Isolierschicht eine Passivierungsschicht (180) und eine auf der Passivierungsschicht gebildete organische Isolierschicht (187) umfasst.

13. TFT-Matrixpanel nach Anspruch 12, wobei die organische Isolierschicht (187) eine erhabene Oberfläche aufweist.

14. TFT-Matrixpanel nach einem der Ansprüche 6 bis 13, wobei die erste Reflexionselektrode (194) auf der Transmissionselektrode (192) angeordnet ist.

15. TFT-Matrixpanel nach einem der Ansprüche 6 bis 14, wobei die zweite Reflexionselektrode (196) einen Transmissionsleiter und einen auf dem Transmissionsleiter gebildeten Reflexionsleiter umfasst.

16. TFT-Matrixpanel nach Anspruch 6, ferner umfassend eine Speicherelektrode (133), die die Drainelektrode überlappt.

17. Dünnschichttransistor(TFT)-Matrixpanel, umfassend:

ein Substrat (110),
eine Mehrzahl von Pixelelektroden, wobei jede der Pixelelektroden beinhaltet:

eine Transmissionselektrode (192), die in einem Transmissionsbereich gebildet ist,
eine erste Reflexionselektrode (194) in einem Reflexionsbereich, die mit der Transmissionselektrode verbunden ist, und
einen ersten Leiter (170), der mit der Transmissionselektrode und/oder der ersten Reflexionselektrode elektrisch verbunden ist,
dadurch gekennzeichnet, dass sie ferner umfasst:

eine zweite Reflexionselektrode (196) im Reflexionsbereich, die von der Transmissionselektrode und der ersten Reflexionselektrode elektrisch getrennt ist,
so dass die Transmissionselektrode (192) und/oder der erste Leiter (170) die zweite Reflexionselektrode (196) zum Ausbilden einer kapazitiven Kopplung überlappt.

18. TFT-Matrixpanel nach Anspruch 17, ferner umfassend eine Isolierschicht (802), die zwischen die Transmissionselektrode (192) und die zweite Reflexionselektrode (196) eingesetzt ist.

19. TFT-Matrixpanel nach Anspruch 18, ferner umfassend ein Schaltelement mit dem ersten Leiter als Ausgabeelektrode

(170), das mit der Transmissionselektrode (192) verbunden ist.

20. TFT-Matrixpanel nach einem der vorhergehenden Ansprüche, ferner umfassend eine erste Isolierschicht (801), die zwischen den ersten Leiter (170) und den zweiten Leiter (120) eingesetzt ist.

21. TFT-Matrixpanel nach einem der vorhergehenden Ansprüche, ferner umfassend eine Isolierschicht (801), die zwischen den ersten Leiter und die zweite Reflexionselektrode eingesetzt ist.

22. TFT-Matrixpanel nach Anspruch 8, ferner umfassend ein Schaltelement mit dem ersten Leiter als Ausgabeelektrode (170), das mit dem ersten Leiter (170) verbunden ist, wobei die erste Reflexionselektrode (194) mit dem ersten Leiter (170) verbunden ist.

Revendications

1. Panneau de matrice de transistors à couches minces, TFT, comprenant :

un substrat (110) ;
une pluralité d'électrodes de pixel, chacune des électrodes de pixel comprenant :

une électrode de transmission (192) formée dans une région de transmission ;
une première électrode de réflexion (194) dans une région de réflexion et connectée à l'électrode de transmission ; et
un premier conducteur (170) connecté électriquement à au moins l'une de l'électrode de transmission et de la première électrode de réflexion ;
caractérisé en ce qu'il comprend en outre :

une deuxième électrode de réflexion (196) dans la région de réflexion et séparée électriquement de l'électrode de transmission et de la première électrode de réflexion ; et
un deuxième conducteur (120) connecté électriquement à la deuxième électrode de réflexion,
de sorte que le premier conducteur (170) recouvre au moins l'un de la deuxième électrode de réflexion (196) et du deuxième conducteur (120) de manière à former un couplage capacitif.

2. Panneau de matrice de TFT selon l'une quelconque des revendications précédentes, comprenant en outre une première couche isolante (140) interposée entre le premier conducteur (170) et le deuxième conducteur (120).

3. Panneau de matrice de TFT selon la revendication 2, comprenant en outre une deuxième couche isolante (801) interposée entre les première et deuxième électrodes de réflexion (194, 196) et le premier conducteur (170).

4. Panneau de matrice de TFT selon la revendication 3, comprenant en outre un élément de commutation comportant le premier conducteur (170) en tant qu'élément de sortie, dans lequel la première électrode de réflexion (194) est connectée au premier conducteur (170).

5. Panneau de matrice de TFT selon la revendication 4, dans lequel les première et deuxième couches isolantes (140, 801) comportent un premier trou de contact (184) exposant le deuxième conducteur (120) et la deuxième couche isolante (801) comporte un deuxième trou de contact (183) exposant le premier conducteur (170), dans lequel la deuxième électrode de réflexion (196) est connectée au deuxième conducteur (120) à travers le premier trou de contact (184) et la première électrode de réflexion (194) est connectée au premier conducteur (170) à travers le deuxième trou de contact (183).

6. Panneau de matrice de transistors à couche mince selon la revendication 1, comprenant en outre :

une ligne de grille (121) formée sur le substrat ;
une première couche isolante (140) formée sur la ligne de grille ;
une couche semi-conductrice (151) formée sur la première couche isolante (140) ;
une ligne de données (171) ayant au moins une partie formée sur la couche semi-conductrice ;
une électrode de drain (175) ayant au moins une partie formée sur la couche semi-conductrice (151) et séparée électriquement de la ligne de données (171) ; et

une deuxième couche isolante (180) formée sur la ligne de données et l'électrode de drain et comportant un premier trou de contact (185) exposant l'électrode de drain (175) ;
dans lequel l'électrode de transmission (192) est formée sur la deuxième couche isolante (180) et connectée électriquement à l'électrode de drain (175) à travers le premier trou de contact (185) ;
le premier conducteur (170) est une première électrode auxiliaire (127) et le deuxième conducteur (120) est une deuxième électrode auxiliaire (126).

7. Panneau de matrice de TFT selon la revendication 6, dans lequel la deuxième électrode auxiliaire (120) est disposée sous la première couche isolante (140).

8. Panneau de matrice de TFT selon la revendication 7, dans lequel les première et deuxième couches isolantes (140, 180) comportent un deuxième trou de contact (186) exposant la deuxième électrode auxiliaire (126), est la deuxième électrode de réflexion est connectée à l'électrode auxiliaire à travers le deuxième trou de contact.

9. Panneau de matrice de TFT selon la revendication 8, dans lequel l'électrode de drain (175) comporte une ouverture et le deuxième trou de contact est formé à travers l'ouverture.

10. Panneau de matrice de TFT selon la revendication 8, dans lequel la première électrode auxiliaire (127) est interposée entre la première couche isolante et la deuxième couche isolante.

11. Panneau de matrice de TFT selon la revendication 10, dans lequel la première électrode auxiliaire (127) comporte une ouverture et le deuxième trou de contact est formé à travers l'ouverture.

12. Panneau de matrice de TFT selon l'une quelconque des revendications 6 à 11, dans lequel la deuxième couche isolante comprend une couche de passivation (180) et une couche isolante organique (187) formée sur la couche de passivation.

13. Panneau de matrice de TFT selon la revendication 12, dans lequel la couche isolante organique (187) a une surface bosselée.

14. Panneau de matrice de TFT selon l'une quelconque des revendications 6 à 13, dans lequel la première électrode de réflexion (194) est disposée sur l'électrode de transmission (192).

15. Panneau de matrice de TFT selon l'une quelconque de revendications 6 à 14, dans lequel la deuxième électrode de réflexion (196) comprend un conducteur de transmission et un conducteur de réflexion formé sur le conducteur de transmission.

16. Panneau de matrice de TFT selon la revendication 6, comprenant en outre une électrode de stockage (133) recouvrant l'électrode de drain.

17. Panneau de matrice de transistors à couches minces, TFT, comprenant :

un substrat (110) ;
une pluralité d'électrodes de pixel, chacune des électrodes de pixel comprenant :

une électrode de transmission (192) formée dans une région de transmission ;
une première électrode de réflexion (194) dans une région de réflexion et connectée à l'électrode de transmission ; et
un premier conducteur (170) connecté électriquement à au moins l'une de l'électrode de transmission et de la première électrode de réflexion ;
caractérisé en ce qu'il comprend en outre :

une deuxième électrode de réflexion (196) dans la région de réflexion et séparée électriquement de l'électrode de transmission et de la première électrode de réflexion ;
de sorte qu'au moins l'un de l'électrode de transmission (192) et du premier conducteur (170) recouvre la deuxième électrode de réflexion (196) pour obtenir un couplage capacitif.

18. Panneau de matrice de TFT selon la revendication 17, comprenant en outre une couche isolante (802) interposée

entre l'électrode de transmission (192) et la deuxième électrode de réflexion (196).

19. Panneau de matrice de TFT selon la revendication 18, comprenant en outre un élément de commutation comportant le premier conducteur en tant qu'électrode de sortie (170) connecté à l'électrode de transmission (192).

20. Panneau de matrice de TFT selon l'une quelconque des revendications précédentes, comprenant en outre une première couche isolante (801) interposée entre le premier conducteur (170) et le deuxième conducteur (120).

21. Panneau de matrice de TFT selon l'une quelconque des revendications précédentes, comprenant en outre une couche isolante (801) interposée entre le premier conducteur et la deuxième électrode de réflexion.

22. Panneau de matrice de TFT selon la revendication 8, comprenant en outre un élément de commutation comportant le premier conducteur en tant qu'électrode de sortie (170) connecté au premier conducteur (170), dans lequel la première électrode de réflexion (194) est connectée au premier conducteur (170).

FIG. 1

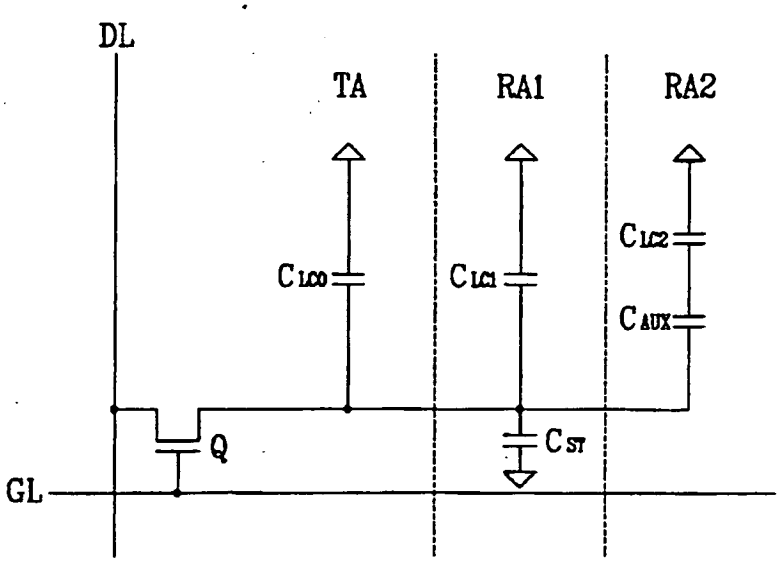


FIG. 2

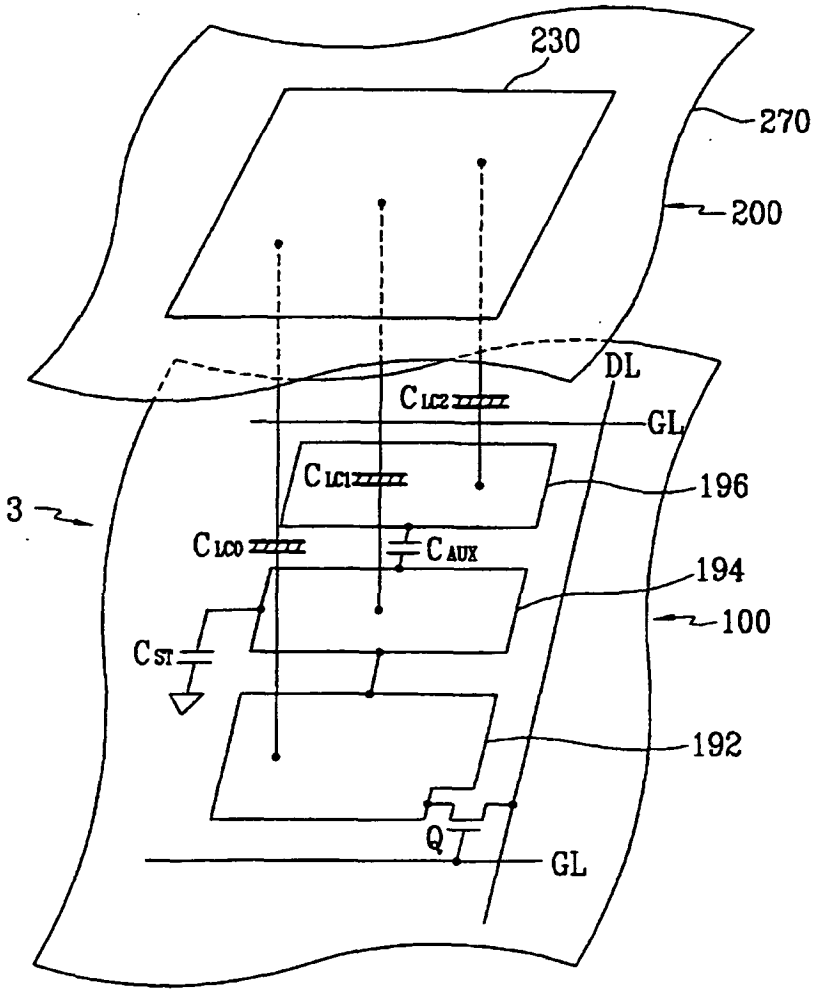


FIG. 3

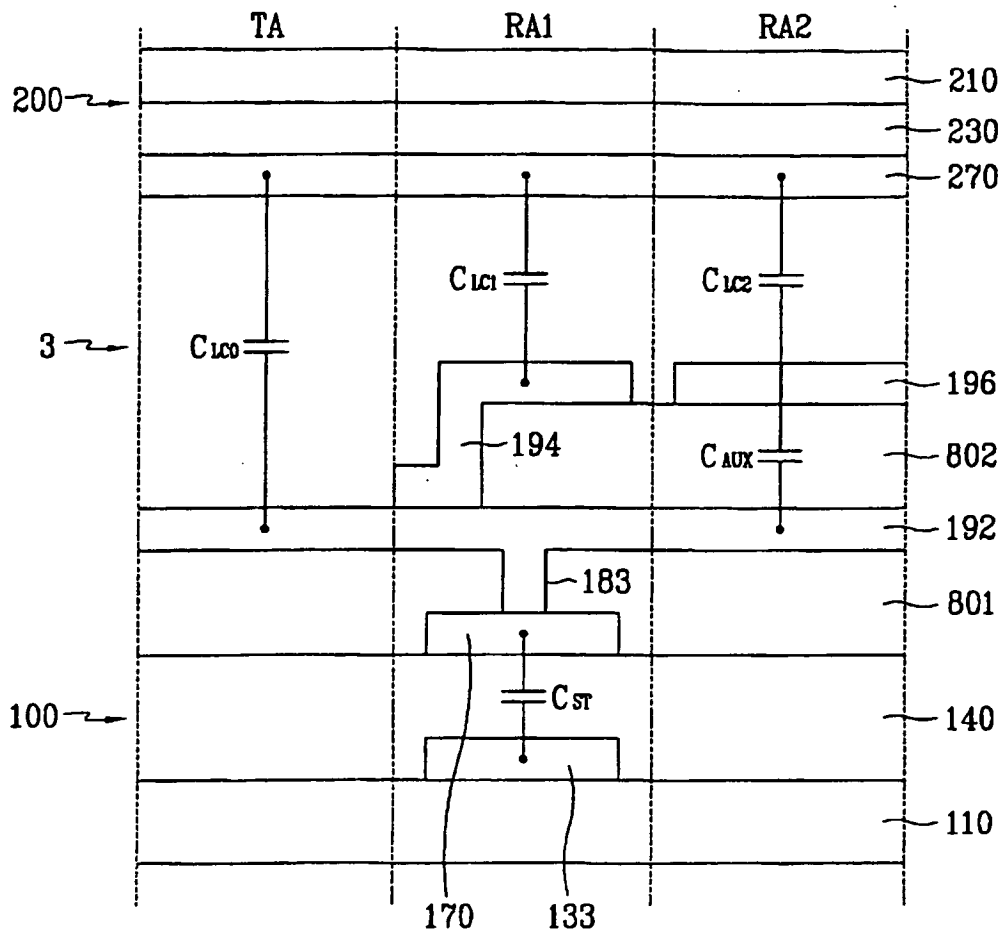

TA
RA1
RA2
200
210
230
270
3
C_{LC0}
C_{LC1}
C_{LC2}
196
194
C_{AUX}
802
192
183
801
100
C_{ST}
140
110
170
133

FIG. 4

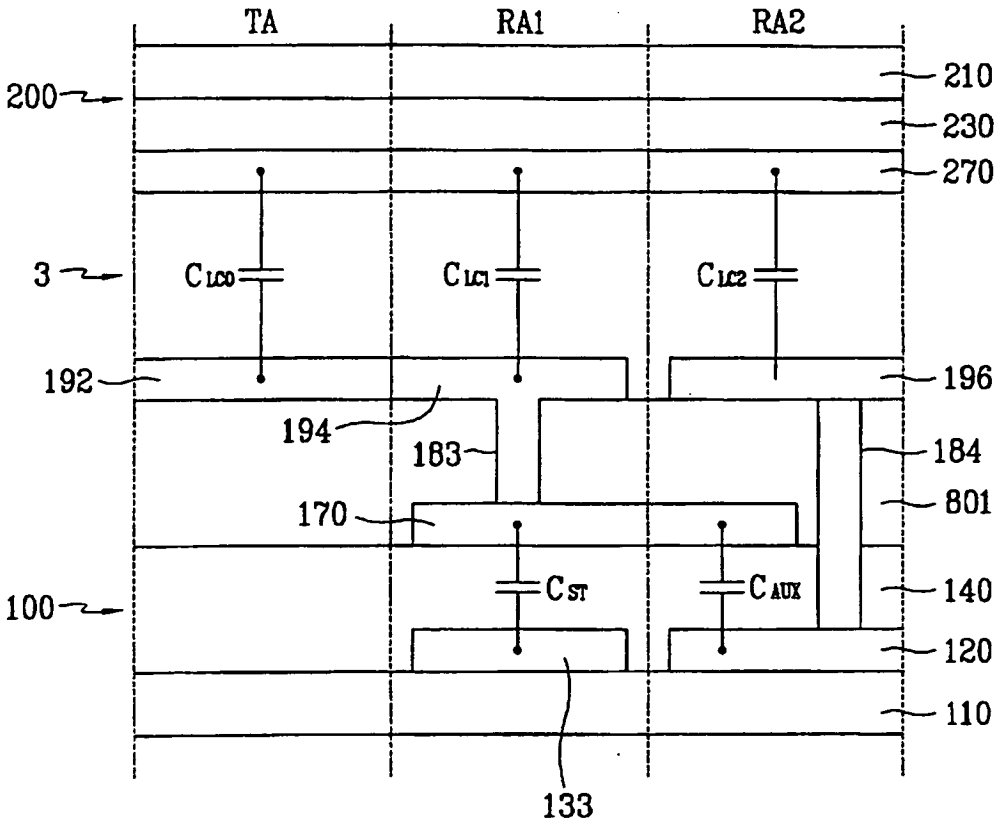

TA
RA1
RA2
200
210
230
270
3
C_{LC0}
C_{LC1}
C_{LC2}
192
196
194
183
184
170
801
C_{ST}
C_{AUX}
100
140
120
110
133

FIG. 5

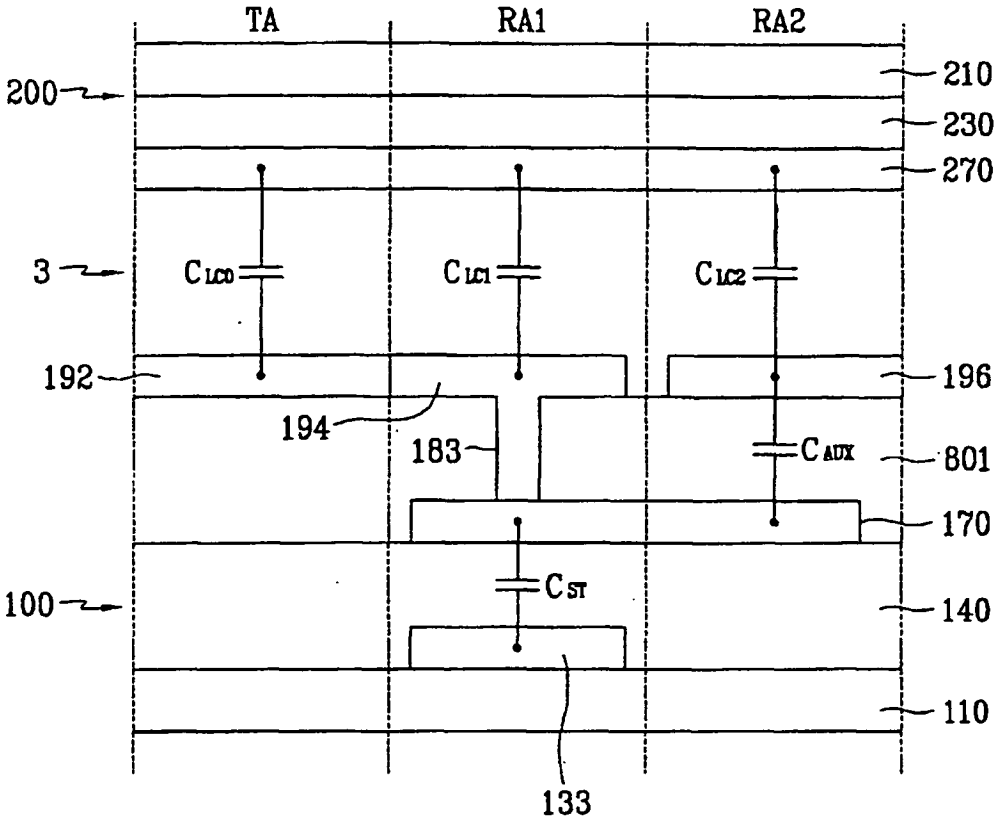

TA
RA1
RA2
200
210
230
270
3
C_{LC0}
C_{LC1}
C_{LC2}
192
196
194
183
C_{AUX}
801
170
C_{ST}
100
140
110
133

FIG. 6A

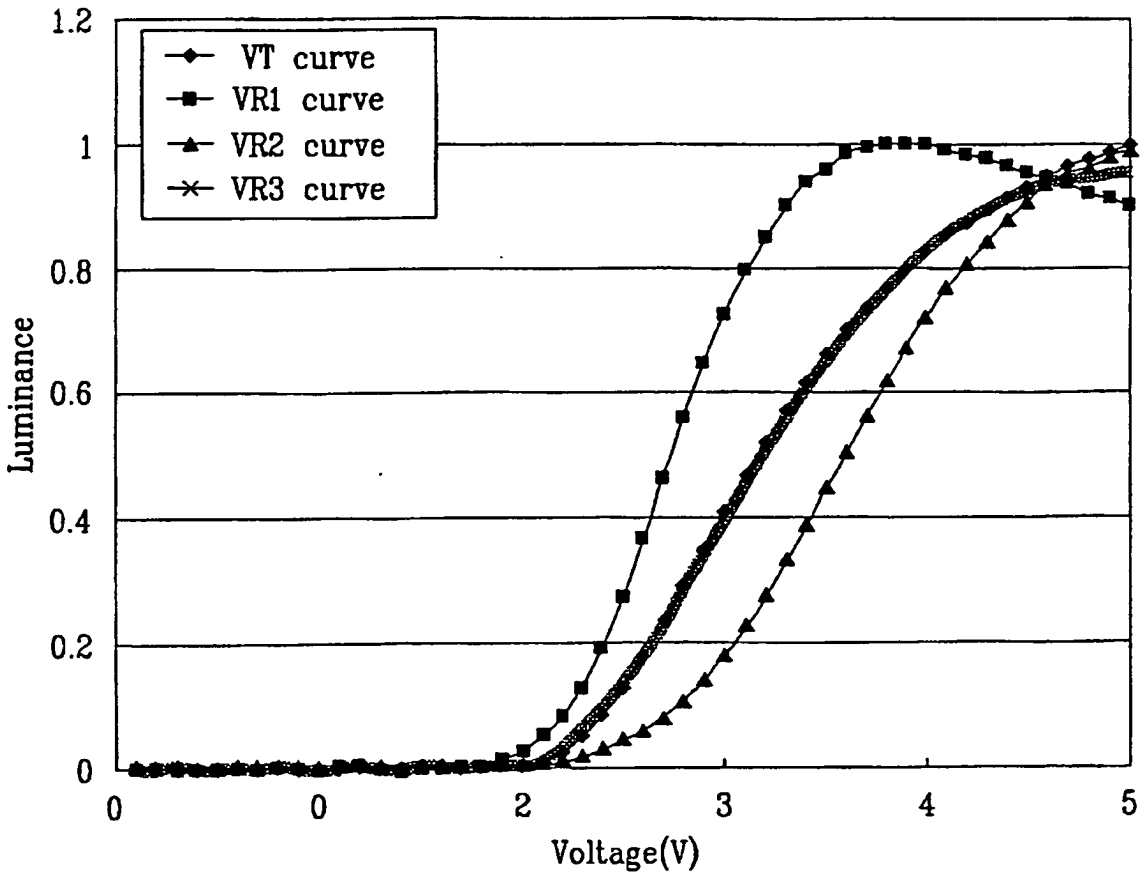

VT curve
VR1 curve
VR2 curve
VR3 curve
Luminance
1.2
1
0.8
0.6
0.4
0.2
0
0
0
2
3
4
5
Voltage(V)

FIG. 6B

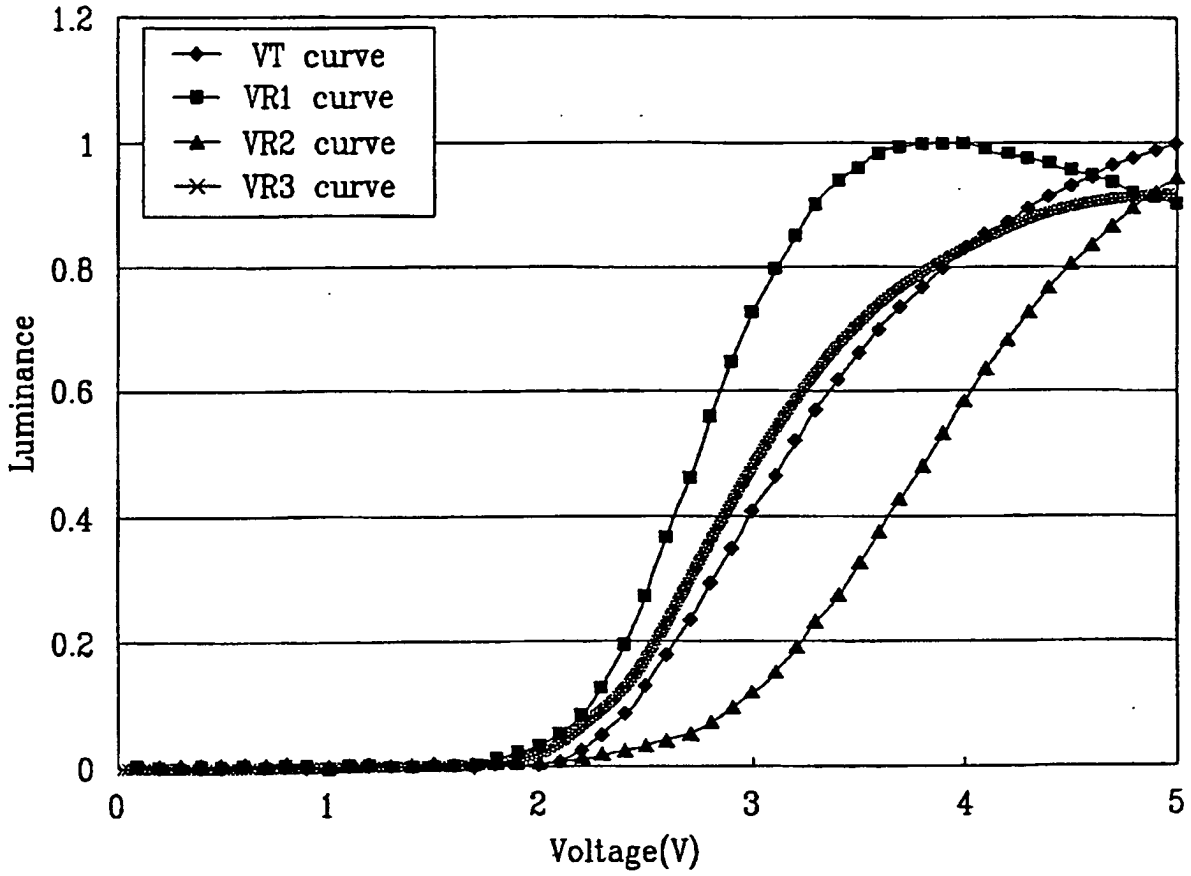

VT curve
VR1 curve
VR2 curve
VR3 curve
Luminance
1.2
1
0.8
0.6
0.4
0.2
0
0
1
2
3
4
5
Voltage(V)

FIG. 6C

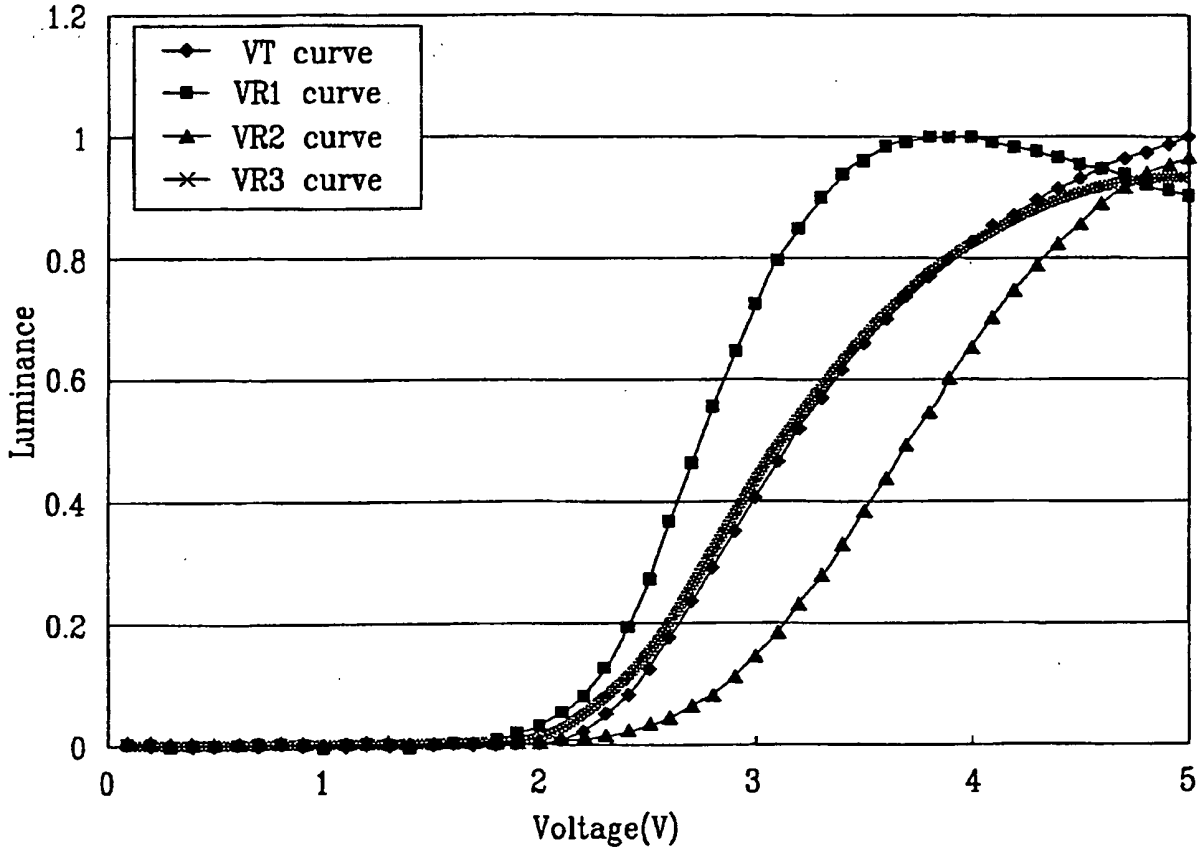

VT curve
VR1 curve
VR2 curve
VR3 curve
Luminance
1.2
1
0.8
0.6
0.4
0.2
0
0
1
2
3
4
5
Voltage(V)

FIG. 6D

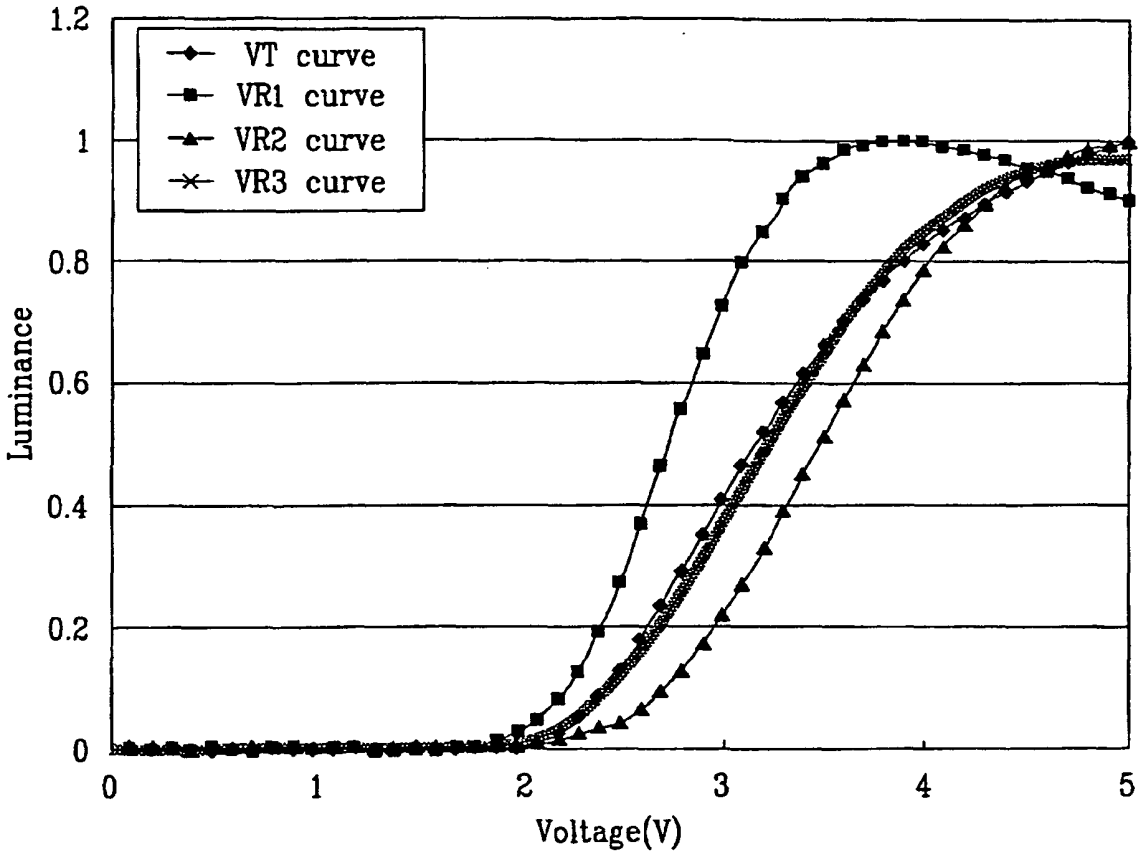

VT curve
VR1 curve
VR2 curve
VR3 curve
Luminance
Voltage(V)
1.2
1
0.8
0.6
0.4
0.2
0
0
1
2
3
4
5

FIG. 6E

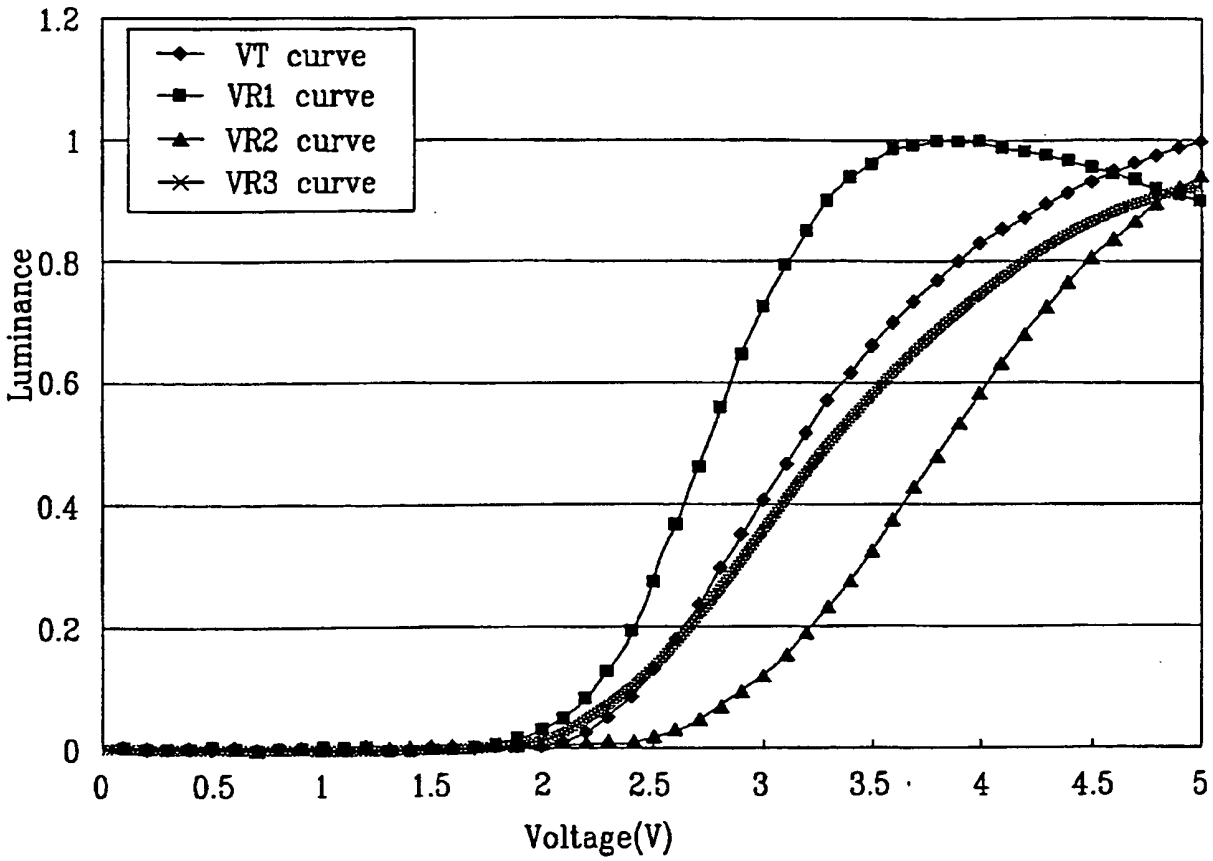

VT curve
VR1 curve
VR2 curve
VR3 curve
Luminance
1.2
1
0.8
0.6
0.4
0.2
0
0
0.5
1
1.5
2
2.5
3
3.5
4
4.5
5
Voltage(V)

FIG. 6F

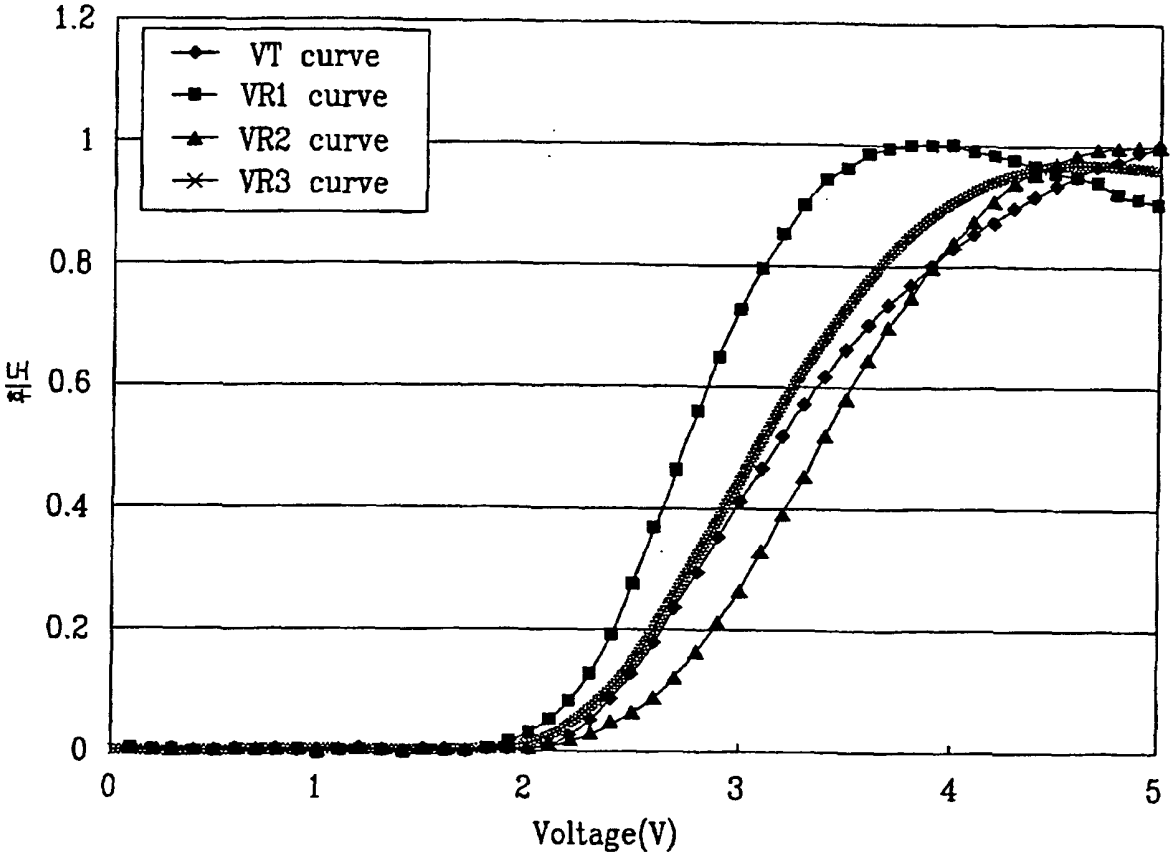

VT curve
VR1 curve
VR2 curve
VR3 curve
1.2
1
0.8
0.6
0.4
0.2
0
휘도
0
1
2
3
4
5
Voltage(V)

FIG. 7

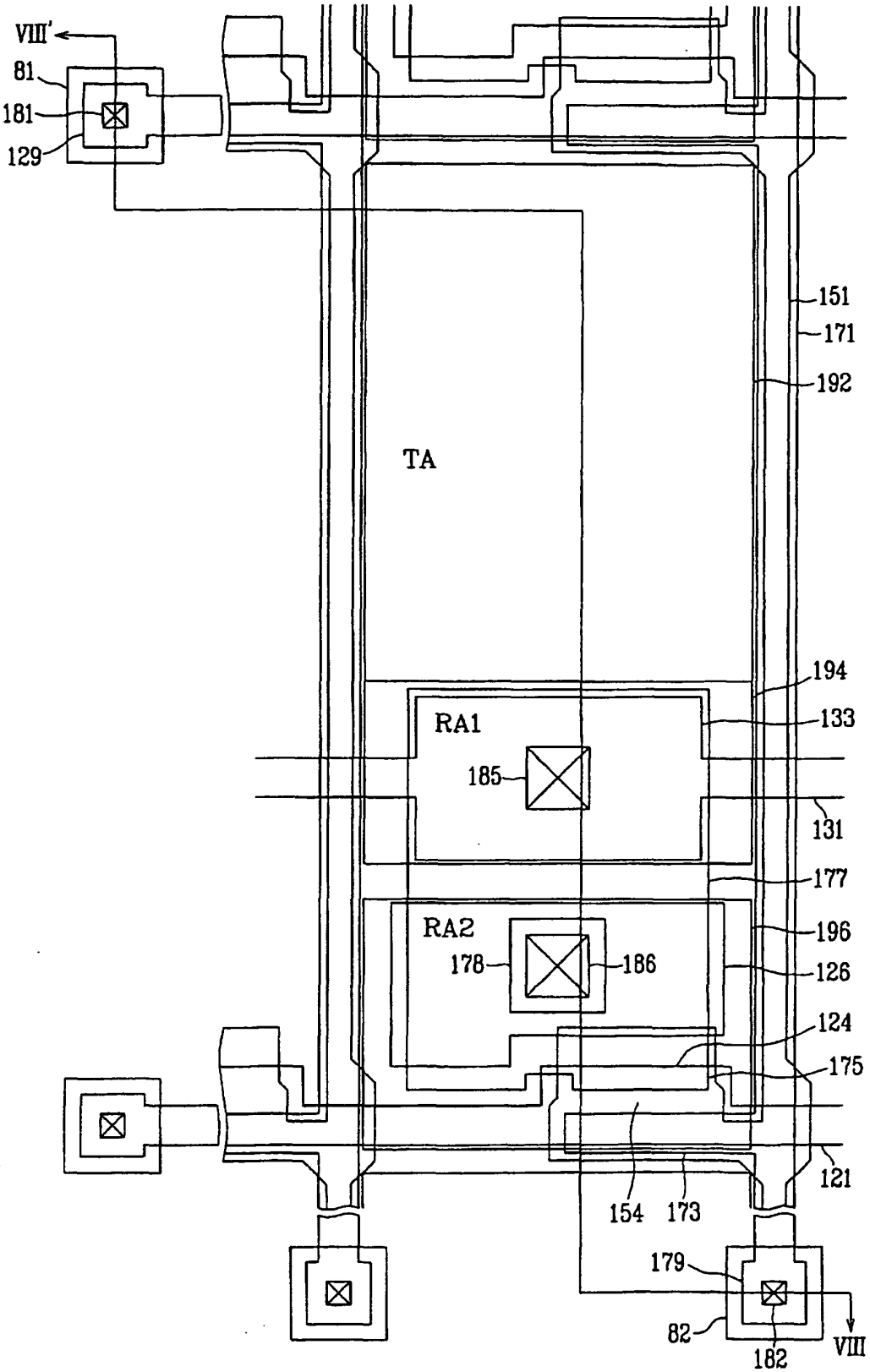

VIII'
81
181
129
151
171
192
TA
194
RA1
133
185
131
177
RA2
196
178
186
126
124
175
121
154
173
179
82
182
VIII

FIG. 8

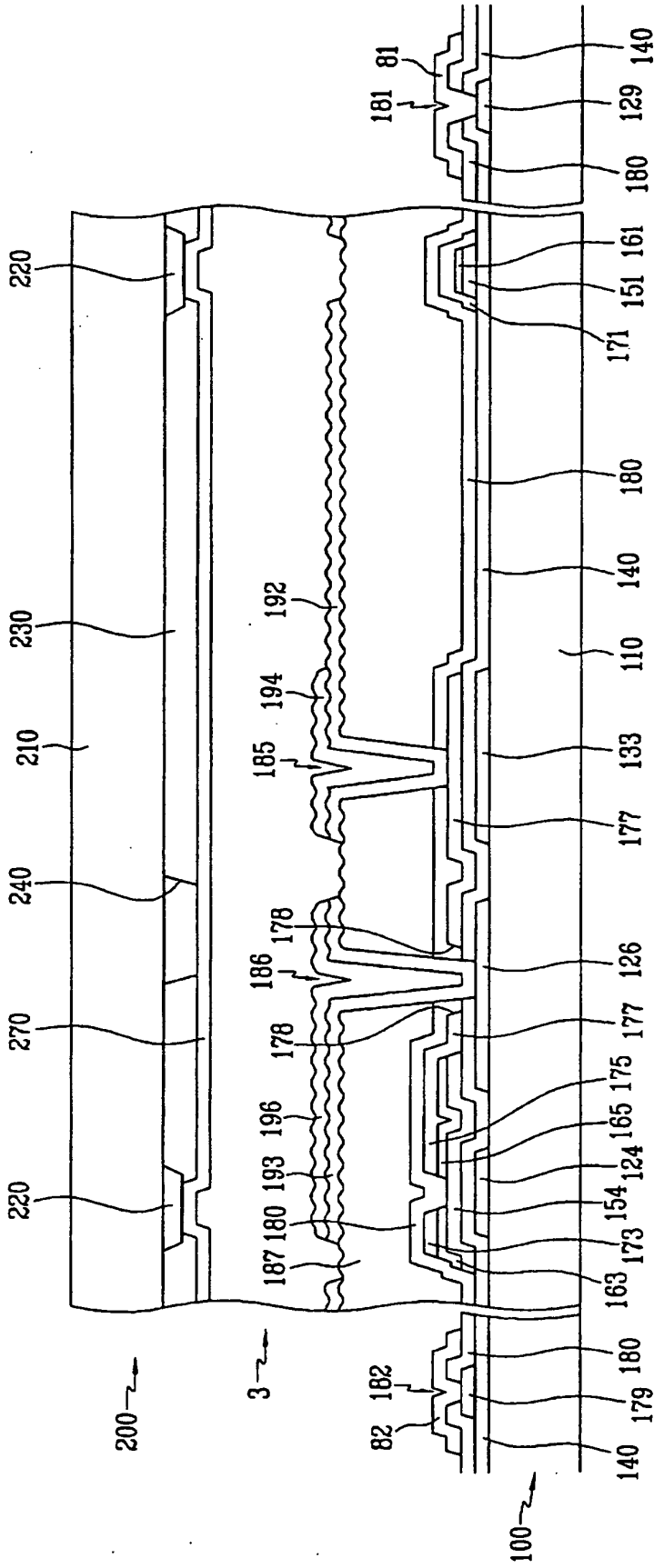

220
230
210
240
270
220
200
3
100
81
181
140
129
180
161
151
171
180
140
110
133
177
126
177
175
165
124
154
173
163
180
179
140
182
82
192
194
185
178
186
178
196
193
180
187

FIG. 9

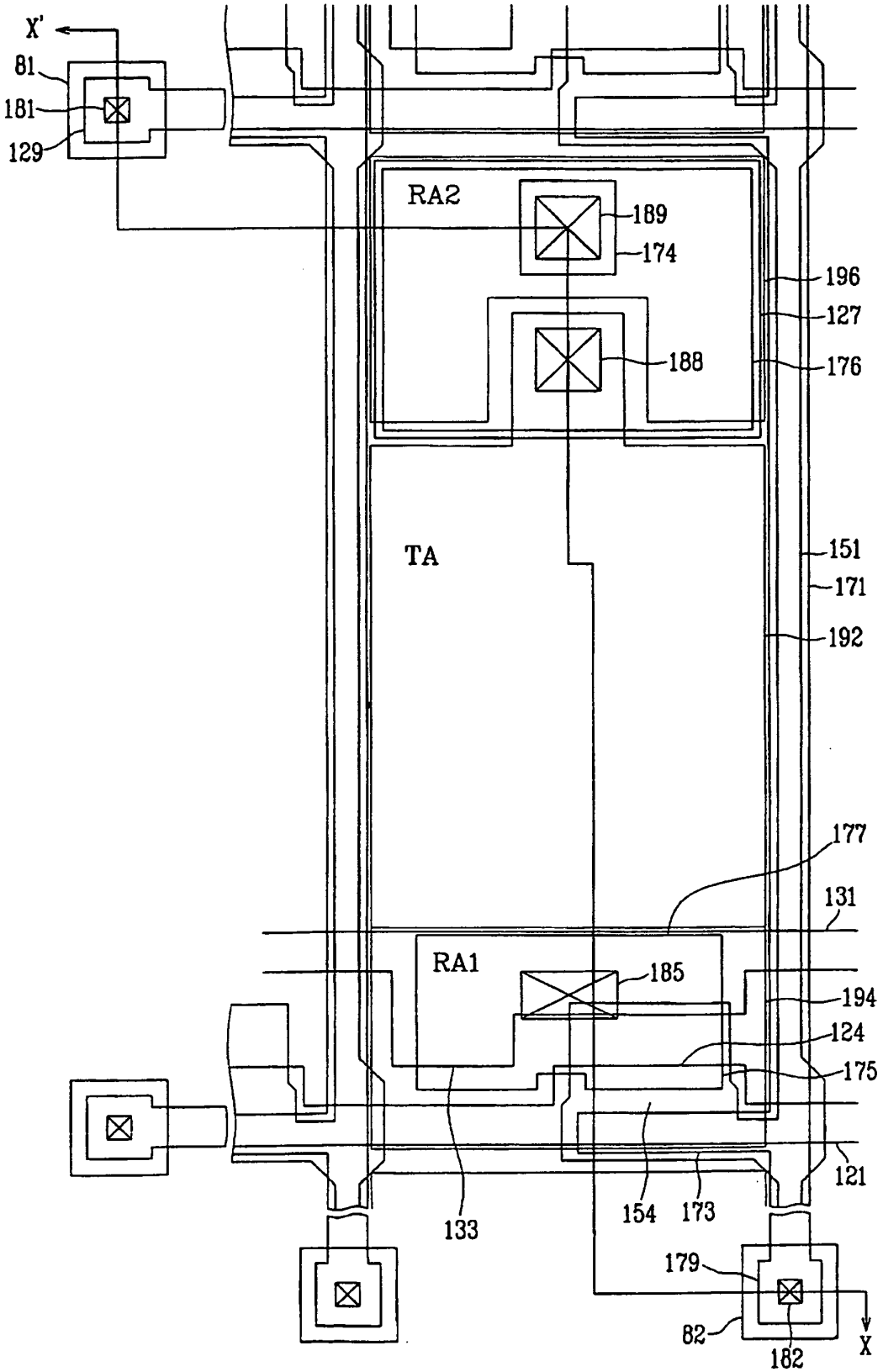
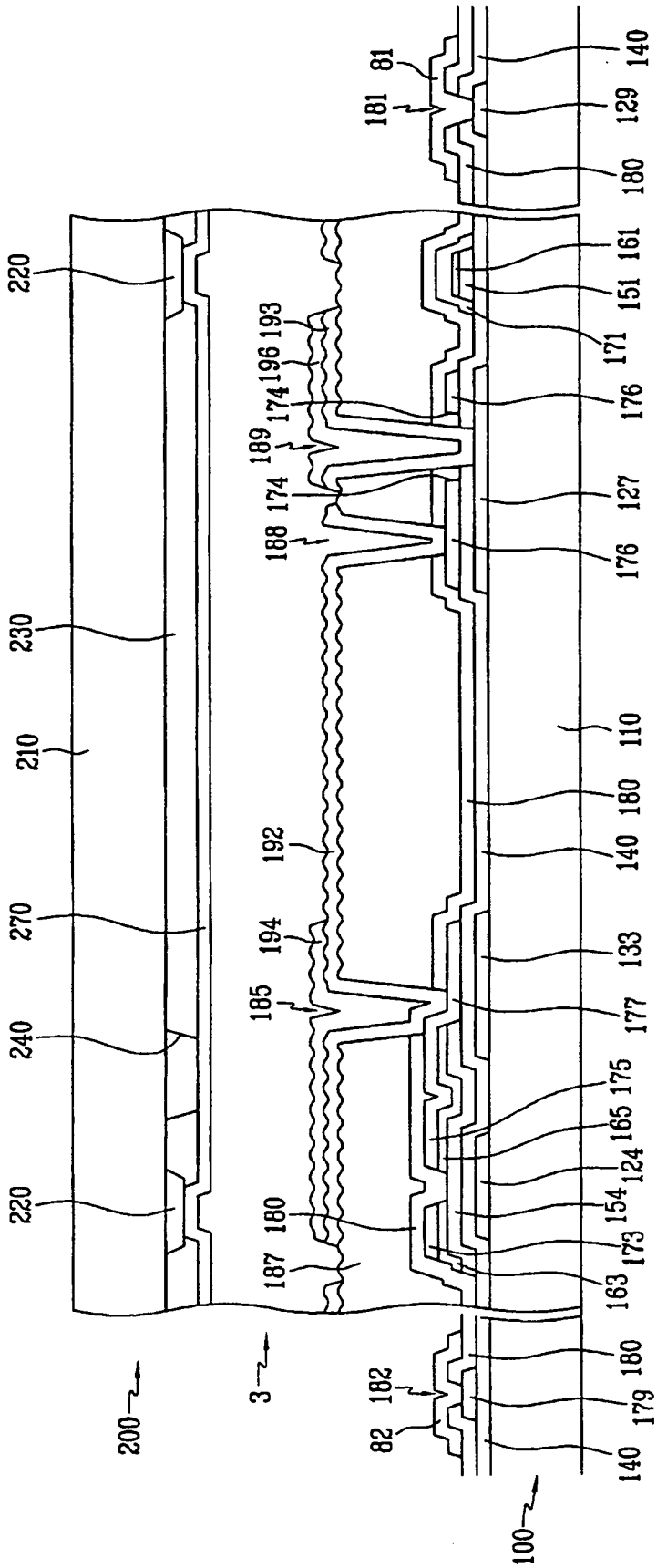

X'
81
181
129
RA2
189
174
196
127
188
176
TA
151
171
192
177
131
RA1
185
194
124
175
121
133
154
173
179
82
182
X

FIG. 10


220
230
210
270
240
220
200
3
100
81
181
140
129
180
161
151
171
193
196
174
176
189
174
127
188
176
110
180
140
192
194
133
185
177
175
165
124
154
180
187
173
163
182
180
82
179
140

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- WO 2004057411 A **[0007]**
- EP 562120 A **[0008]**

专利名称(译)	薄膜晶体管阵列面板和包括面板的液晶显示器		
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[标]申请(专利权)人(译)	三星电子株式会社		
申请(专利权)人(译)	SAMSUNG ELECTRONICS CO.，LTD.		
当前申请(专利权)人(译)	SAMSUNG ELECTRONICS CO.，LTD.		
[标]发明人	CHAI CHONG CHUL CHOI JEONG YE 203 1102 SANGHYEONMAEUL KWAG JIN OH KIM JIN HONG KIM SANG IL HONG MUN PYO ROH NAM SEOK YANG YOUNG CHOL		
发明人	CHAI, CHONG-CHUL CHOI, JEONG-YE 203-1102 SANGHYEONMAEUL KWAG, JIN-OH KIM, JIN-HONG KIM, SANG-IL HONG, MUN-PYO ROH, NAM-SEOK YANG, YOUNG-CHOL		
IPC分类号	G02F1/1335		
CPC分类号	G02F1/133555 G02F2001/134345 G02F2001/134354		
优先权	1020040108173 2004-12-17 KR		
其他公开文献	EP1672414A1		
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摘要(译)

本发明提供一种TFT阵列面板，其具有透射区域和反射区域。透射电极（192）设置在透射区域中。连接到透射电极的第一反射电极（194）设置在反射区域上。与透射电极和第一反射区域分离的第二反射电极（196）形成在反射区域中。第一导体连接到透射电极和第一反射电极中的至少一个。第二导体连接到第二反射电极。透射电极，第一反射电极和第一导体中的至少一个与第二反射电极和第二导体中的至少一个重叠，以形成辅助电容器（Caux）。

[Equation 1]

$$V2 = \frac{C_{AUX}}{(C_{AUX} + C_{LC2})} V$$