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(54) **Thin film transistor array panel for liquid crystal display device and manufacturing method thereof**

Tafel mit Dünnschichttransistormatrix für Flüssigkristallanzeigegerät und Herstellungsverfahren dafür

Panneau à réseau de transistors à couche mince pour un dispositif d'affichage à cristal liquide et procédé de fabrication correspondant

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Description

[0001] This application claims priority to Korean patent application no. 10-2004-0100915, filed on December 3, 2004.

BACKGROUND OF THE INVENTION

(a) Field of the Invention

[0002] The present invention relates to a thin film transistor array panel according to the preamble of claim 1, and to a method of manufacturing a thin film transistor array panel according to the preamble of claim 17.

(b) Description of Related Art

[0003] A thin film transistor array panel according to the preamble of claim 1 is known from US 5 576 858 A, which discloses a gray scale liquid crystal display panel. The liquid crystal display of US 5 576 858 A comprises a thin film transistor array panel with a gate line being disposed on a substrate. A capacitive electrode is separated from the gate line and data line intersects the gate lines. A thin film transistor includes a drain electrode and is connected to the gate line and the data line. A coupling electrode is connected to the drain electrode, overlapping the capacitive electrode. A pixel electrode consists of a first subpixel electrode and a second subpixel electrode. The first subpixel electrode is connected to the drain electrode and the second subpixel electrode is capacitively connected to the capacitive electrode.

[0004] Liquid crystal displays (LCDs) are among the most widely used flat panel displays. An LCD includes two panels provided with field-generating electrodes, such as pixel electrodes and a common electrode, and a liquid crystal (LC) layer interposed therebetween. The LCD displays an image by applying voltages to the field-generating electrodes to generate an electric field in the LC layer, which controls an orientation of LC molecules in the LC layer to adjust polarization of incident light.

[0005] Among the different types of LCDs, a vertical alignment (VA) mode LCD achieves a high contrast ratio and wide reference-viewing angle. The VA mode LCD aligns (e.g., tilts) LC molecules such that the long axes of the LC molecules are perpendicular to the panels in the absence of an electric field.

[0006] The reference-viewing angle of the VA mode LCD depends upon the arrangement of cutouts in the field-generating electrodes and protrusions on the field-generating electrodes. The cutouts and the protrusions can determine the tilt of the LC molecules. The reference-viewing angle can be widened by appropriately arranging cutouts and protrusions to vary the tilt of the LC molecules.

[0007] In the VA mode LCD, poor lateral visibility can be a problem. The pixel electrodes of the VA mode LCD overlap signal lines for transmitting signals to the pixel electrodes for increasing the aperture ratio and a thick, low dielectric insulator is disposed between the pixel electrodes and the signal line for reducing parasitic capacitance between the pixel electrodes and the signal lines.

[0008] The thick insulator causes deep contact holes for connecting the signal lines and the pixel electrodes, etc., and thus sidewall profiles of the contact holes need to be smoothed. The smooth sidewalls of the contact holes cause light leakage, thereby degrading image quality. Although the light leakage may be substantially blocked by widening opaque members in the LCD, widened opaque members may decrease the aperture ratio.

[0009] Therefore, a need exists for a thin film transistor array panel for improving the lateral visibility in LCDs.

SUMMARY OF THE INVENTION

[0010] The thin film transistor array panel according to the Invention is defined in claim 1. Advantageous embodiments thereof are defined in dependent claims 2 to 16. Accordingly, the through-hole may be substantially equidistant from two opposite edges of the capacitive electrode, and may be rectangular, octagonal, or circular.

[0011] The contact hole may have a stepped sidewall.

[0012] A distance between an edge of the contact hole and the through-hole may be equal to or greater than about 3.0 microns.

[0013] The thin film transistor array panel may further include a shielding electrode separated from the pixel electrode and overlapping a portion of the data line or the gate line. The pixel electrode and the shielding electrode may be disposed on the passivation layer.

[0014] The thin film transistor array panel may further include a storage electrode overlapping the drain electrode. The shielding electrode and the storage electrode may be supplied with substantially the same voltage. The shielding electrode may extend along the data line or the gate lines, and it may fully cover the data line.

[0015] The pixel electrode may have a chamfered corner.

[0016] The passivation layer may include an organic insulator.

[0017] The thin film transistor array panel may further include a color filter disposed on or under the passivation layer.

[0018] The pixel electrode may include a partitioning member for partitioning the pixel electrode into a plurality of partitions. The partitioning member may make an angle of about 45 degrees with the gate line.

[0019] The method of manufacturing a thin film transistor array according to the invention is defined in claim 17. Advantageous embodiments thereof are defined in dependent claims 2 to 16. Accordingly, the through-hole may be rectangular, octagonal, or circular and substantially equidistant from two opposite edges of the capacitive electrode.

[0020] The contact hole may have a stepped sidewall.

BRIEF DESCRIPTION OF THE DRAWINGS

[0021] The present invention will become more apparent by describing embodiments thereof in detail with reference to the accompanying drawings in which:

Fig. 1 is a layout view of a TFT array panel of an LCD according to an embodiment of the present invention;
Fig. 2 is a layout view of a common electrode panel of an LCD according to an embodiment of the present invention;
Fig. 3 is a layout view of an LCD including the TFT array panel shown in Fig. 1 and the common electrode panel shown in Fig. 2;
Fig. 4 is a sectional view of the LCD shown in Fig. 3 taken along line IV-IV';
Fig. 5 is an equivalent circuit diagram of the LCD shown in Figs. 1-4;
Fig. 6 is a layout view of an LCD according to another embodiment of the present invention;
Fig. 7 is a sectional view of the LCD shown in Fig. 6 taken along line VII-VII'; and
Fig. 8 is a sectional view of the LCD shown in Fig. 3 taken along line IV-IV' according to another embodiment of the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0022] The present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. The present invention may, however, be embodied in many different forms and should not be construed as limited to embodiments set forth herein.

[0023] In the drawings, the thickness of layers, films and regions are exaggerated for clarity. Like numerals refer to like elements throughout. It will be understood that when an element such as a layer, film, region or substrate is referred to as being "on" another element, it can be directly on the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly on" another element, there are no intervening elements present.

[0024] An LCD according to an embodiment of the present invention will be described in detail with reference to Figs. 1-5.

[0025] Fig. 1 is a layout view of a thin film transistor (TFT) array panel of an LCD according to an embodiment of the present invention, Fig. 2 is a layout view of a common electrode panel of an LCD according to an embodiment of the present invention, Fig. 3 is a layout view of an LCD including the TFT array panel shown in Fig. 1 and the common electrode panel shown in Fig. 2, Fig. 4 is a sectional view of the LCD shown in Fig. 3 taken along line IV-IV', and Fig. 5 is an equivalent circuit diagram of the LCD shown in Figs. 1-4.

[0026] Referring to Fig. 4, an LCD according to an embodiment of the present invention includes a TFT array panel 100 (see Fig. 1), a common electrode panel 200 (see Fig. 2), and a LC layer 3 interposed between the panels 100 and 200.

[0027] The TFT array panel 100 is now described in detail with reference Figs. 1, 3 and 4.

[0028] A plurality of gate conductors including a plurality of gate lines 121, a plurality of storage electrode lines 131, and a plurality of capacitive electrodes 136 are formed on an insulating substrate 110 such as transparent glass or plastic.

[0029] The gate lines 121 transmit gate signals and extend substantially in a transverse direction on the substrate. Each gate line 121 includes a plurality of gate electrodes 124 projecting upward and an end portion 129 having an area for contact with another layer or an external driving circuit. A gate driving circuit (not shown) for generating the gate signals may be mounted on a flexible printed circuit (FPC) film (not shown), which may be coupled to the substrate 110, directly mounted on the substrate 110, or integrated onto the substrate 110. The gate lines 121 may be connected to a driving circuit that may be integrated on the substrate 110.

[0030] The storage electrode lines 131 are supplied with a predetermined voltage and extend substantially parallel to the gate lines 121. Each of the storage electrode lines 131 is disposed between two gate lines 121 and is nearer a lower one of the two adjacent gate lines 121. Each of the storage electrode lines 131 includes a plurality of storage electrodes 137 extending upward and downward as viewed from the perspective of Fig. 1.

[0031] Each capacitive electrode 136, which are separated from the storage electrode lines 131, includes a wide transverse portion and a narrow oblique portion. The transverse portion is a rectangle elongated substantially parallel to the gate lines 121 and substantially equidistant from adjacent two gate lines 121. The oblique portion extends from a right end of the transverse portion toward a storage electrode line 131, making an angle of about 45 degrees with the gate lines 121.

[0032] The gate conductors 121, 131 and 136 are preferably made of an aluminum (Al) containing metal such as Al and Al alloy, silver (Ag) containing metal such as Ag and Ag alloy, copper (Cu) containing metal such as Cu and Cu alloy, molybdenum (Mo) containing metal such as Mo and Mo alloy, chromium (Cr), tantalum (Ta), or titanium (Ti). The gate lines 121 may have a multilayered structure including two conductive films (not shown) having different physical characteristics. One of the two films is preferably made of low resistivity metal including an Al containing metal, a Ag containing metal, or a Cu containing metal. Such a film can reduce a signal delay or voltage drop. The other film is preferably made of material such as a Mo containing metal, Cr, Ta, or Ti. Such a film has desirable physical, chemical, and electrical contact characteristics with other materials such as indium tin oxide (ITO) or indium zinc oxide (IZO). Exam-

ples of the multi-layer structure include a lower Cr film and an upper Al (alloy) film and a lower Al (alloy) film and an upper Mo (alloy) film. The gate conductors 121, 131 and 136 may be made of various metals or conductors.

[0033] Lateral sides of the gate conductors 121, 131 and 136 are inclined relative to a surface of the substrate 110, and an inclination angle thereof ranges about 30-80 degrees.

[0034] A gate insulating layer 140, preferably made of silicon nitride (SiNx) or silicon oxide (SiOx), is formed on the gate conductors 121, 131 and 136.

[0035] A plurality of semiconductor islands 154, preferably made of hydrogenated amorphous silicon (abbreviated to "a-Si") or polysilicon, are formed on the gate insulating layer 140. The semiconductor islands 154 are disposed on the gate electrodes 124 and include extensions covering edges of the gate lines 121. A plurality of other semiconductor islands (not shown) may be disposed on the storage electrode lines 131.

[0036] A plurality of ohmic contact islands 163 and 165 are formed on the semiconductor islands 154. The ohmic contacts 163 and 165 are preferably made of n+ hydrogenated a-Si, heavily doped with an n-type impurity such as phosphorous or they may be made of silicide. The ohmic contacts 163 and 165 are located in pairs on the semiconductor islands 154.

[0037] The lateral sides of the semiconductor islands 154 and the ohmic contacts 163 and 165 are inclined relative to the surface of the substrate 110, and the inclination angles thereof are preferably in a range of about 30-80 degrees.

[0038] A plurality of data conductors including a plurality of data lines 171 and a plurality of drain electrodes 175 are formed on the ohmic contacts 163 and 165 and the gate insulating layer 140.

[0039] The data lines 171 transmit data signals and extend substantially in a longitudinal direction to intersect the gate lines 121 and the storage electrode lines 131. Each data line 171 includes a plurality of source electrodes 173 projecting toward the gate electrodes 124 and an end portion 179 having an area for contact with another layer or an external driving circuit. A data driving circuit (not shown) for generating the data signals may be mounted on a FPC film (not shown), which may be coupled to the substrate 110, directly mounted on the substrate 110, or integrated onto the substrate 110. The data lines 171 may extend to be connected to a driving circuit that may be integrated on the substrate 110.

[0040] Each of the drain electrodes 175 is separated from the data lines 171 and includes a narrow end portion disposed opposite the source electrodes 173 with respect to the gate electrodes 124. The end portion of each drain electrode 175 is partly surrounded by a respective source electrode 173 that is curved like a character U.

[0041] Each drain electrode 175 further includes an expansion 177 and a coupling electrode 176 connected thereto.

[0042] The expansion 177 overlaps a storage electrode 137 and it has nearly the same shape as the storage electrode 137.

[0043] The coupling electrode 176 is disposed above a capacitive electrode 136 and has substantially the same shape as the capacitive electrode 136. In detail, the coupling electrode 176 has a wide transverse portion and an oblique portion connected to the transverse portion of the expansion 177. The transverse portion of the coupling electrode 176 has a through-hole 176H exposing the gate insulating layer 140. The through-hole 176H is disposed preferably within the boundary of the transverse portion of the coupling electrode 176 and it is preferably equidistant from lower and upper edges of the transverse portion as viewed from the perspective of Fig. 1. Although the through-hole 176H is shown to be square, it may be circular, octagonal, etc.

[0044] A gate electrode 124, a source electrode 173, and a drain electrode 175 along with a semiconductor island 154 form a TFT having an electric channel formed in the semiconductor island 154 disposed between the source electrode 173 and the drain electrode 175.

[0045] The data conductors 171 and 175 are preferably made of a refractory metal such as Cr, Mo, Ta, Ti, or alloys thereof. The data conductors 171 and 175 may have a multilayered structure including a refractory metal film (not shown) and a low resistivity film (not shown). Examples of the multi-layered structure are a double-layered structure including a lower Cr/Mo (alloy) film and an upper Al (alloy) film and a triple-layered structure of a lower Mo (alloy) film, an intermediate A1 (alloy) film, and an upper Mo (alloy) film. The data conductors 171 and 175 may be made of various metals or conductors.

[0046] The data conductors 171 and 175 have inclined edge profiles, and the inclination angles thereof range between about 30-80 degrees.

[0047] The ohmic contacts 163 and 165 are interposed only between the underlying semiconductor islands 154 and the overlying data conductors 171 and 175 thereon and reduce a contact resistance therebetween. Extensions of the semiconductor islands 154 disposed on the edges of the gate lines 121 smooth the profile of the surface to substantially prevent a disconnection of the data lines 171. The semiconductor islands 154 include exposed portions, which are not covered with the data conductors 171 and 175, such as portions located between the source electrodes 173 and the drain electrodes 175.

[0048] A passivation layer 180 is formed on the data conductors 171 and 175, and the exposed portions of the semiconductor islands 154. The passivation layer 180 is preferably made of an inorganic or organic insulator, and may have a flat surface. Examples of the inorganic insulator include silicon nitride and silicon oxide. The organic insulator may be photosensitive and preferably has a dielectric constant of less than about 4.0. The passivation layer 180 may include a lower film of inorganic insulator and an upper film of organic insulator, such that the passivation layer 180 has the insulating characteristics of the organic insulator while substantially

preventing the exposed portions of the semiconductor islands 154 from being damaged by the organic insulator.

[0049] The passivation layer 180 has a plurality of contact holes 182 exposing the end portions 179 of the data lines 171 and a plurality of contact holes 185 exposing the expansions 177 of the drain electrodes 175. The passivation layer 180 and the gate insulating layer 140 have a plurality of contact holes 181 exposing the end portions 129 of the gate lines 121 and a plurality of contact holes 186 penetrating the through-holes 176H without exposing the coupling electrodes 176 and exposing portions of the capacitive electrodes 136. The contact holes 181, 182, 185 and 186 have inclined or stepped sidewalls that can be obtained by using organic material.

[0050] It is preferable that the sidewalls of the contact holes 186 have smooth profiles. The smooth profile having a varying thickness may result in light leakage.. The contact holes 186 are disposed on the coupling electrodes 176 and the capacitive electrodes 136, which are opaque. The opaque area formed by the coupling electrodes 176 and the capacitive electrodes 136 substantially blocks light leakage. A marginal area in the coupling electrode 176 for aligning the through-holes 176H to the contact holes 186 is needed, and the marginal area is relatively small as compared to the opaque area for blocking light leakage. Accordingly, the aperture ratio can be increased.

[0051] The edge of a contact hole 186 is sufficiently spaced apart from a coupling electrode 176 or a capacitive electrode 136 for substantially blocking light leakage and the distance between the edges is preferably greater than about 3.0 microns.

[0052] A plurality of pixel electrodes 190, a shielding electrode 88, and a plurality of contact assistants 81 and 82 are formed on the passivation layer 180. They are preferably made of a transparent conductor such as ITO or IZO or a reflective conductor such as Ag, Al, Cr, or alloys thereof.

[0053] Each pixel electrode 190 is approximately a rectangle having chamfered corners. The chamfered corners of the pixel electrode 190 make an angle of about 45 degrees with the gate lines 121. The pixel electrodes 190 overlap the gate lines 121 to increase the aperture ratio.

[0054] Each of the pixel electrodes 190 has a gap 93 that divides the pixel electrode 190 into an outer subpixel electrode 190a and an inner sub-pixel electrode190b.

[0055] The gap 93 includes lower and upper portions 93a and 93b, respectively, and a longitudinal portion 93c connecting them. The lower and the upper portions 93a and 93b of the gap 93 extend from a left edge to a right edge of the pixel electrode 190, making an angle of about 45 degrees away from and towards the gate lines 121, respectively. The longitudinal portion 93c of the gap 93 connects right ends of the lower and the upper portions 93a and 93b.

[0056] The inner sub-pixel electrode 190b is an isosceles trapezoid rotated by a right angle. The outer subpixel electrode 190a includes a pair of right-angled trapezoids rotated by a right angle and a longitudinal connection connecting the right-angled trapezoids.

[0057] The outer subpixel electrode 190a is connected to an expansion 177 of a drain electrode 175 through a contact hole 185.

[0058] The inner sub-pixel electrode 190b is connected to a capacitive electrode 136 through a contact hole 186 and overlaps a coupling electrode 176. The inner sub-pixel electrode 190b, the capacitive electrode 136, and the coupling electrode 176 form a coupling capacitor.

[0059] The inner sub-pixel electrode 190b has central cutouts 91 and 92. A lower half of the outer sub-pixel electrode 190a has lower cutouts 94a and 95a, and an upper half of the outer sub-pixel electrode 190a has upper cutouts 94b and 95b. The cutouts 91, 92 and 94a-95b partition the sub-pixel electrodes 190b and 190a into a plurality of partitions. The pixel electrode 190 having the cutouts 91, 92 and 94a-95b and the gap 93 substantially has inversion symmetry across the capacitive electrode 136. Individual portions 93a-93c of the gap 93 will be also referred to as cutouts hereinafter.

[0060] Each of the lower and the upper cutouts 94a-95b obliquely extends approximately from a left corner, a lower edge, or an upper edge of the pixel electrode 190 approximately to a right edge of the pixel electrode 190. The lower and the upper cutouts 94a-95b make an angle of about 45 degrees to the gate lines 121, and they extend substantially perpendicular to each other.

[0061] Each of the center cutouts 91 and 92 includes a transverse portion and a pair of oblique portions connected thereto. The transverse portion extends along the capacitive electrode 136, and the oblique portions obliquely extend from the transverse portion toward the left edge of the pixel electrode 190 in parallel to the lower and the upper cutouts 94a-95b, respectively. The transverse portion of the center cutout 92 is connected to the longitudinal portion 93c of the gap 93.

[0062] The number of the cutouts or the number of the partitions may be varied depending on design factors such as the size of the pixel electrode 190, the ratio of the transverse edges to the longitudinal edges of the pixel electrode 190, the type and characteristics of the liquid crystal layer 3, and so on.

[0063] The shielding electrode 88 is supplied with the common voltage and it includes longitudinal portions extending along the data lines 171 and transverse portions extending along the gate lines 121 to connect adjacent longitudinal portions. The longitudinal portions fully cover the data lines 171, while each of the transverse portions lies within the boundary of a gate line 121.

[0064] The shielding electrode 88 substantially blocks electromagnetic interference between the data lines 171 and the pixel electrodes 190 and between the data lines 171 and a common electrode 270 to reduce distortion of the voltage of the pixel electrodes 190 and a signal delay of the data voltages carried by the data lines 171.

[0065] The contact assistants 81 and 82 are connected to the end portions 129 of the gate lines 121 and the end portions 179 of the data lines 171 through the contact holes 181 and 182, respectively. The contact assistants 81 and 82 protect the end portions 129 and 179, respectively, and enhance the adhesion between the end portions 129 and 179 and external devices.

[0066] The description of the common electrode panel 200 follows with reference to Figs. 2-4.

[0067] A light blocking member 220, referred to as a black matrix, for preventing light leakage is formed on an insulating substrate 210 such as transparent glass or plastic. The light blocking member 220 includes a plurality of rectilinear portions facing the data lines 171 on the TFT array panel 100 and a plurality of widened portions facing the TFTs on the TFT array panel 100. Alternatively, the light blocking member 220 may have a plurality of through-holes that face the pixel electrodes 190, the light blocking member 220 having substantially the same planar shape as the pixel electrodes 190.

[0068] A plurality of color filters 230 are also formed on the substrate 210, disposed substantially in the areas between the light blocking member 220. The color filters 230 may extend substantially along the longitudinal direction along the pixel electrodes 190. The color filters 230 may represent one of the primary colors such as red, green or blue.

[0069] An overcoat 250 is formed on a surface of the color filters 230 and the light blocking member 220 facing the TFT array panel 100. The overcoat 250 is preferably made of (organic) insulator and substantially prevents the color filters 230 from being exposed and provides a flat surface.

[0070] A common electrode 270 is formed on a surface of the overcoat 250 facing the TFT array panel 100. The common electrode 270 is preferably made of a transparent conductive material such as ITO and IZO and has a plurality of sets of cutouts 71, 72, 73, 74a, 74b, 75a, 75b, 76a and 76b.

[0071] A set of cutouts 71-76b face a pixel electrode 190 and include center cutouts 71, 72 and 73, lower cutout 74a, 75a and 76a and upper cutouts 74b, 75b and 76b. The cutout 71 is disposed near the contact hole 186 and each of the cutouts 72-76b is disposed between adjacent cutouts 91-95b of the pixel electrode 190 or between a cutout 95a or 95b and a chamfered edge of the pixel electrode 190. Each of the cutouts 71-76b has at least an oblique portion extending substantially parallel to the lower cutout 93a-95a or the upper cutout 93b-95b of the pixel electrode 190. The cutouts 71-76b substantially have inversion symmetry across the capacitive electrode 136.

[0072] Each of the lower and the upper cutouts 74a-76b includes an oblique portion, a transverse portion and a longitudinal portion or an oblique portion and a pair of longitudinal portions. The oblique portion extends approximately from a left edge, a lower edge, or an upper edge of the pixel electrode 190 approximately to a right edge of the pixel electrode 190. The transverse and longitudinal portions extend from respective ends of the oblique portion along edges of the pixel electrode 190, overlapping the edges of the pixel electrode 190, and making obtuse angles with the oblique portion.

[0073] Each of the center cutouts 71 and 72 includes a central transverse portion, a pair of oblique portions, and a pair of terminal longitudinal portions. The center cutout 73 includes a pair of oblique portions and a pair of terminal longitudinal portions. The central transverse portions of cutouts 71 and 72 are disposed near the left edge or a center of the pixel electrode 190 and extend along the capacitive electrode 136. The oblique portions extend from an end of the central transverse portion or approximately from a center of the right edge of the pixel electrode 190, approximately to the left edge of the pixel electrode. The oblique portions of the cutouts 71 and 72 make oblique angles with the respective central transverse portion and an oblique portion of the cutout 73 overlaps an oblique portion of a capacitive electrode 136 or a coupling electrode 176. The terminal longitudinal portions extend from the ends of the respective oblique portions along the left edge of the pixel electrode 190, overlapping the left edge of the pixel electrode 190, and making obtuse angles with the respective oblique portions.

[0074] The number of the cutouts 71-76b may be also varied depending on the design factors. The light blocking member 220 may overlap the cutouts 71-76b to block the light leakage through the cutouts 71-76b.

[0075] Alignment layers 11 and 21, which may be homeotropic, are coated on inner surfaces of the panels 100 and 200, and polarizers 12 and 22 are provided on outer surfaces of the panels 100 and 200 having crossed polarization axes, wherein one of the polarization axes may be parallel to the gate lines 121. One of the polarizers 12 and 22 may be omitted when the LCD is a reflective LCD.

[0076] The LCD may further include at least one retardation film (not shown) for compensating a retardation of the LC layer 3. The retardation film has birefringence and gives a retardation opposite to that given by the LC layer 3.

[0077] The LCD may further include a backlight unit (not shown) supplying light to the LC layer 3 through the polarizers 12 and 22, the retardation film, and the panels 100 and 200.

[0078] It is preferable that the LC layer 3 has negative dielectric anisotropy and is subjected to a vertical alignment, wherein the LC molecules in the LC layer 3 are aligned such that their long axes are substantially vertical to the surfaces of the panels 100 and 200 in the absence of an electric field. Accordingly, incident light cannot pass the crossed polarization system 12 and 22.

[0079] The LCD shown in Figs. 1-4 is represented as an equivalent circuit shown in Fig. 5.

[0080] Referring to Fig. 5, a pixel of the LCD includes a TFT Q, a first subpixel including a first LC capacitor Clca and a storage capacitor Csta, a second subpixel

including a second LC capacitor Clcb, and a coupling capacitor Ccp.

[0081] The first LC capacitor Clca includes an outer sub-pixel electrode 190a as one terminal, a portion of the common electrode 270 corresponding thereto as a second terminal, and a portion of the LC layer 3 disposed therebetween as a dielectric. Similarly, the second LC capacitor Clcb includes an inner sub-pixel electrode 190b as one terminal, a portion of the common electrode 270 corresponding thereto as a second terminal, and a portion of the LC layer 3 disposed thereon as a dielectric.

[0082] The storage capacitor Csta includes an expansion 177 of a drain electrode 175 as one terminal, a storage electrode 137 as a second terminal, and a portion of the gate insulating layer 140 disposed therebetween as a dielectric.

[0083] The coupling capacitor Ccp includes an inner sub-pixel electrode 190b and a capacitive electrode 136 as one terminal, a coupling electrode 176 as a second terminal, and portions of the passivation layer 180 and the gate insulating layer 140 disposed therebetween as a dielectric.

[0084] The first LC capacitor Clca and the storage capacitor Csta are connected in parallel to a drain of the TFT Q. The coupling capacitor Ccp is connected between the drain of the TFT Q and the second LC capacitor Clcb. The common electrode 270 is supplied with a common voltage Vcom and the storage electrode lines 131 may be supplied with the common voltage Vcom.

[0085] The TFT Q applies data voltages from a data line 171 to the first LC capacitor Clca and the coupling capacitor Ccp in response to a gate signal from a gate line 121. The coupling capacitor Ccp transmits the data voltage with a modified magnitude to the second LC capacitor Clcb.

[0086] If the storage electrode line 131 is supplied with the common voltage Vcom and each of the capacitors Clca, Csta, Clcb and Ccp and the capacitance thereof are denoted as the same reference characters, the voltage Vb charged across the second LC capacitor Clcb may be given by:

$$Vb=Va\times[Ccp/(Ccp+Clcb)],$$

where Va denotes the voltage of the first LC capacitor Clca.

[0087] Since the term Ccp/(Ccp+Clcb) is smaller than one, the voltage Vb of the second LC capacitor Clcb is greater than that of the first LC capacitor Clca. This inequality may be true for a case that the voltage of the storage electrode line 131 is not equal to the common voltage Vcom.

[0088] When the potential difference is generated across the first LC capacitor Clca or the second LC capacitor Clcb, an electric field substantially perpendicular to the surfaces of the panels 100 and 200 is generated in the LC layer 3. The pixel electrode 190 and the common electrode 270 are commonly referred to as field generating electrodes hereinafter. The LC molecules in the LC layer 3 tilt in response to the electric field such that their long axes are substantially perpendicular to the field direction. The degree of the tilt of the LC molecules determines the variation of the polarization of light incident on the LC layer 3. The variation of the light polarization is transformed into the variation of the light transmittance by the polarizers 12 and 22. In this way, the LCD displays images.

[0089] The tilt angle of the LC molecules depends on the strength of the electric field. Since the voltage Va of the first LC capacitor Clca and the voltage Va of the second LC capacitor Clcb are different from each other, the tilt direction of the LC molecules in the first subpixel is different from that in the second subpixel and thus the luminances of the two subpixels are different. For maintaining the average luminance of the two subpixels in a target luminance, the voltages Va and Vb of the first and the second subpixels can be adjusted so that an image viewed from a lateral side is the substantially similar to an image viewed from the front, thereby improving the lateral visibility.

[0090] The ratio of the voltages Va and Vb can be adjusted by varying the capacitance of the coupling capacitor Ccp. The coupling capacitance Ccp can be varied by changing the overlapping area and distance between the coupling electrode 176 and the inner sub-pixel electrode 190b (and the capacitive electrode 136). For example, the distance between the coupling electrode 176 and the inner sub-pixel electrode 190b increases when the capacitive electrode 136 is removed and the coupling electrode 176 is moved to the position of the capacitive electrode 136. Preferably, the voltage Vb of the second LC capacitor Clcb is from about 0.6 to about 0.8 times the voltage Va of the first LC capacitor Clca.

[0091] The voltage Vb charged in the second LC capacitor Clcb may be larger than the voltage Va of the first LC capacitor Clca. This can be realized by precharging the second LC capacitor Clcb with a predetermined voltage such as the common voltage Vcom.

[0092] The ratio of the outer subpixel electrode 190a of the first subpixel and the inner sub-pixel electrode 190b of the second subpixel is preferably from about 1:0.85 to about 1:1.15. Further, the number of the sub-pixel electrodes in each of the LC capacitors Clca and Clcb may be changed.

[0093] The tilt direction of the LC molecules is determined by a horizontal component generated by the cutouts 91-95b and 71-76b of the field generating electrodes 190 and 270 and the oblique edges of the pixel electrodes 190 distorting the electric field, which is substantially perpendicular to the edges of the cutouts 91-95b and 71-76b and the oblique edges of the pixel electrodes 190. Referring to Fig. 3, a set of the cutouts 91-95b and 71-76b divides a pixel electrode 190 into a plurality of subareas and each sub-area has two major edges. Since the LC

molecules on each sub-area tilt substantially perpendicular to the major edges, the azimuthal distribution of the tilt directions are substantially localized to four directions, thereby increasing the reference viewing angle of the LCD.

[0094] The shapes and the arrangements of the cutouts 91-95b and 71-76b for determining the tilt directions of the LC molecules may be modified and at least one of the cutouts 91-95b and 71-76b can be substituted with protrusions (not shown) or depressions (not shown). The protrusions are preferably made of organic or inorganic material and disposed on or under the field-generating electrodes 190 or 270.

[0095] Since there is substantially no electric field between the shielding electrode 88 and the common electrode 270, the LC molecules on the shielding electrode 88 remain in an initial orientation and thus the light incident thereon is blocked. Accordingly, the shielding electrode 88 may serve as a light blocking member.

[0096] Now, a method of manufacturing a TFT array panel shown in Figs. 1-4 will be described in detail.

[0097] A conductive layer preferably made of metal is deposited on an insulating substrate 110, for example, by sputtering, etc. The conductive layer is subjected to lithography and etching to form a plurality of gate lines 121 including gate electrodes 124 and end portions 129, a plurality of storage electrode lines 131 including storage electrodes 137, and a plurality of capacitive electrodes 136.

[0098] A gate insulating layer 140 having a thickness of about 1,500-5,000 Å, an intrinsic amorphous silicon layer having a thickness of about 500-2,000 Å, and an extrinsic amorphous silicon layer having a thickness of about 300-600 Å are sequentially deposited. The extrinsic amorphous silicon layer and the intrinsic amorphous silicon layer are patterned by lithography and etching to form a plurality of extrinsic semiconductor islands and a plurality of intrinsic semiconductor islands 154.

[0099] A conductive layer having a thickness of about 1,500-3,000 Å is deposited, for example, by sputtering, etc., and patterned by lithography and etching to form a plurality of data lines 171 including source electrodes 173 and end portions 179, a plurality of drain electrodes 175 including expansions 177, and coupling electrodes 176 having through-holes 176H.

[0100] Exposed portions of the extrinsic semiconductor islands, which are not covered by the data lines 171 and the drain electrodes 175, are removed to form a plurality of ohmic contact islands 163 and 165 and to expose portions of the intrinsic semiconductor islands 154. Oxygen plasma treatment preferably follows to stabilize the exposed surfaces of the semiconductor islands 154.

[0101] An organic insulating film having positive photosensitivity is coated, exposed to light through a mask (not shown), and developed to form a passivation layer 180 having a plurality of contact holes 182 and 185 and upper portions of a plurality of contact holes 181 and 186. The mask used for forming the passivation layer 180 has light blocking areas, light transmitting areas, and translucent areas. When the mask is aligned with the substrate 110, the light transmitting areas face centers of the contact holes 181, 182, 185 and 186 and the translucent areas surround the light transmitting areas. The contact holes 181, 182, 185 and 186 have smooth or stepped sidewall profiles. The through-holes 176H are designed in consideration of the size of the contact holes 186. When the organic insulating film has negative photosensitivity, the transmittance of the areas in the mask is exchanged as compared with positive sensitivity.

[0102] Portions of the gate insulating layer 140 exposed through the upper portions of the contact holes 181 and 186 are removed to complete the contact holes 181 and 186.

[0103] When the data lines 171, the drain electrodes 175, the gate lines 121, or the capacitive electrodes 136 have Al upper films, portions of the Al upper films exposed through the contact holes 181,182,185 and 186 are removed by a blanket etch.

[0104] An ITO or IZO layer having a thickness of about 400-500 Å is deposited, for example, by sputtering, etc., and patterned by lithography and etching to form a plurality of pixel electrodes 190, a shielding electrode 88, and a plurality of contact assistants 81 and 82.

[0105] An LCD according to an embodiment of the present invention will be described in detail with reference to Figs. 6 and 7.

[0106] Fig. 6 is a layout view of an LCD according to an embodiment of the present invention, and Fig. 7 is a sectional view of the LCD shown in Fig. 6 taken along line VII-VII'.

[0107] Referring to Figs. 6 and 7, an LCD includes a TFT array panel 100, a common electrode panel 200, a LC layer 3 interposed between the panels 100 and 200, and a pair of polarizers 12 and 22 attached on outer surfaces of the panels 100 and 200.

[0108] Layered structures of the panels 100 and 200 are substantially the same as those shown in Figs. 1-4.

[0109] Regarding the TFT array panel 100, a plurality of gate lines 121, including gate electrodes 124 and end portions 129, a plurality of storage electrode lines 131, including storage electrodes 137, and a plurality of capacitive electrodes 136 are formed on a substrate 110. A gate insulating layer 140, a plurality of semiconductors 154, and a plurality of ohmic contacts 163 and 165 are sequentially formed on the gate lines 121 and the storage electrodes lines 131. A plurality of data lines 171, including source electrodes 173 and end portions 179, and a plurality of drain electrodes 175, including expansions 177, and coupling electrodes 176 are formed on the ohmic contacts 163 and 165. A passivation layer 180 is formed on the data lines 171, the drain electrodes 175, and exposed portions of the semiconductors 154. A plurality of contact holes 181, 182, 185 and 186 are provided through the passivation layer 180. The gate insulating layer 140 and the contact holes 186 pass through through-holes 176H provided at the coupling electrodes

176. A plurality of pixel electrodes 190 including subpixel electrodes 190a and 190b and having cutouts 91-95b, a shielding electrode 88, and a plurality of contact assistants 81 and 82 are formed on the passivation layer 180, and an alignment layer 11 is coated thereon.

[0110] Regarding the common electrode panel 200, a light blocking member 220, a plurality of color filters 230, an overcoat 250, a common electrode 270 having cutouts 71-76b, and an alignment layer 21 are formed on an insulating substrate 210 facing the TFT array panel 100.

[0111] Different from the LCD shown in Figs. 1-4, the semiconductor islands 154 and the ohmic contacts 163 of the TFT array panel 100 extend along the data lines 171 to form a semiconductor island 151 and an ohmic contact 161. In addition, the semiconductor islands 154 have substantially the same planar shapes as the data lines 171 and the drain electrodes 175 as well as the underlying ohmic contacts 163 and 165. The semiconductor islands 154 include some exposed portions, which are not covered with the data lines 171 and the drain electrodes 175, such as portions located between the source electrodes 173 and the drain electrodes 175.

[0112] In addition, the capacitive electrodes 136 have no oblique portion, and each of the drain electrodes 175 includes an interconnection 178 extending substantially parallel to the data lines 171 and connecting the expansion 177 and the coupling electrode 176 near left sides thereof.

[0113] A manufacturing method of the TFT array panel according to an embodiment of the present invention simultaneously forms the data lines 171 and the drain electrodes 175, the semiconductor islands 151, and the ohmic contacts 161 and 165 using one photolithography step.

[0114] A photoresist masking pattern for the photolithography process has position-dependent thickness, and in particular, it has thicker portions and thinner portions. The thicker portions are located on wire areas that will be occupied by the data lines 171 and the drain electrodes 175, and the thinner portions are located on channel areas of TFTs.

[0115] The position-dependent thickness of the photoresist is obtained by several techniques, for example, by providing translucent areas on the exposure mask as well as transparent areas and light blocking opaque areas. The translucent areas may have a slit pattern, a lattice pattern, or a thin film(s) with intermediate transmittance or intermediate thickness. When using a slit pattern, it is preferable that the width of the slits or the distance between the slits is smaller than the resolution of a light exposer used for the photolithography. Another example is to use a reflowable photoresist. In detail, once a photoresist pattern made of a reflowable material is formed by using an exposure mask with transparent areas and opaque areas, it is subjected to a reflow process to flow onto areas without the photoresist, thereby forming thin portions.

[0116] As a result, the manufacturing process is simplified by omitting a photolithography step.

[0117] Many of the above-described features of the LCD shown in Figs. 1-4 may be appropriate to the LCD shown in Figs. 6 and 7.

[0118] An LCD according to an embodiment of the present invention will be described in detail with reference to Fig. 8.

[0119] Fig. 8 is a sectional view of the LCD shown in Fig. 3 taken along line IV-IV'.

[0120] Referring to Fig. 8, an LCD includes a TFT array panel 100, a common electrode panel 200, a LC layer 3 interposed between the panels 100 and 200, and a pair of polarizers 12 and 22 attached on outer surfaces of the panels 100 and 200.

[0121] Layered structures of the panels 100 and 200 are substantially the same as those shown in Figs. 1-4.

[0122] Regarding the TFT array panel 100, a plurality of gate lines 121 including gate electrodes 124 and end portions 129, a plurality of storage electrode lines 131 including storage electrodes 137, and a plurality of capacitive electrodes 136 are formed on a substrate 110. A gate insulating layer 140, a plurality of semiconductors islands 154, and a plurality of ohmic contacts 163 and 165 are sequentially formed on the gate lines 121 and the storage electrodes lines 131. A plurality of data lines 171 including source electrodes 173 and end portions 179 and a plurality of drain electrodes 175 including expansions 177 and coupling electrodes 176 are formed on the ohmic contacts 163 and 165 and the gate insulating layer 140. A passivation layer 180 is formed on the data lines 171, the drain electrodes 175, and exposed portions of the semiconductors 154. A plurality of contact holes 181, 182,185 and 186 are provided through the passivation layer 180 and the gate insulating layer 140. The contact holes 186 pass through through-holes 176H provided at the coupling electrodes 176. A plurality of pixel electrodes 190 including subpixel electrodes 190a and 190b and having cutouts 91-95b, a shielding electrode 88, and a plurality of contact assistants 81 and 82 are formed on the passivation layer 180, and an alignment layer 11 is coated thereon.

[0123] Regarding the common electrode panel 200, a light blocking member 220, an overcoat 250, a common electrode 270 having cutouts 71-76b, and an alignment layer 21 are formed on a surface an insulating substrate 210 facing the TFT array panel 100.

[0124] Different from the LCD shown in Figs. 1-4, the TFT array panel 100 includes a plurality of color filters 230 disposed under the passivation layer 180, while the common electrode panel 200 has no color filter. In this case, the overcoat 250 may be removed from the common electrode panel 200.

[0125] The color filters 230 are disposed between two adjacent data lines 171 and have a plurality of through-holes 235 and 236 through which the contact holes 185 and 186 pass through, respectively. The color filters 230 are not provided on peripheral areas provided with the end portions 129 and 179 of the signal lines 121 and 171.

[0126] The color filters 230 may extend along a longi-

tudinal direction to form stripes and the edges of two adjacent color filters 230 may match with each other on the data lines 171. The color filters 230 may overlap each other to block light leakage between the pixel electrodes 190, or may be spaced apart from each other. When the color filters 230 overlap each other, linear portions of the light blocking member 220 may be omitted and the shielding electrode 88 may cover edges of the color filters 230. Overlapping portions of the color filters 230 may have a reduced thickness to decrease the height difference.

[0127] The color filters 230 may be disposed on the passivation layer 180, or the passivation layer 180 may be omitted.

[0128] Many of the above-described features of the LCD shown in Figs. 1-4 may be appropriate to the LCD shown in Fig. 8.

Claims

1. A thin film transistor array panel (100) comprising:

a substrate (110);
gate lines (121) disposed on the substrate (110);
capacitive electrodes (136) disposed on the substrate (110) and separated from the gate lines (121);
data lines (171) intersecting the gate lines (121);
a gate insulating layer (140) covering the gate lines (121) and the capacitive electrodes (136); and
thin film transistors (154);
wherein each of the thin film transistors (154) is connected to a respective one of the gate lines (121) and the data lines (171), and includes a drain electrode (175), a coupling electrode (176) connected to the drain electrode (175), and a pixel electrode (190) including a first subpixel electrode (190a) and a second subpixel electrode (190b), the first subpixel electrode (190a) being connected to the drain electrode (175);
characterized in that
each coupling electrode (176) overlaps a respective one of the capacitive electrodes (136) and comprises a through-hole (176H);
a passivation layer (180) is disposed on the gate lines (121), the data lines (171), and the thin film transistors (154) and has contact holes (181, 182, 185, 186) penetrating the through-holes (176H) for exposing the capacitive electrodes (136); and **in that**
each of the second subpixel electrodes (190b) is connected to the associated capacitive electrode (136) through a contact hole (181, 182, 185, 186),

2. The thin film transistor array panel (100) of claim 1, wherein the through-hole (176H) is substantially equidistant from two opposite edges of the capacitive electrode (136).

3. The thin film transistor array panel (100) of claim 1, wherein the through-hole (176H) is rectangular, octagonal, or circular.

4. The thin film transistor array panel (100) of claim 1, wherein the contact hole (181, 182, 185, 186) has a stepped sidewall.

5. The thin film transistor array panel (100) of claim 1, wherein a distance between an edge of the contact hole (181, 182, 185, 186) and the through-hole (176H) is equal to or greater than about 3.0 microns.

6. The thin film transistor array panel (100) of claim 1, further comprising a shielding electrode (88) separated from the pixel electrode (190) and overlapping a portion of the data lines (171) or the gate lines (121).

7. The thin film transistor array panel (100) of claim 6, wherein the pixel electrode (190) and the shielding electrode (88) are disposed on the passivation layer (180).

8. The thin film transistor array panel (100) of claim 6, further comprising a storage electrode (137) overlapping the drain electrode (175).

9. The thin film transistor array panel (100) of claim 8, wherein the shielding electrode (88) and the storage electrode (137) are supplied with substantially the same voltage.

10. The thin film transistor array panel (100) of claim 9, wherein the shielding electrode (88) extends along the data lines (171) or the gate lines (121).

11. The thin film transistor array panel (100) of claim 10, wherein the shielding electrode (88) fully covers the data lines (171).

12. The thin film transistor array panel (100) of claim 1, wherein the pixel electrode (190) has a chamfered corner.

13. The thin film transistor array panel (100) of claim 1, wherein the passivation layer (180) comprises an organic insulator.

14. The thin film transistor array panel (100) of claim 13, further comprising a color filter (230) disposed on or under the passivation layer (180).

15. The thin film transistor array panel (100) of claim 1, wherein the pixel electrode(190) comprises a parti-

tioning member for partitioning the pixel electrode (190) into a plurality of partitions.

16. The thin film transistor array panel (100) of claim 15, wherein the partitioning member makes an angle of about 45 degrees with the gate lines (121).

17. A method of manufacturing a thin film transistor array panel (100), the method comprising:

forming gate lines (121) and capacitive electrodes (136) on a substrate (110);
forming a gate insulating layer (140) covering the gate lines (121), the capacitive electrode (136) and the substrate (110);
forming data lines (171) on the gate insulating layer (140);
forming thin film transistors (154), each of the thin film transistors (154), including a drain electrode (175), and a coupling electrode (176) being formed on the gate insulating layer (140), the coupling electrode (176) being connected to the drain electrode (175);
connecting each of thin film transistors (154) to a respective one of the gate lines (121) and the data lines (171);
forming a pixel electrode (190) for the each of thin film transistors (154), the pixel electrodes (190) including a first subpixel electrode (190a) and a second subpixel electrode (190b), the first subpixel electrode (190a) being connected to the drain electrode (175);
characterized in that each coupling electrode (176) overlaps a respective one of the capacitive electrodes (136) and comprises a through-hole (176H);
a passivation layer (180) is disposed on the data lines (171), the drain electrode (175), and the coupling electrode (176), the passivation layer (180) having contact holes (181, 182, 185, 186) penetrating the through-holes (176H) for exposing the capacitive electrodes (136); and **in that** the pixel electrode (190) is formed on the passivation layer (180), and each of the second subpixel electrodes (190b) is connected to the associated capacitive electrode (136) through a contact hole (181, 182, 185, 186).

18. The method of claim 17, wherein the through-hole (176H) is substantially equidistant from two opposite edges of the capacitive electrode (136)

19. The method of claim 17, wherein the through-hole (176H) is rectangular, octagonal, or circular.

20. The method of claim 17, wherein the contact hole (181, 182, 185, 186) has a stepped sidewall.

Patentansprüche

1. Platte mit Dünnschichttransistoranordnung (100), umfassend:

ein Substrat (110);
Gateleitungen (121), die am Substrat (110) angeordnet sind;
kapazitive Elektroden (136), die am Substrat (110) angeordnet sind und von den Gateleitungen (121) getrennt sind;
Datenleitungen (171), die die Gateleitungen (121) kreuzen;
eine Gate-Isolierschicht (140), die die Gateleitungen (121) und die kapazitiven Elektroden (136) bedeckt); und
Dünnschichttransistoren (154);
wobei jeder der Dünnschichttransistoren (154) jeweils mit einer der Gateleitungen (121) und der Datenleitungen (171) verbunden ist und umfasst: eine Drainelektrode (175), eine Kopplungselektrode (176), die mit der Drainelektrode (175) verbunden ist, und eine Pixelelektrode (190) mit einer ersten Subpixelelektrode (190a) und einer zweiten Subpixelelektrode (190b), wobei die erste Subpixelelektrode (190a) mit der Drainelektrode (175) verbunden ist;
dadurch gekennzeichnet, dass
jede Kopplungselektrode (176) jeweils eine der kapazitiven Elektroden (136) überlappt und eine Durchgangsbohrung (176H) umfasst;
eine Passivierungsschicht (180) auf den Gateleitungen (121), den Datenleitungen (171) und den Dünnschichttransistoren (154) angeordnet ist und Kontaktöffnungen (181, 182, 185, 186) aufweist, die durch die Durchgangsbohrungen (176H) gehen, um die kapazitiven Elektroden (136) freizulegen; und dass
jede der zweiten Subpixelelektroden (190b) durch eine Kontaktöffnung (181, 182, 185, 186) mit der zugeordneten kapazitiven Elektrode (136) verbunden ist.

2. Platte mit Dünnschichttransistoranordnung (100) nach Anspruch 1, wobei die Durchgangsbohrung (176H) im Wesentlichen gleich weit von den zwei entgegengesetzten Rändern der kapazitiven Elektrode (136) entfernt ist.

3. Platte mit Dünnschichttransistoranordnung (100) nach Anspruch 1, wobei die Durchgangsbohrung (176H) rechteckig, achteckig oder kreisförmig ist.

4. Platte mit Dünnschichttransistoranordnung (100) nach Anspruch 1, wobei die Kontaktöffnung (181, 182, 185, 186) eine stufenförmige Seitenwand aufweist.

5. Platte mit Dünnschichttransistoranordnung (100) nach Anspruch 1, wobei ein Abstand zwischen einem Rand der Kontaktöffnung (181, 182, 185, 186) und der Durchgangsbohrung (176H) gleich oder größer als etwa 3,0 Mikron ist.

6. Platte mit Dünnschichttransistoranordnung (100) nach Anspruch 1, darüber hinaus umfassend eine Abschirmelektrode (88), die von der Pixelelektrode (190) getrennt ist und einen Teil der Datenleitungen (171) oder der Gateleitungen (121) überlappt.

7. Platte mit Dünnschichttransistoranordnung (100) nach Anspruch 6, wobei die Pixelelektrode (190) und die Abschirmelektrode (88) auf der Passivierungsschicht (180) angeordnet sind.

8. Platte mit Dünnschichttransistoranordnung (100) nach Anspruch 6, darüber hinaus eine Speicherelektrode (137), die die Drainelektrode (175) überlappt.

9. Platte mit Dünnschichttransistoranordnung (100) nach Anspruch 8, wobei die Abschirmelektrode (88) und die Speicherelektrode (137) mit im Wesentlichen der gleichen Spannung gespeist werden.

10. Platte mit Dünnschichttransistoranordnung (100) nach Anspruch 9, wobei sich die Abschirmelektrode (88) entlang der Datenleitungen (171) oder der Gateleitungen (121) erstreckt.

11. Platte mit Dünnschichttransistoranordnung (100) nach Anspruch 10, wobei die Abschirmelektrode (88) die Datenleitungen (171) vollständig bedeckt.

12. Platte mit Dünnschichttransistoranordnung (100) nach Anspruch 1, wobei die Pixelelektrode (190) eine abgeschrägte Ecke aufweist.

13. Platte mit Dünnschichttransistoranordnung (100) nach Anspruch 1, wobei die Passivierungsschicht (180) eine organische Isolierung umfasst.

14. Platte mit Dünnschichttransistoranordnung (100) nach Anspruch 13, darüber hinaus umfassend einen Farbfilter (230), der auf oder unter der Passivierungsschicht (180) angeordnet ist.

15. Platte mit Dünnschichttransistoranordnung (100) nach Anspruch 1, wobei die Pixelelektrode (190) ein Unterteilungselement umfasst, um die Pixelelektrode (190) in eine Vielzahl von Unterteilungen aufzuteilen.

16. Platte mit Dünnschichttransistoranordnung (100) nach Anspruch 15, wobei das Unterteilungselement mit den Gateleitungen (121) einen Winkel von etwa 45 Grad bildet.

17. Verfahren zur Herstellung einer Platte mit Dünnschichttransistoranordnung (100), wobei das Verfahren umfasst:

die Bildung von Gateleitungen (121) und kapazitiven Elektroden (136) auf einem Substrat (110);
die Bildung einer Gate-Isolierschicht (140), die die Gateleitungen (121), die kapazitive Elektrode (136) und das Substrat (110) bedeckt;
die Bildung von Datenleitungen (171) auf der Gate-Isolierschicht (140);
die Bildung von Dünnschichttransistoren (154), wobei jeder der Dünnschichttransistoren (154) umfasst: eine Drainelektrode (175) und eine Kopplungselektrode (176), die auf der Gate-Isolierschicht (140) gebildet sind, wobei die Kopplungselektrode (176) mit der Drainelektrode (175) verbunden ist;
die Verbindung jedes der Dünnschichttransistoren (154) mit jeweils einer der Gateleitungen (121) und der Datenleitungen (171);
die Bildung einer Pixelelektrode (190) für jeden der Dünnschichttransistoren (154), wobei die Pixelelektroden (190) eine erste Subpixelelektrode (190a) und eine zweite Subpixelelektrode (190b) umfassen, wobei die erste Subpixelelektrode (190a) mit der Drainelektrode (175) verbunden ist;
dadurch gekennzeichnet, dass
jede Kopplungselektrode (176) jeweils eine der kapazitiven Elektroden (136) überlappt und eine Durchgangsbohrung (176H) umfasst;
eine Passivierungsschicht (180) auf den Datenleitungen (171), der Drainelektrode (175) und der Kopplungselektrode (176) angeordnet ist,
wobei die Passivierungsschicht (180) Kontaktöffnungen (181, 182, 185, 186) aufweist, die durch die Durchgangsbohrungen (176H) gehen, um die kapazitiven Elektroden (136) freizulegen; und dass
die Pixelelektrode (190) auf der Passivierungsschicht (180) gebildet ist und jede der zweiten Subpixelelektroden (190b) durch eine Kontaktöffnung (181, 182, 185, 186) mit der zugeordneten kapazitiven Elektrode (136) verbunden ist.

18. Verfahren nach Anspruch 17, wobei die Durchgangsbohrung (176H) im Wesentlichen gleich weit von den zwei entgegengesetzten Rändern der kapazitiven Elektrode (136) entfernt ist.

19. Verfahren nach Anspruch 17, wobei die Durchgangsbohrung (176H) rechteckig, achteckig oder kreisförmig ist.

20. Verfahren nach Anspruch 17, wobei die Kontaktöff-

nung (181, 182, 185, 186) eine stufenförmige Seitenwand aufweist.

Revendications

1. Panneau à matrice de transistors à couche mince (100) comprenant :

un substrat (110) ;
des lignes de grille (121) disposées sur le substrat (110);
des électrodes capacitives (136) disposées sur le substrat (110) et
séparées des lignes de grille (121) ;
des lignes de données (171) croisant les lignes de grille (121) ;
une couche isolante de grille (140) recouvrant les lignes de grille (121) et
les électrodes capacitives (136) ; et
des transistors à couche mince (154) ;
dans lequel chacun des transistors à couche mince (154) est connecté respectivement à l'une des lignes de grille (121) et des lignes de données (171), et comprend une électrode de drain (175), une électrode de couplage (176) connectée à l'électrode de drain (175) et une électrode de pixel (190) comprenant une première électrode de sous-pixel (190a) et une deuxième électrode de sous-pixel (190b), la première électrode de sous-pixel (190a) étant connectée à l'électrode de drain (175) ;
caractérisé en ce que
chaque électrode de couplage (176) chevauche une électrode capacitive (136) correspondante et comprend un trou traversant (176H) ;
une couche de passivation (180) est disposée sur les lignes de grille (121), les lignes de données (171) et les transistors à couche mince (154) et possède des trous de contact (181, 182, 185, 186) pénétrant dans les trous traversants (176H) pour exposer les électrodes capacitives (136) ; et **en ce que**
chacune des deuxièmes électrodes de sous-pixel (190b) est connectée à l'électrode capacitive (136) correspondante à travers un trou de contact (181, 182, 185, 186).

2. Panneau à matrice de transistors à couche mince (100) selon la revendication 1, dans lequel le trou traversant (176H) est substantiellement équidistant de deux bords opposés de l'électrode capacitive (136).

3. Panneau à matrice de transistors à couche mince (100) selon la revendication 1, dans lequel le trou traversant (176H) est rectangulaire, octogonal ou circulaire.

4. Panneau à matrice de transistors à couche mince (100) selon la revendication 1, dans lequel le trou de contact (181, 182, 185, 186) possède une paroi latérale étagée.

5. Panneau à matrice de transistors à couche mince (100) selon la revendication 1, dans lequel une distance entre un bord du trou de contact (181, 182, 185, 186) et le trou traversant (176H) est égale ou supérieure à environ 3,0 microns.

6. Panneau à matrice de transistors à couche mince (100) selon la revendication 1, comprenant en outre une électrode de blindage (88) séparée de l'électrode de pixel (190) et chevauchant une partie des lignes de données (171) ou des lignes de grille (121).

7. Panneau à matrice de transistors à couche mince (100) selon la revendication 6, dans lequel l'électrode de pixel (190) et l'électrode de blindage (88) sont disposées sur la couche de passivation (180).

8. Panneau à matrice de transistors à couche mince (100) selon la revendication 6, comprenant en outre une électrode de stockage (137) chevauchant l'électrode de drain (175).

9. Panneau à matrice de transistors à couche mince (100) selon la revendication 8, dans lequel l'électrode de blindage (88) et l'électrode de stockage (137) sont alimentées sensiblement sous la même tension.

10. Panneau à matrice de transistors à couche mince (100) selon la revendication 9, dans lequel l'électrode de blindage (88) s'étend le long des lignes de données (171) ou des lignes de grille (121).

11. Panneau à matrice de transistors à couche mince (100) selon la revendication 10, dans lequel l'électrode de blindage (88) couvre totalement les lignes de données (171).

12. Panneau à matrice de transistors à couche mince (100) selon la revendication 1, dans lequel l'électrode de pixel (190) possède un coin biseauté.

13. Panneau à matrice de transistors à couche mince (100) selon la revendication 1, dans lequel la couche de passivation (180) contient un isolant organique.

14. Panneau à matrice de transistors à couche mince (100) selon la revendication 13, comprenant en outre un filtre coloré (230) disposé sur ou sous la couche de passivation (180).

15. Panneau à matrice de transistors à couche mince (100) selon la revendication 1, dans lequel l'électro-

de de pixel (190) comprend un élément de cloisonnement pour diviser l'électrode de pixel (190) en plusieurs compartiments.

16. Panneau à matrice de transistors à couche mince (100) selon la revendication 15, dans lequel l'élément de cloisonnement forme un angle d'environ 45 degrés avec les lignes de grille (121).

17. Méthode de fabrication d'un panneau à matrice de transistors à couche mince (100), laquelle méthode comprend :

la formation de lignes de grille (121) et d'électrodes capacitives (136) sur un substrat (110) ;
la formation d'une couche isolante de grille (140) couvrant les lignes de grille (121), l'électrode capacitive (136) et le substrat (110) ;
la formation de lignes de données (171) sur la couche isolante de grille (140) ;
la formation des transistors à couche mince (154), chacun de ces transistors à couche mince (154) comprenant une électrode de drain (175) et une électrode de couplage (176), formés sur la couche isolante de grille (140), l'électrode de couplage (176) étant connectée à l'électrode de drain (175) ;
la connexion de chacun des transistors à couche mince (154) respectivement à une des lignes de grille (121) et des lignes de données (171) ;
la formation d'une électrode de pixel (190) pour chacun des transistors à couche mince (154), les électrodes de pixel (190) comprenant une première électrode de sous-pixel (190a) et une deuxième électrode de sous-pixel (190b), la première électrode de sous-pixel (190a) étant connectée à l'électrode de drain (175) ;
caractérisée en ce que
chaque électrode de couplage (176) chevauche l'une des électrodes capacitives (136) et comprend un trou traversant (176H) ;
une couche de passivation (180) est disposée sur les lignes de données (171), l'électrode de drain (175) et l'électrode de couplage (176), la couche de passivation (180) ayant des trous de contact (181, 182, 185, 186) pénétrant dans les trous traversants (176H) pour exposer les électrodes capacitives (136) ; et **en ce que**
l'électrode de pixel (190) est formée sur la couche de passivation (180), et chacune des deuxièmes électrodes de sous-pixel (190b) est connectée à une électrode capacitive (136) correspondante à travers un trou de contact (181, 182, 185, 186).

18. Méthode selon la revendication 17, dans laquelle le trou traversant (176H) est substantiellement équidistant des deux bords opposés de l'électrode capacitive (136).

19. Méthode selon la revendication 17, dans laquelle le trou passant (176H) est rectangulaire, octogonal ou circulaire.

20. Méthode selon la revendication 17, dans laquelle le trou de contact (181, 182, 185, 186) possède une paroi latérale étagée.

FIG.1

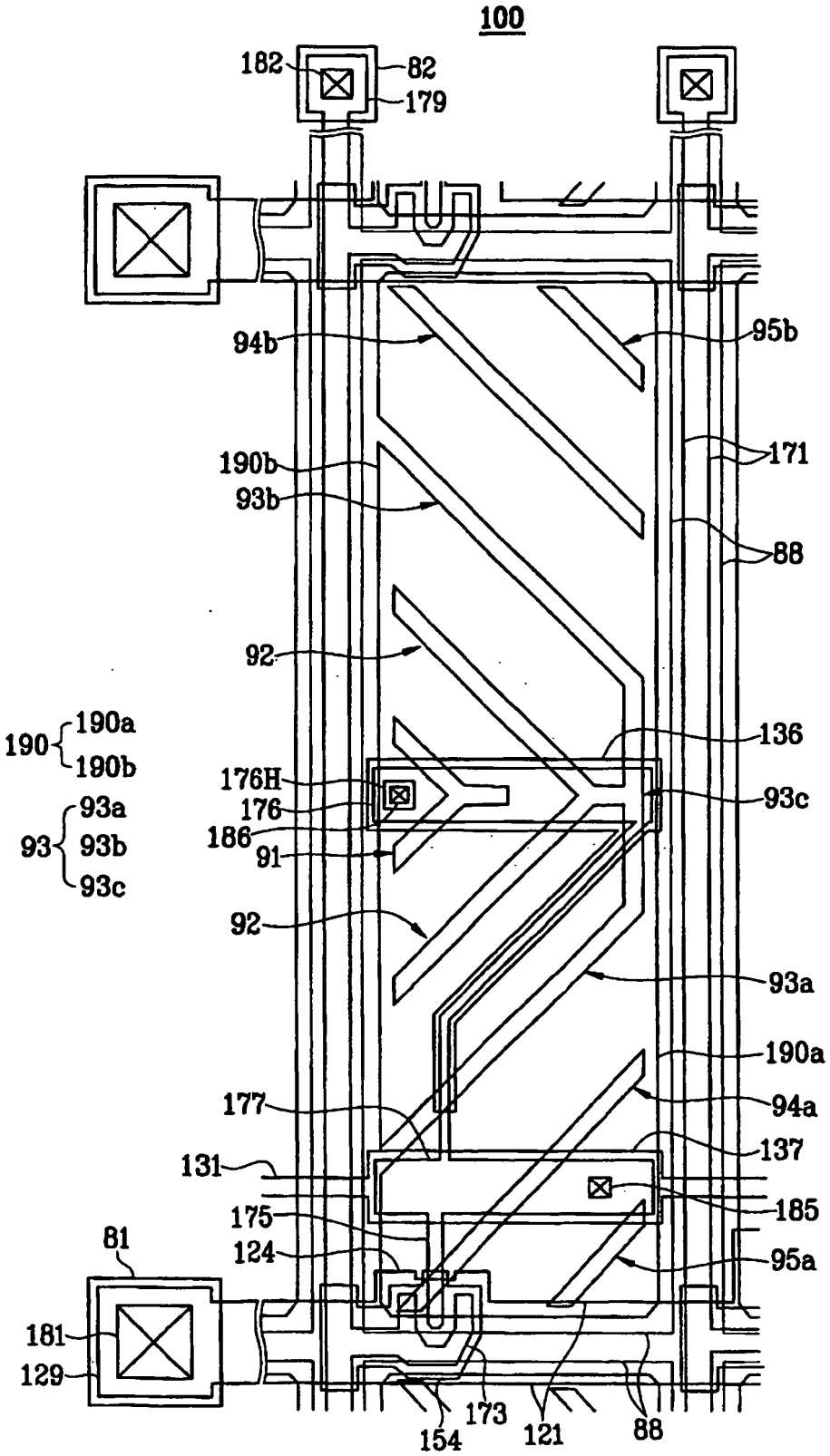

100
182
82
179
94b
95b
190b
171
93b
88
92
190
190a
190b
136
176H
93c
176
93
93a
93b
93c
186
91
92
93a
190a
177
94a
137
131
185
175
95a
124
81
181
129
173
154
121
88

FIG.2

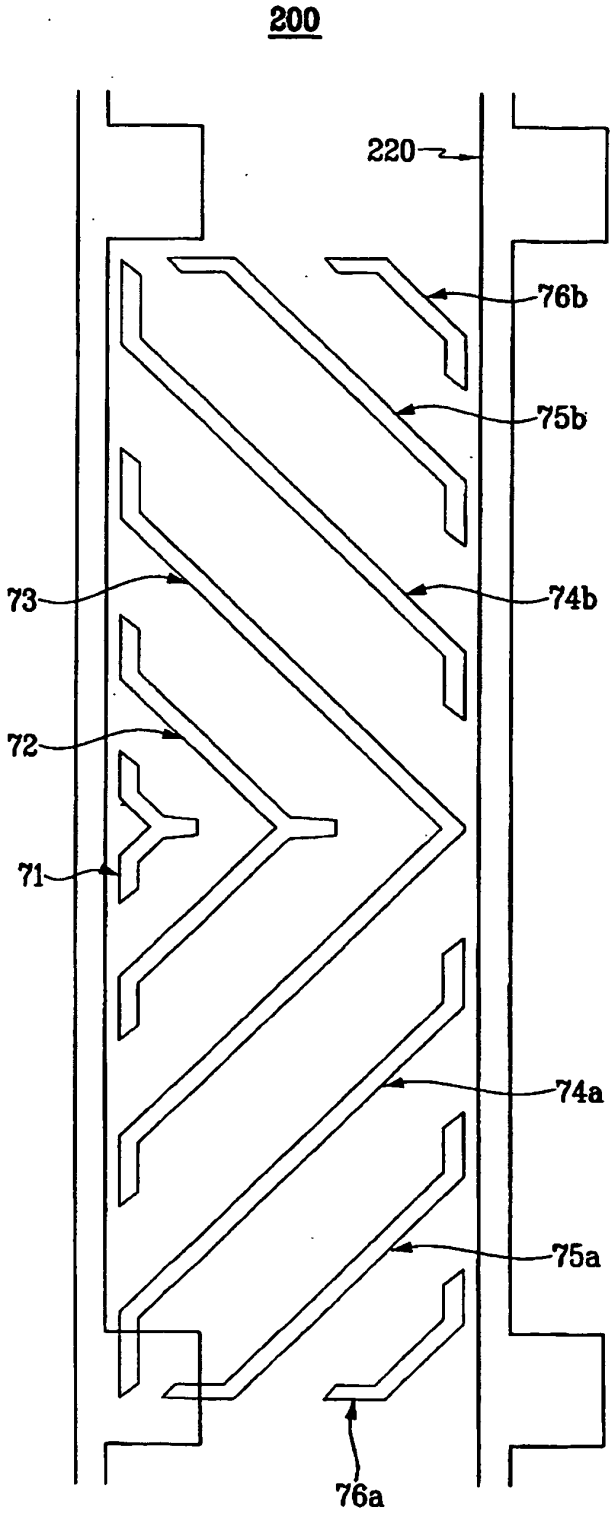


FIG.3

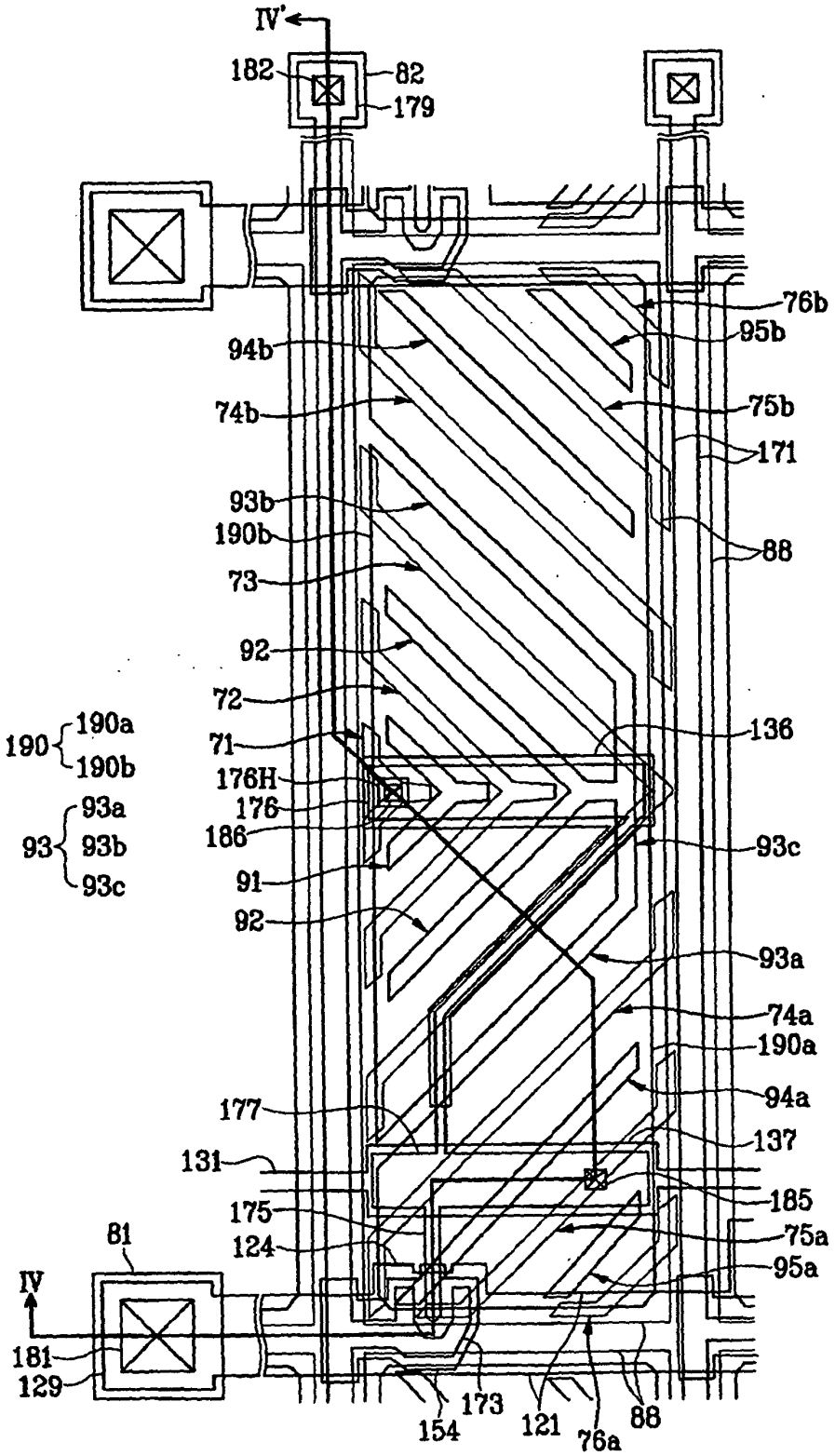

IV'
182
82
179
76b
95b
94b
74b
75b
171
93b
190b
88
73
92
72
190
190a
190b
71
136
176H
176
93
93a
93b
93c
186
91
92
93c
93a
74a
190a
94a
177
137
131
185
175
75a
124
95a
81
IV
181
129
173
154
121
76a
88

FIG.4

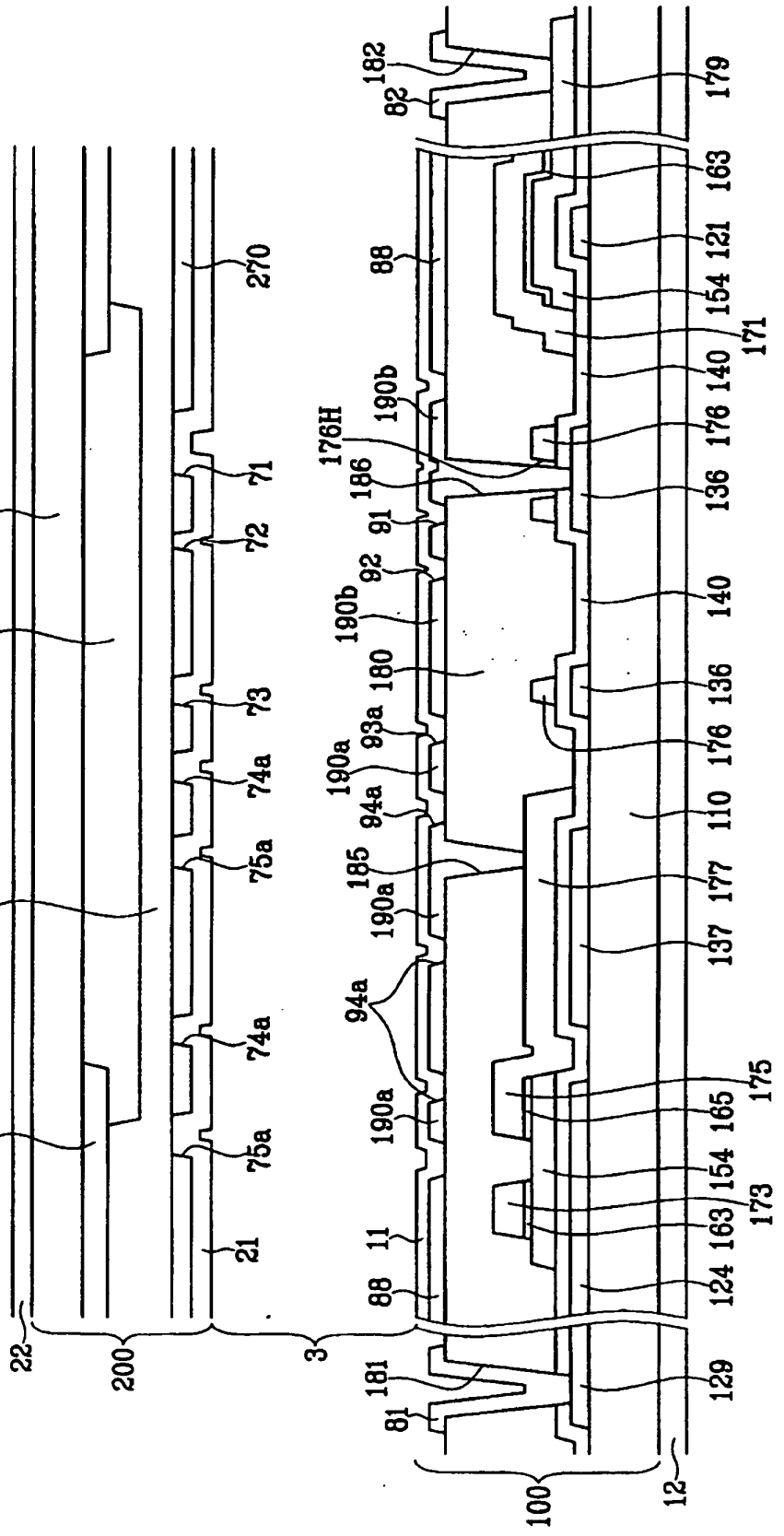

22
200
3
100
12
210
230
250
220
270
71
72
73
74a
75a
21
11
81
82
91
92
93a
94a
185
186
176H
180
190a
190b
88
181
182
179
163
121
154
171
140
176
136
110
177
137
165
175
173
124
129

FIG.5

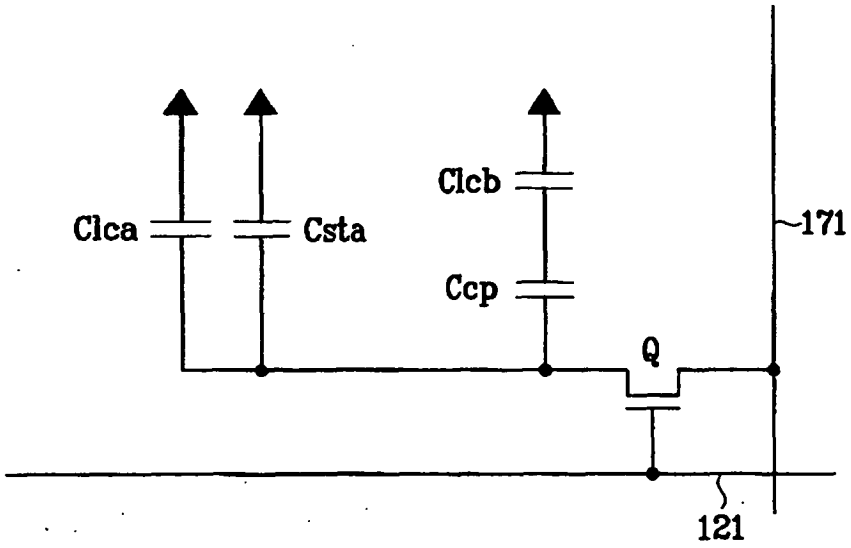


FIG.6

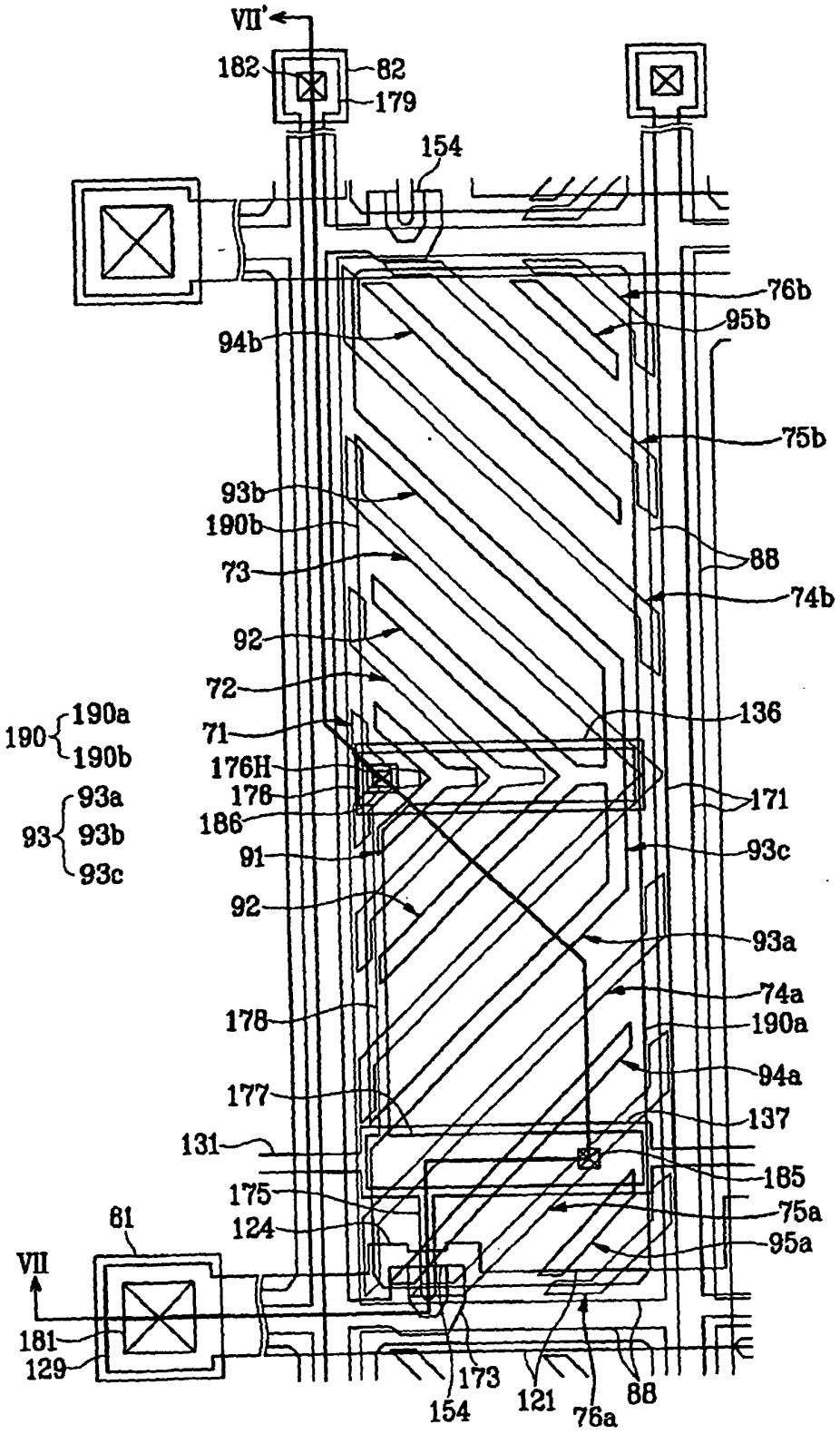

VII'
182
82
179
154
76b
95b
94b
75b
93b
190b
88
73
74b
92
72
190
190a
190b
71
136
176H
176
171
93
93a
93b
93c
186
91
93c
92
93a
74a
178
190a
94a
177
137
131
185
175
75a
124
95a
81
VII
181
129
173
154
121
76a
88

FIG.7

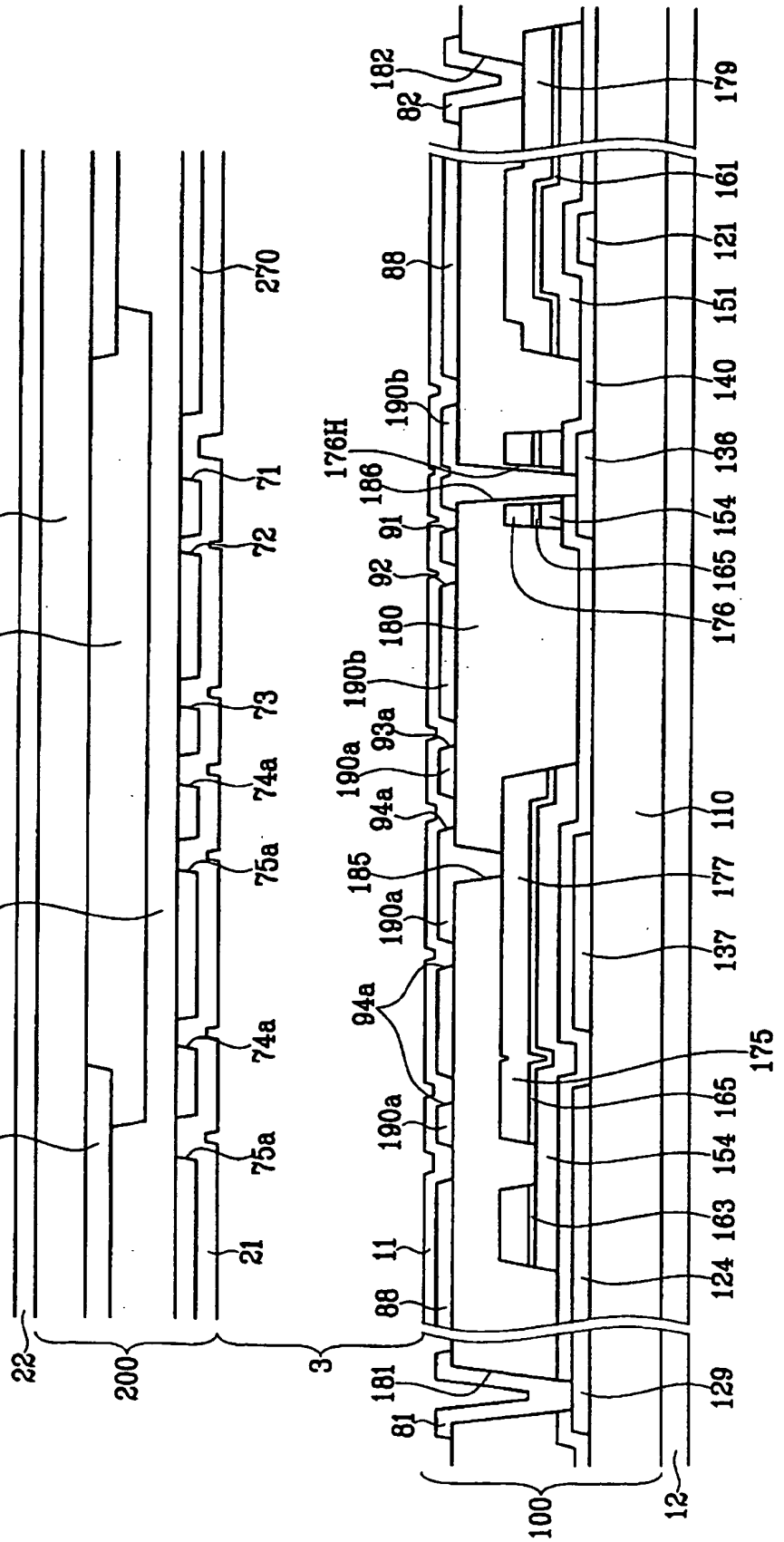
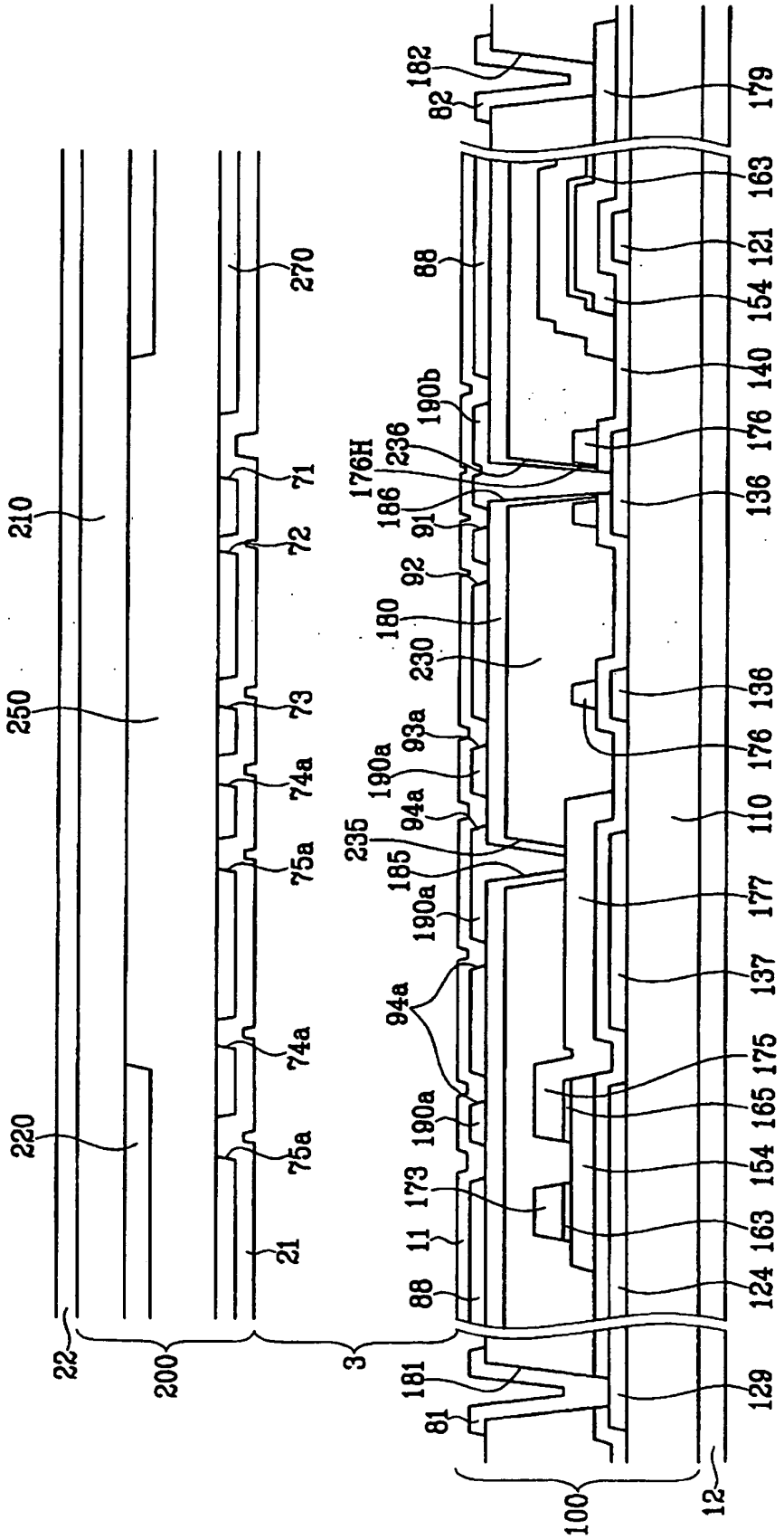

182
82
179
161
121
151
140
138
154
165
176
88
190b
176H
186
91
92
180
190b
93a
190a
94a
185
190a
94a
190a
190a
11
88
181
81
210
230
250
220
270
71
72
73
74a
75a
74a
75a
21
22
200
3
100
12
110
177
137
175
165
154
163
124
129

FIG.8


182
82
179
163
88
121
154
270
140
190b
176
236
176H
71
186
136
91
72
92
180
230
73
136
93a
190a
74a
176
94a
110
235
185
75a
190a
177
94a
137
74a
175
190a
165
75a
173
154
220
11
163
21
88
124
22
200
3
181
129
81
100
12

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- KR 1020040100915 **[0001]**
- US 5576858 A **[0003] [0003]**

专利名称(译)	用于液晶显示装置的薄膜晶体管阵列面板及其制造方法		
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当前申请(专利权)人(译)	SAMSUNG ELECTRONICS CO.，LTD.		
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IPC分类号	G02F1/139 G02F1/1362 G02F1/1343		
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代理机构(译)	韦策尔，WOLFGANG		
优先权	1020040100915 2004-12-03 KR		
其他公开文献	EP1666963A1		
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摘要(译)

薄膜晶体管阵列面板包括基板（110），设置在基板上的栅极线（121），以及设置在基板上并与栅极线分离的电容电极（136）。薄膜晶体管（154）包括与栅极线交叉的数据线（171），薄膜晶体管连接到栅极线和数据线并包括漏电极（175）和连接的耦合电极（176）漏电极与电容电极重叠，并且具有设置在电容电极上的通孔（176H）。薄膜晶体管包括设置在栅极线，数据线和薄膜晶体管上的钝化层（180），并且具有穿透通孔并暴露电容电极的接触孔（186），以及像素电极（190）包括连接到漏电极的第一子像素电极（190a）和通过接触孔连接到电容电极的第二子像素电极（190b）。