



(11) **EP 1 655 632 B1**

(12) **EUROPEAN PATENT SPECIFICATION**

(45) Date of publication and mention
of the grant of the patent:
02.03.2011 Bulletin 2011/09

(51) Int Cl.:
G02F 1/13 ^(2006.01) **G02F 1/1333** ^(2006.01)
G02F 1/1343 ^(2006.01)

(21) Application number: **05110301.8**

(22) Date of filing: **03.11.2005**

(54) **Thin film transistor array panel**

Dünnschichttransistoranordnungstafel

Panneau à réseau de transistors à couche mince

(84) Designated Contracting States:
DE FR GB

(30) Priority: **04.11.2004 KR 2004089246**

(43) Date of publication of application:
10.05.2006 Bulletin 2006/19

(73) Proprietor: **Samsung Electronics Co., Ltd.**
Suwon-si, Gyeonggi-Do (KR)

(72) Inventors:
• **Shin, Kyoung-Ju**
Yongin-si,
Gyeonggi-do (KR)
• **Park, Cheol-Woo**
Suwon-si,
Gyeonggi-do (KR)

• **Lyu, Jae-Jin**
Gwangju-gun,
Gyeonggi-do (KR)
• **Chai, Chong-Chul**
Mapo-gu,
Seoul (KR)

(74) Representative: **Modiano, Micaela Nadia et al**
Modiano Josif Pisanty & Staub Ltd
Thierschstrasse 11
80538 München (DE)

(56) References cited:
EP-A- 1 605 511 **WO-A-2004/029709**
US-A1- 2004 085 272 **US-A1- 2004 160 560**

Note: Within nine months of the publication of the mention of the grant of the European patent in the European Patent Bulletin, any person may give notice to the European Patent Office of opposition to that patent, in accordance with the Implementing Regulations. Notice of opposition shall not be deemed to have been filed until the opposition fee has been paid. (Art. 99(1) European Patent Convention).

EP 1 655 632 B1

Description

BACKGROUND OF THE INVENTION

(a) Field of the Invention

[0001] The present invention relates to a thin film transistor (TFT) array panel.

(b) Description of the Related Art

[0002] A liquid crystal display apparatus (hereinafter referred to as an LCD) is one of the most widely used flat panel displays. An LCD typically includes two panels provided with field-generating electrodes such as pixel electrodes and a common electrode and a liquid crystal (LC) layer interposed therebetween. The LCD displays images by applying voltages to the field-generating electrodes to generate an electric field in the LC layer, which determines orientations of LC molecules in the LC layer for adjusting polarization of the incident light.

[0003] One popular type of LCD, is the vertical alignment (VA) mode LCD, which aligns LC molecules such that the long axes of the LC molecules are perpendicular to the panels in the absence of an electric field. Much attention has been focused on the VA mode LCD because of its high contrast ratio and wide reference viewing angle.

[0004] Wide viewing angle of the VA mode LCD can be achieved via cutouts in the field-generating electrodes and protrusions on the field-generating electrodes. The cutouts and the protrusions affect the tilt directions of the LC molecules, e.g., the tilt directions can be distributed into several directions such that the reference viewing angle is widened. However, lateral visibility may not be improved in comparison to front visibility.

[0005] US 2004/085272 A1 discloses a multi-domain vertical alignment liquid crystal display in which a first and a second sub-pixel electrodes are respectively connected to the gate lines and the data lines, such that the first and the second sub-pixel electrodes receive the pixel signals from the different thin film transistors. Moreover, the arrangement shown is a drain electrode divided and extended into two portions each of which is connected to data lines.

US 2004/160560 A1 discloses liquid crystal display comprising first and second pixel electrodes placed on a first substrate, located opposite a data line and having a plurality of first cutouts. Moreover, a common electrode formed on a second substrate and having a plurality of second and third cutouts defines a plurality of domains along with the first cutouts and facing the first and the second pixel electrodes, respectively, wherein the second and the third cutouts have portions overlapping the data line and the overlapping portions of the second and the third cutouts are alternately arranged along the data line.

[0006] EP-A-1 605 511 discloses a TFT array panel

comprising a pixel electrode divided into a first sub-pixel electrode and a second sub-pixel electrode by an aperture. Sub-pixel electrode connects through contact hole to drain electrode and the sub-pixel electrode connects to an auxiliary coupling electrode through contact hole and auxiliary coupling electrode is coupled to coupling electrode to form a capacitor.

[0007] WO 2004/029709 A discloses a TFT array panel for use in an LCD device including a plurality of pixel electrodes each of which is connected to the first drain electrode through the contact hole and comprising a plurality of X-shaped cutouts and a plurality of linear cutouts. The X-shaped cutouts overlap the X-shaped portions of the direction control electrode (DCE) while the linear cutouts overlap the third and the fourth storage electrodes and. The DCE broadly overlaps peripheries of the cutouts as well as the cutouts themselves to form a storage capacitance along with the pixel electrode.

SUMMARY OF THE INVENTION

[0008] A thin film transistor (TFT) array panel for a Liquid Crystal Display apparatus (LCD) is provided according to the subject-matter of Claim 1.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009]

Fig. 1 is a layout view of a TFT array panel of an LCD according to an exemplary embodiment of the present invention;

Fig. 2 is a layout view of a common electrode panel of an LCD according to an exemplary embodiment of the present invention;

Fig. 3 is a layout view of an LCD including the TFT array panel shown in Fig. 1 and the common electrode panel shown in Fig. 2;

Fig. 4 is a sectional view of the LCD shown in Fig. 3 taken along line IV-IV';

Fig. 5 is an equivalent circuit diagram of the LCD shown in Figs. 1-4;

Fig. 6 is a layout view of an LCD according to an exemplary embodiment of the present invention;

Fig. 7 is a sectional view of the LCD shown in Fig. 6 taken along line VII-VII'; and

Fig. 8 is a sectional view of the LCD shown in Fig. 3 taken along line IV-IV' according to an exemplary embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0010] The exemplary embodiments of the present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. The present invention may, however, be embodied in many

different forms and should not be construed as limited to the embodiments set forth herein.

[0011] Like numerals refer to like elements throughout. It will be understood that when an element such as a layer, film, region or substrate is referred to as being "on" another element, it can be directly on the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly on" another element, there are no intervening elements present.

[0012] An LCD according to an exemplary embodiment of the present invention will be described in detail with reference to Figs. 1-5.

[0013] Fig. 1 is a layout view of a TFT array panel of the LCD, Fig. 2 is a layout view of a common electrode panel of an LCD, Fig. 3 is a layout view of the LCD including the TFT array panel shown in Fig. 1 and the common electrode panel shown in Fig. 2, Fig. 4 is a sectional view of the LCD shown in Fig. 3 taken along line IV-IV', and Fig. 5 is an equivalent circuit diagram of the LCD shown in Figs. 1-4.

[0014] Referring to Figs. 1-4, the LCD according to an exemplary embodiment of the present invention includes a TFT array panel 100, a common electrode panel 200, and a LC layer 3 interposed between the panels 100 and 200.

[0015] The TFT array panel 100 is now described in detail with reference Figs. 1, 3 and 4.

[0016] The TFT array panel 100 includes a plurality of gate conductors which include a plurality of gate lines 121, a plurality of storage electrode lines 131, and a plurality of capacitive electrodes 136 formed on an insulating substrate 110, such as a transparent glass or plastic substrate.

[0017] The gate lines 121 transmit gate signals and extend substantially in a transverse direction. Each gate line 121 includes a plurality of gate electrodes 124 projecting upwardly and an end portion 129 having an area for contact with another layer or external driving circuit. In addition, a gate driving circuit for generating gate signals may be mounted on a flexible printed circuit (FPC) film. The FPC film may either be attached to the substrate 110, directly mounted on the substrate 110, or integrated onto the substrate 110. The gate lines 121 may in turn be connected to the gate driving circuit on the substrate 110.

[0018] The storage electrodes 131 are supplied with a predetermined voltage and each of the storage electrodes 131 includes a pair of first and second stems 131a1 and 131a2 extend substantially parallel to the gate lines 121. Moreover, each of the storage electrode lines 131 are disposed between the gate lines 121, with the lower and the upper stems 131a1 and 131a2 being disposed in close proximity to the gate lines 121. The first and the second stems 131a1 and 131a2 include first and second storage electrodes 137a1 and 137a2, respectively, expanding in upward and downward directions, respectively. It is noted however that the storage elec-

trode lines 131 may have various shapes and arrangements.

[0019] Further, each of the capacitive electrodes 136 is rectangularly shaped and elongated parallel with respect to the gate lines 121. The capacitive electrodes 136 are separated from the gate lines 121 and the storage electrode lines 131. Moreover, each of the capacitive electrodes 136 is disposed between the pair of first and second storage electrodes 137a1 and 137a2 and are also substantially equidistant from the first and the second storage electrodes 137a1 and 137a2 and from the gate lines 121. In addition, each of the capacitive electrodes 136 also includes a funneled left end portion that has oblique or inclined edges which make about a 45 degrees angle with respect to the gate lines 121.

[0020] The gate conductors 121, 131 and 136 may be made of various metals or conductors. However, the gate conductors 121, 131 and 136 are preferably made of aluminum (Al) or an Al alloy, silver (Ag) or an Ag alloy, copper (Cu) or a Cu alloy, molybdenum (Mo) or a Mo alloy, chromium (Cr), Tantalum (Ta), or Titanium (Ti). In addition, the gate conductors 121, 131 and 136 may each have a multi-layered structure including two conductive films having different physical characteristics. In the above case, one of the two films is preferably made of a low resistivity metal, such as for example an Al containing metal, a Ag containing metal, or a Cu containing metal for reducing signal delay or voltage drop. The other film is preferably made of a material (e.g. a Mo containing metal, Cr, Ta, or Ti) which has good physical, chemical, and electrical contact characteristics with respect to indium tin oxide (ITO) or indium zinc oxide (IZO), such as for example Mo or Mo alloys, Cr, Ta or Ti. Examples of possible combinations for the two films include but are not limited to a lower Cr film and an upper Al (alloy) film and a lower Al (alloy) film and an upper Mo (alloy) film.

[0021] The lateral sides of the gate conductors 121, 131 and 136 are inclined relative to a surface of the substrate 110, with an inclination angle from about 30 to about 80 degrees.

[0022] Further, a gate insulating layer 140 preferably made of silicon nitride (SiN_x) or silicon oxide (SiO_x) is formed on the gate conductors 121, 131 and 136.

[0023] A plurality of semiconductor islands 154 preferably made of hydrogenated amorphous silicon (abbreviated to "a-Si") or polysilicon are formed on the gate insulating layer 140. The semiconductor islands 154 are disposed on the gate electrodes 124 and include extensions covering edges of the gate lines 121. A plurality of other semiconductor islands (not shown) may be disposed on the storage electrode lines 131.

[0024] A plurality of ohmic contact islands 163 and 165 are formed on the semiconductor islands 154. The ohmic contacts 163 and 165 are preferably made of n⁺ hydrogenated a-Si, which is heavily doped with n type impurity such as phosphorous. Alternatively, the ohmic contacts 163 and 165 may be made of silicide. The ohmic contacts 163 and 165 are located in pairs on the semiconductor

islands 154.

[0025] The lateral sides of the semiconductor islands 154 and the ohmic contacts 163 and 165 are inclined relative to the surface of the substrate 110, with an inclination angle preferably in a range of about 30 to about 80 degrees.

[0026] A plurality of data conductors including a plurality of data lines 171 and a plurality of drain electrodes 175 are formed on the ohmic contacts 163 and 165 and the gate insulating layer 140.

[0027] The data lines 171 transmit data signals and extend substantially in a longitudinal direction to intersect the gate lines 121 and the storage electrode lines 131. Each data line 171 includes a plurality of source electrodes 173 projecting toward the gate electrodes 124 and an end portion 179 having an area for contact with another layer or an external driving circuit. A data driving circuit for generating the data signals may be mounted on a FPC film. The FPC film may be attached to the substrate 110, directly mounted on the substrate 110, or integrated onto the substrate 110. The data lines 171 may in turn be connected to the driving circuit on the substrate 110.

[0028] Each of the drain electrodes 175 is separated from the data lines 171 and includes an end portion disposed opposite to the source electrodes 173. The end portion is partly enclosed by a source electrode 173 which is curved like the letter U of the alphabet.

[0029] Each drain electrode 175 further includes first, second, and central expansions 177a1, 177a2, and 176 and a pair of interconnections 178a1 and 178a2 connecting the expansions 177a1, 177a2, and 176. Each of the expansions 177a1, 177a2, and 176 are rectangularly shaped and are elongated parallel with respect to the gate lines 121. Interconnections 178a1 and 178a2 connect the expansions 177a1, 177a2, and 176 near left sides thereof and extend substantially parallel to the data lines 171,

[0030] The first and second expansions 177a1 and 177a2 overlap first and second storage electrodes 137a1 and 137a2, respectively.

[0031] The central expansion 176 overlaps a capacitive electrode 136 to form a "coupling electrode." The coupling electrode which includes central expansion 176 and capacitive electrode 136, further includes a through-hole 176H exposing a top surface of the gate insulating layer 140 near a left end portion of the coupling electrode. The through-hole 176H has substantially the same shape as the capacitive electrode 136.

[0032] A gate electrode 124, a source electrode 173, and a drain electrode 175 along with a semiconductor island 154 form a TFT having a channel formed in the semiconductor island 154 disposed between the source electrode 173 and the drain electrode 175.

[0033] The data conductors 171 and 175 may be made of various metals or conductors. However, the data conductors 171 and 175 are preferably made of refractory metal such as Cr, Mo, Ta, Ti, or alloys thereof. In addition,

the data conductors 171 and 175 may each have a multilayered structure including a refractory metal film and a low resistivity film. Examples of the multi-layered structure include but are not limited to a double-layered structure including a lower Cr/Mo (alloy) film and an upper Al (alloy) film or a triple-layered structure of a lower Mo (alloy) film, an intermediate Al (alloy) film, and an upper Mo (alloy) film. However, the data conductors 171 and 175 may be made of various metals or conductors.

[0034] The data conductors 171 and 175 have inclined edge profiles, with an inclination angle from about 30 to about 80 degrees.

[0035] The ohmic contacts 163 and 165 are interposed between the underlying semiconductor islands 154 and the overlying data conductors 171 and 175 thereon and reduce contact resistance therebetween. Extensions of the semiconductor islands 154 disposed on the edges of the gate lines 121 smooth the profile of the surface of these edges of the gate lines 121 to prevent the disconnection of the data lines 171 there. The semiconductor islands 154 include some exposed portions, which are not covered with the data conductors 171 and 175, such as portions located between the source electrodes 173 and the drain electrodes 175.

[0036] A passivation layer 180 is formed on the data conductors 171 and 175, and the exposed portions of the semiconductor islands 154. The passivation layer 180 is preferably made of an inorganic or an organic insulator and may also have a flat surface. Examples of the inorganic insulator include but are not limited to silicon nitride and silicon oxide. The organic insulator may be photosensitive. Moreover, the organic insulator preferably has dielectric constant less than about 4.0. Alternatively, the passivation layer 180 may include a lower film of inorganic insulator and an upper film of organic insulator such that it takes the excellent insulating characteristics of an organic insulator while preventing the exposed portions of the semiconductor islands 154 from being damaged by the organic insulator.

[0037] Additionally, the passivation layer 180 has a plurality of contact holes 182 exposing the end portions 179 of the data lines 171 and a plurality of contact holes 185a1 and 185a2 exposing the first and the second expansions 177a1 and 177a2 of the drain electrodes 175, respectively. The passivation layer 180 and the gate insulating layer 140 have a plurality of contact holes 181 exposing the end portions 129 of the gate lines 121 and a plurality of contact holes 186 penetrating the through-holes 176H and exposing the end portions of the capacitive electrodes 136. The contact holes 181, 182, 185a1, 185a2 and 186 may have inclined or stepped sidewalls.

[0038] A plurality of pixel electrodes 190, a shielding electrode 88, and a plurality of contact assistants 81 and 82 are also formed on the passivation layer 180. They are preferably made of a transparent conductor such as ITO or IZO or reflective conductor such as Ag, Al, Cr, or alloys thereof.

[0039] Each pixel electrode 190 is rectangularly

shaped or substantially rectangularly shaped and has chamfered corners. The chamfered edges of the pixel electrode 190 make an angle of about 45 degrees with the gate lines 121. The pixel electrodes 190 overlap the gate lines 121 to increase the aperture ratio.

[0040] In addition, each of the pixel electrodes 190 has first and second gaps 93a and 93b that divide the pixel electrode 190 into first, second, and central sub-pixel electrodes 190a1, 190a2 and 190b, respectively. The first and the second gaps 93a and 93b obliquely extend from a left edge to a right edge of the pixel electrode 190 such that the central sub-pixel electrode 190b resembles an isosceles trapezoid rotated at a right angle with respect to the gate lines 121 and the first and the second sub-pixel electrodes 190a1 and 190a2 resemble right-angled trapezoids rotated at a right angle with respect to the gate lines 121. The first and the second gaps 93a and 93b are perpendicular to each other and make an angle of about 45 degrees with respect to the gate lines 121.

[0041] The first and the second sub-pixel electrodes 190a1 and 190a2 are connected to the first and the second expansions 177a1 and 177a2 of the drain electrodes 175 through contact holes 185a1 and 185a2, respectively.

[0042] The central sub-pixel electrode 190b is connected to a capacitive electrode 136 through a contact hole 186 and overlaps a coupling electrode 176. The central sub-pixel electrode 190b, the capacitive electrode 136, and the coupling electrode 176 form a "coupling capacitor."

[0043] The central sub-pixel electrode 190b has central cutouts 91 and 92, the first sub-pixel electrode 190a1 has first cutouts 94a and 95a, and the second sub-pixel electrode 190a2 has second cutouts 94b and 95b. The cutouts 91, 92 and 94a-95b partition the sub-pixel electrodes 190b, 190a1 and 190a2 into a plurality of partitions. The pixel electrode 190 having the cutouts 91, 92 and 94a-95b and the gaps 93a and 93b (also referred to as cutouts hereinafter) substantially has an inversion symmetry with respect to a capacitive electrode 136.

[0044] Each of the first and the second cutouts 94a-95b obliquely or slantingly extends to a right edge of the pixel electrode 190 from a left corner, a lower edge, or an upper edge of the pixel electrode 190. The first and the second cutouts 94a-95b extend substantially perpendicular to each other and make an angle of about 45 degrees with respect to the gate lines 121.

[0045] Each of the center cutouts 91 and 92 includes a transverse portion and a pair of oblique portions connected thereto. The transverse portion extends along the capacitive electrode 136, and the oblique portions obliquely or slantingly extends from the transverse portion toward the left edge of the pixel electrode 190 parallel to the first and the second cutouts 94a-95b, respectively. The center cutout 91 overlaps the funneled end portion of the coupling electrode 176 and the capacitive electrode 136.

[0046] The number of cutouts or the number of partitions may be varied depending on the design factors such as the size of the pixel electrode 190, the ratio of the transverse edges and the longitudinal edges of the pixel electrode 190, the type and characteristics of the liquid crystal layer 3, etc.

[0047] The shielding electrode 88 is supplied with common voltage and it includes longitudinal portions extending along the data lines 171 and transverse portions extending along the gate lines 127 to connect adjacent longitudinal portions. The longitudinal portions fully or substantially cover the data lines 171 entirely, while each of the transverse portions lies within the boundary of the gate line 121.

[0048] The shielding electrode 88 blocks electromagnetic interference between the data lines 171 and the pixel electrodes 190 and between the data lines 171 and the common electrode 270 to reduce the distortion of the voltage of the pixel electrodes 190 and the signal delay of the data voltages carried by the data lines 171.

[0049] The contact assistants 81 and 82 are connected to the end portions 129 of the gate lines 121 and the end portions 179 of the data lines 171 through the contact holes 181 and 182, respectively. The contact assistants 81 and 82 protect the end portions 129 and 179 and enhance the adhesion between the end portions 129 and 179 and external devices.

[0050] The description of the common electrode panel 200 follows with reference to Figs. 2-4.

[0051] A light blocking member 220, also referred to as a black matrix herein, for preventing light leakage is formed on an insulating substrate 210, such as for example a transparent glass or plastic substrate. The light blocking member 220 includes a plurality of rectilinear portions facing the data lines 171 on the TFT array panel 100 and a plurality of widened portions facing the TFTs on the TFT array panel 100. Also, the light blocking member 220 may have a plurality of through-holes that face the pixel electrodes 190. In addition, the light blocking member 220 may have substantially the same shape (e.g. planar shape) as the pixel electrodes 190.

[0052] A plurality of color filters 230 are also formed on the substrate 210 and they are disposed substantially in the areas enclosed by the light blocking member 220.

The color filters 230 may extend in a longitudinal direction substantially along the pixel electrodes 190. The color filters 230 may each represent one of the primary colors such as red, green and blue colors.

[0053] An overcoat 250 is formed on the color filters 230 and the light blocking member 220. The overcoat 250 is preferably made of an (organic) insulator and it prevents the color filters 230 from being exposed and also provides a flat surface.

[0054] A common electrode 270 is formed on the overcoat 250. The common electrode 270 is preferably made of transparent conductive material such as ITO and IZO and has a plurality of cutout sets 71, 72, 73, 74a, 74b, 75a, 75b, 76a and 76b.

[0055] Cutout sets 71-76b face a pixel electrode 190 and include center cutouts 71, 72 and 73, first cutout 74a, 75a and 76a and second cutouts 74b, 75b and 76b. Cutout 71 is disposed near the contact hole 186, while each of the other cutouts 72-76b of the set are disposed between adjacent cutouts 91-95b of the pixel electrode 190. Alternatively, each of the cutouts 72-76b may be disposed between a cutout 95a or 95b and a chamfered edge of the pixel electrode 190. In addition, each of the cutouts 71-76b has at least an oblique portion extending parallel to the first cutout 93a-95a or the second cutout 93b-95b of the pixel electrode 190. Moreover, each of the oblique portions of the cutouts 72-75b has a depressed notch and the cutouts 71-76b have substantially an inversion symmetry with respect to a capacitive electrode 136.

[0056] Each of the first and the second cutouts 74a-76b includes an oblique portion and a pair of transverse and a pair of longitudinal portions. The oblique portion extends to a right edge of the pixel electrode 190 from either a left edge, a lower edge, or an upper edge of the pixel electrode 190. The transverse and longitudinal portions extend from respective ends of the oblique portion along edges of the pixel electrode 190, overlapping the edges of the pixel electrode 190, and making obtuse angles with respect to the oblique portion.

[0057] Each of the center cutouts 71 and 72 includes a central transverse portion, a pair of oblique portions, and a pair of terminal longitudinal portions. The center cutout 73 includes a pair of oblique portions and a pair of terminal longitudinal portions. The central transverse portion is disposed near the left edge or the center of the pixel electrode 190 and extends along the capacitive electrode 136. The oblique portions of the center cutout 73 extend from an end of the central transverse portion or from the center of the right edge of the pixel electrode 190, located to the left edge of the pixel electrode. The oblique portions of the cutouts 71 and 72 make oblique angles with respect to the central transverse portion. The terminal longitudinal portions extend from the ends of the respective oblique portions along the left edge of the pixel electrode 190, overlapping the left edge of the pixel electrode 190, and make obtuse angles with respect to the respective oblique portions.

[0058] The number of cutouts 71-76b may be also varied depending on the design factors. The light blocking member 220 preferably overlaps the cutouts 71-76b to block the light leakage through the cutouts 71-76b.

[0059] Alignment layers 11 and 21 may be homeotropic and are coated on inner surfaces of the panels 100 and 200. Polarizers 12 and 22 are provided on outer surfaces of the panels 100 and 200 so that their polarization axes may be crossed and one of the polarization axes may be parallel to the gate lines 121. One of the polarizers 12 and 22 may be omitted when the LCD is a reflective LCD.

[0060] The LCD may further include at least one retardation film for compensating the retardation of the LC

layer 3. The retardation film has birefringence and gives a retardation opposite to that given by the LC layer 3.

[0061] The LCD may further include a backlight unit supplying light to the LC layer 3 through the polarizers 12 and 22, the retardation film, and the panels 100 and 200.

[0062] It is preferable that the LC layer 3 is in a state of negative dielectric anisotropy. In addition, it is also preferable that the LC layer 3 have been subjected to a vertical alignment in that the LC molecules in the LC layer 3 are aligned such that their long axes are substantially vertical to the surfaces of the panels 100 and 200 in the absence of an electric field. Accordingly, incident light cannot pass the crossed polarization system 12 and 22.

[0063] Opaque members such as the storage electrode lines 131, the expansions 177a1, 177a2 and 176, the interconnections 178a1 and 178a2 of the drain electrodes 175, and the transparent members such as the pixel electrodes 190 having the cutouts 91-95b and 71-76b are symmetrically arranged with respect to the capacitive electrodes 136. Also, since the interconnections 178a1 and 178a2 are disposed near the edges of the pixel electrodes 190, they do not decrease the light transmissive areas, but rather block the texture generated near the light transmissive areas.

[0064] The LCD according to an exemplary embodiment of the present invention and shown in Figs. 1-4 is represented as an equivalent circuit shown in Fig. 5.

[0065] Referring to Fig. 5, a pixel of the LCD includes a TFT Q, a first subpixel unit including a first LC capacitor (C_{LCa}) and a storage capacitor (C_{ST}), a second subpixel unit including a second LC capacitor (C_{LCb}), and a coupling capacitor (C_{cp}).

[0066] The first LC capacitor C_{LCa} includes first and second sub-pixel electrodes 190a1 and 190a2 as one terminal, a portion of the common electrode 270 corresponding thereto as the other terminal, and a portion of the LC layer 3 disposed therebetween as a dielectric. Similarly, the second LC capacitor C_{LCb} includes a central sub-pixel electrode 190b as one terminal, a portion of the common electrode 270 corresponding thereto as the other terminal, and a portion of the LC layer 3 disposed thereon as a dielectric.

[0067] The storage capacitor C_{ST} includes first and second expansions 177a1 and 177a2 of a drain electrode 175 as one terminal, first and second storage electrodes 137a1 and 137a2 as the other terminal, and a portion of the gate insulating layer 140 disposed therebetween as a dielectric. The coupling capacitor C_{cp} includes a central sub-pixel electrode 190b and a capacitive electrode 136 as one terminal, a coupling electrode 176 as the other terminal, and portions of the passivation layer 180 and the gate insulating layer 140 disposed therebetween as a dielectric.

[0068] The first LC capacitor C_{LCa} and the storage capacitor C_{ST} are connected in parallel to a drain of the TFT Q. The coupling capacitor C_{cp} is connected between the drain of the TFT Q and the second LC capacitor C_{LCb} .

The common electrode 270 is supplied with a common voltage V_{com} and the storage electrode lines 131 may be supplied with the common voltage V_{com} .

[0069] The TFT Q applies data voltages from data line 171 to the first LC capacitor C_{LCa} and the coupling capacitor C_{cp} in response to a gate signal from gate line 121. The coupling capacitor C_{cp} transmits the data voltage with a modified magnitude to the second LC capacitor C_{LCb} .

[0070] When the storage electrode line 131 is supplied with the common voltage V_{com} , the voltage V_b charged across the second LC capacitor C_{LCb} is given by:

$$V_b = V_a \times [C_{cp} / (C_{cp} + C_{LCb})],$$

where V_a denotes the voltage of the first LC capacitor C_{LCa} .

[0071] Since the term $C_{cp} / (C_{cp} + C_{LCb})$ is smaller than one, the voltage V_b of the second LC capacitor C_{LCb} is greater than that of the first LC capacitor C_{LCa} . The above inequality may also occur in the situation wherein the voltage of the storage electrode line 131 does not equal the common voltage V_{com} .

[0072] When the potential difference is generated across the first LC capacitor C_{LCa} or the second LC capacitor C_{LCb} , an electric field substantially perpendicular to the surfaces of the panels 100 and 200 is generated in the LC layer 3. Both the pixel electrode 190 and the common electrode 270 are commonly referred to as field generating electrodes hereinafter. Then, the LC molecules in the LC layer 3 tilt in response to the electric field such that their long axes are perpendicular to the field direction. The degree of the tilt of the LC molecules determines the variation of the polarization of light incident on the LC layer 3. In turn, the variation of the light polarization is transformed into the variation of the light transmittance by the polarizers 12 and 22. In this way, the LCD displays images.

[0073] The tilt angle of the LC molecules depends on the strength of the electric field. Since the voltage V_a of the first LC capacitor C_{LCa} and the voltage V_b of the second LC capacitor C_{LCb} are different from each other, the tilt direction of the LC molecules in the first subpixel unit is different from that in the second subpixel unit and thus the luminances of the two subpixels units are different. Thus, by maintaining the average luminance of the two subpixels units in a target luminance, the voltages V_a and V_b of the first and the second subpixels units can be adjusted so that an image viewed from a lateral side is closer to an image viewed from the front, thereby improving the lateral visibility.

[0074] The ratio of the voltages V_a and V_b can be adjusted by varying the capacitance of the coupling capacitor C_{cp} . Moreover, the coupling capacitance C_{cp} can be varied by changing the overlapping area and distance between the coupling electrode 176 and the central sub-

pixel electrode 190b (and the capacitive electrode 136). For example, the distance between the coupling electrode 176 and the central sub-pixel electrode 190b becomes large when the capacitive electrode 136 is removed and the coupling electrode 176 is moved to the position of the capacitive electrode 136. Preferably, the voltage V_b of the second LC capacitor C_{LCb} is from about 0.6 to about 0.8 times the voltage V_a of the first LC capacitor C_{LCa} .

[0075] The voltage V_b charged in the second LC capacitor C_{LCb} may be larger than the voltage V_a of the first LC capacitor C_{LCa} . This is achieved by precharging the second LC capacitor C_{LCb} with a predetermined voltage such as the common voltage V_{com} .

[0076] The ratio between the lower and the first subpixel second 190a1 and 190a2 of the first subpixel unit and the central sub-pixel electrode 190b of the second subpixel unit is preferably from about 1:0.85 to about 1:1.15. In addition, the number of the sub-pixel electrodes in each of the LC capacitors C_{LCa} and C_{LCb} may be changed.

[0077] The tilt direction of the LC molecules is determined by a horizontal component generated by the cutouts 91-95b and 71-76b of the field generating electrodes 190 and 270 and the oblique edges of the pixel electrodes 190 distorting the electric field. The electric field being perpendicular or at least substantially perpendicular to the edges of cutouts 91-95b and 71-76b and the oblique edges of the pixel electrodes 190. Referring to Fig. 3, a set of the cutouts 91-95b and 71-76b divides a pixel electrode 190 into a plurality of sub-areas and each sub-area has two major edges. Since the LC molecules on each sub-area tilt perpendicular to the major edges, the azimuthal distribution of the tilt directions are localized to four directions, thereby increasing the reference viewing angle of the LCD.

[0078] In addition, when the areas that can transmit light for the above-described four tilt directions are the same, the visibility improves for various viewing directions. Since the opaque members are symmetrically arranged as described above, the adjustment of the transmissive areas is relatively simple.

[0079] The notches in the cutouts 72-75b help determine the tilt directions of the LC molecules on the cutouts 72-75b. Notches may also be provided in cutouts 91-95b and may have various shapes and arrangements.

[0080] The shapes and the arrangements of the cutouts 91-95b and 71-76b for determining the tilt directions of the LC molecules may be modified and at least one of the cutouts 91-95b and 71-76b can be substituted with protrusions or depressions. The protrusions are preferably made of organic or inorganic material and disposed on or under the field-generating electrodes 190 or 270.

[0081] Further, since there is no electric field between the shielding electrode 88 and the common electrode 270, the LC molecules on the shielding electrode 88 remain in their initial orientations and thus the light incident thereon is blocked. In the above situation, the shielding

electrode 88 may serve as a light blocking member and the light blocking member 220 may thus be omitted.

[0082] An LCD according to an exemplary embodiment of the present invention will be described in detail with reference to Figs. 6 and 7.

[0083] Fig. 6 is a layout view of an LCD according to another exemplary embodiment of the present invention, and Fig. 7 is a sectional view of the LCD shown in Fig. 6 taken along line VII-VII'.

[0084] Referring to Figs. 6 and 7, the LCD includes a TFT array panel 100, a common electrode panel 200, a LC layer 3 interposed between the panels 100 and 200, and a pair of polarizers 12 and 22 attached on outer surfaces of the panels 100 and 200.

[0085] Layered structures of the panels 100 and 200 according to this exemplary embodiment are virtually the same as those shown in Figs. 1-4.

[0086] Regarding the TFT array panel 100, a plurality of gate lines 121 including gate electrodes 124 and end portions 129, a plurality of storage electrode lines 131 including stems 131a1 and 131a2 and storage electrodes 137a1 and 137a2, and a plurality of capacitive electrodes 136 are formed on a substrate 110. A gate insulating layer 140, a plurality of semiconductors 154, and a plurality of ohmic contacts 163 and 165 are sequentially formed on the gate lines 121 and the storage electrodes lines 131. A plurality of data lines 171 including source electrodes 173 and end portions 179 and a plurality of drain electrodes 175 including expansions 177a1, 177a2 and 176 and interconnections 178a1 and 178a2 are formed on the ohmic contacts 163 and 165. A passivation layer 180 is formed on the data lines 171, the drain electrodes 175, and exposed portions of the semiconductors 154. A plurality of contact holes 181, 182, 185a1, 185a2 and 186 are provided at the passivation layer 180 and the gate insulating layer 140. The contact holes 186 pass through through-holes 176H provided at the expansions 176 of the drain electrodes 175. Additionally, a plurality of pixel electrodes 190 including subpixel electrodes 190a1, 190a2 and 190b with cutouts 91-95b, a shielding electrode 88, and a plurality of contact assistants 81 and 82 are formed on the passivation layer 180, with an alignment layer 11 being coated thereon.

[0087] Regarding the common electrode panel 200, a light blocking member 220, a plurality of color filters 230, an overcoat 250, a common electrode 270 having cutouts 71-76b, and an alignment layer 21 are formed on an insulating substrate 210.

[0088] In contrast to the LCD shown in Figs. 1-4, the semiconductors 154 and the ohmic contacts 163 of the TFT array panel 100 according to this exemplary embodiment extend along the data lines 171 to form semiconductor stripes 151 and ohmic contact stripes 161. In addition, the semiconductor stripes 151 have substantially the same shapes (e.g. planar shapes) as the data lines 171 and the drain electrodes 175, as well as the underlying ohmic contacts 163 and 165. Moreover, the semiconductors 154 include some exposed portions, which

are not covered with the data lines 171 and the drain electrodes 175, such as portions located between the source electrodes 173 and the drain electrodes 175.

[0089] A manufacturing method of the TFT array panel according to an exemplary embodiment simultaneously forms the data lines 171 and the drain electrodes 175, the semiconductors 151, and the ohmic contacts 161 and 165 using one photolithography step.

[0090] A photoresist masking pattern for the photolithography process has position-dependent thickness, and in particular, it has thicker portions and thinner portions. The thicker portions are located on wire areas that will be occupied by the data lines 171 and the drain electrodes 175, and the thinner portions are located on channel areas of TFTs.

[0091] The position-dependent thickness of the photoresist may be obtained using several techniques. For example, by providing translucent areas on the exposure mask as well as transparent areas and light blocking opaque areas. The translucent areas may have a slit pattern, a lattice pattern, a thin film(s) with intermediate transmittance or intermediate thickness. When using a slit pattern, it is preferable that the width of the slits or the distance between the slits is smaller than the resolution of a light exposer used for the photolithography. Another example is to use reflowable photoresist. For instance, once a photoresist pattern made of a reflowable material is formed using only a normal exposure mask to have transparent areas and opaque areas. The above photoresist pattern is then subjected to a reflow process without use of a photoresist to form certain thin portions of the TFT array panel.

[0092] Thus, the above manufacturing process is simpler than conventional processes due to the omission of the photolithography step.

[0093] Many of the above-described features of the LCD shown in Figs. 1-4 may be appropriate to the LCD shown in Figs. 6 and 7.

[0094] An LCD according to another exemplary embodiment of the present invention will be described in detail with reference to Fig. 8.

[0095] Fig. 8 is an sectional view of the LCD shown in Fig. 3 taken along line IV-IV'.

[0096] Referring to Fig. 8, the LCD includes a TFT array panel 100, a common electrode panel 200, a LC layer 3 interposed between the panels 100 and 200, and a pair of polarizers 12 and 22 attached on outer surfaces of the panels 100 and 200.

[0097] Layered structures of the panels 100 and 200 according to this exemplary embodiment are virtually the same as those shown in Figs. 1-4.

[0098] Regarding the TFT array panel 100, a plurality of gate lines 121 including gate electrodes 124 and end portions 129, a plurality of storage electrode lines 131 including stems 131a1 and 131a2 and storage electrodes 137a1 and 137a2, and a plurality of capacitive electrodes 136 are formed on a substrate 110. A gate insulating layer 140, a plurality of semiconductors 154, and a plu-

ality of ohmic contacts 163 and 165 are sequentially formed on the gate lines 121 and the storage electrodes lines 131. A plurality of data lines 171 including source electrodes 173 and end portions 179 and a plurality of drain electrodes 175 including expansions 177a1, 177a2 and 176 and interconnections 178a1 and 178a2 are formed on the ohmic contacts 163 and 165 and the gate insulating layer 140. A passivation layer 180 is formed on the data lines 171, the drain electrodes 175, and exposed portions of the semiconductors 154. A plurality of contact holes 181, 182, 185a1, 185a2 and 186 are provided at the passivation layer 180 and the gate insulating layer 140. The contact holes 186 pass through through-holes 176H provided at the expansions 176 of the drain electrodes 175. Also, a plurality of pixel electrodes 190 including subpixel electrodes 190a1, 190a2 and 190b and having cutouts 91-95b, a shielding electrode 88, and a plurality of contact assistants 81 and 82 are formed on the passivation layer 180 with an alignment layer 11 being coated thereon.

[0099] Regarding the common electrode panel 200, a light blocking member 220, an overcoat 250, a common electrode 270 having cutouts 71-76b, and an alignment layer 21 are formed on an insulating substrate 210.

[0100] In contrast to the LCD shown in Figs. 1-4, the TFT array panel 100 includes a plurality of color filters 230 disposed under the passivation layer 180, while the common electrode panel 200 has no color filter. In this case, the overcoat 250 may be removed from the common electrode panel 200.

[0101] The color filters 230 are disposed between two adjacent data lines 171 and they have a plurality of through-holes 235 and 236 through which the contact holes 185 and 186 pass through, respectively. The color filters 230 are not provided on peripheral areas of the end portions 129 and 179 of the signal lines 121 and 171.

[0102] The color filters 230 may extend along a longitudinal direction to form stripes. The color filters 230 may overlap each other to block light leakage between the pixel electrodes 190, or alternatively may be spaced apart from each other. When the color filters 230 overlap each other, linear portions of the light blocking member 220 may be omitted and in this case, the shielding electrode 88 may cover edges of the color filters 230. Overlapping portions of the color filters 230 may also have a reduced thickness to decrease the height difference between the overlapping portions.

[0103] The color filters 230 may be disposed on the passivation layer 180, or the passivation layer 180 may be omitted.

[0104] Many of the above-described features of the LCD shown in Figs. 1-4 are also appropriate for the LCD shown in Fig. 8.

[0105] Having described the exemplary embodiments of the present invention, it is further noted that it is readily apparent to those of reasonable skill on the art that various modifications can be made without departing from the scope of the present invention which is defined by

the metes and bounds of the appended claims.

[0106] Where technical features mentioned in any claim are followed by reference signs, those reference signs have been included for the sole purpose of increasing the intelligibility of the claims and accordingly such reference signs do not have any limiting effect on the scope of each element identified by way of example by such reference signs.

Claims

1. A thin film transistor array panel (100) for a Liquid Crystal Display apparatus (LCD) comprising:

a plurality of gate lines (121);
 a data line (171) intersecting the plurality of gate lines (121);
 a thin film transistor (100) connected to at least one of the gate lines (121) and the data line (171) and including a drain electrode (175); and
 a pixel electrode (190), **characterized in that** said pixel electrode (190) includes a first and a second gap (93a, 93b) dividing the pixel electrode (190) into first, second and central subpixel electrodes (190a1, 190a2, 190b) respectively, said first and second subpixel electrodes (190a1, 190a2) forming at least one first subpixel electrode subpixel electrode unit (190a1, 190a2) connected to the drain electrode (175) of the thin film transistor (100), said central subpixel electrode (190b) forming a second subpixel electrode (190b) unit capacitively coupled to the at least one first subpixel electrode (190a1, 190a2) unit and said first subpixel electrode unit and second subpixel electrodes (190a1, 190a2, 190b) having portions which do not overlap the drain electrode (175) and are disposed substantially symmetrical to a reference line equidistant from the gate lines (121).

2. The thin film array panel of claim 1, wherein the drain electrode (175) comprises first and second portions (177a1, 177a2) connected to the first and the second subpixel electrodes (190a1, 190a2) respectively, and disposed substantially symmetrical to the reference line.
3. The thin film array panel of claim 2, further comprising first and second storage electrodes (137a1, 137a2) overlapping the first and the second portions (177a1, 177a2) of the drain electrode (175), respectively.
4. The thin film array panel of claim 3, wherein the subpixel electrode unit and the second storage electrodes (137a1, 137a2) are disposed substantially symmetrical to the reference line.

5. The thin film array panel of claim 2, wherein the first and the second subpixel electrodes (190a1, 190a2) are disposed opposite to each other with respect to the second subpixel electrode (190b) unit.
6. The thin film array panel of claim 2, wherein the first and the second subpixel electrodes (190a1, 190a2) are disposed substantially symmetrical to the reference line.
7. The thin film array panel of claim 2, wherein the drain electrode (175) comprises an interconnection (178a1, 178a2) connecting the first portion and the second portion (177a1, 177a2).
8. The thin film array panel of claim 7, wherein the interconnection (178a1, 178a2) is disposed adjacent to the data line (171) and substantially parallel to the data line (171).
9. The thin film array panel of claim 2, wherein the drain electrode (175) further comprises a coupling electrode (136, 176) overlapping the second subpixel electrode (190b) unit.
10. The thin film array panel of claim 9, further comprising a capacitive electrode (136) connected to the second subpixel electrode (190b) unit and overlapping the coupling electrode (136, 176).
11. The thin film array panel of claim 10, wherein the coupling electrode (136, 176) or the capacitive electrode (136) is disposed substantially symmetrical to the reference line.
12. The thin film array panel of claim 10, wherein the coupling electrode (136, 176) has a through-hole (176H) and the capacitive electrode (136) and the second subpixel electrode (190b) unit are connected to each other through the through-hole (176H).
13. The thin film array panel of claim 1, further comprising a shielding electrode (88) separated from the pixel electrode (190) and overlapping the data line (171) at least in part.
14. The thin film array panel of claim 13, wherein the pixel electrode (190) and the shielding electrode (88) comprise the same layer.
15. The thin film array panel of claim 13, wherein the shielding electrode (88) extends along the data line (171) or the gate lines (121).
16. The thin film array panel of claim 15, wherein the shielding electrode (88) substantially covers the entire data line (171).

17. The thin film array panel of claim 1, further comprising a shielding electrode (88) separated from the pixel electrode (190) and overlapping the gate line (121) at least in part.

18. The thin film array panel of claim 1, wherein said plurality of gate lines (121) comprises gate electrodes (124) and end portions (129), the thin film array panel further comprising:

a plurality of storage electrode lines (131), a plurality of storage electrodes (137a1, 137a2), and a plurality of capacitive electrodes (136) disposed on a TFT panel substrate (110);
a plurality of said data lines (171) having source electrodes (173) and end portions (179) and which intersect the plurality of gate lines (121), a plurality of said thin film transistors having a plurality of said drain electrodes (175), said plurality of thin film transistors (100) being connected to each of the plurality of gate lines (121) and data lines said plurality of drain electrodes (175) each having a plurality of expansions (177a1, 177a2, 176) and a plurality of interconnections (178a1, 178a2);
a plurality of said pixel electrodes (190), each of said sub-pixels having a plurality of cutouts (91, 92, 93a, 93b, 94a, 94b, 95a, 95b, 71, 72, 73, 74a, 74b, 75a, 76b), each of said pixel electrodes (190) overlap said gate lines (121), said cutouts partition each of the sub-pixel electrodes into a plurality of partitions, wherein said storage electrode lines (131), said expansions (177a1, 177a2, 176) and said interconnections (178a1, 178a2) of the drain electrodes (175), and said plurality of pixel electrodes (190) having said gaps (93a, 93b) are symmetrically arranged with respect to the capacitive electrodes (136).

19. The thin film transistor array panel (100) of claim 18, further comprising a plurality of color filters (230) operatively connected to said thin film transistor (100) array panel (100).

20. The thin film transistor array panel (100) of claim 19, wherein each of the plurality of color filters (230) represent one of the following colors comprising red, green or blue.

Patentansprüche

1. Ein Dünnschicht-Transistor-Matrix-Panel (100) für eine Flüssigkristallanzeige (LCD), das Folgendes umfasst:

eine Vielzahl von Gate-Leitungen (121),
eine Datenleitung (171), die die Vielzahl von Ga-

- te-Leitungen (121) schneidet,
einen Dünnschicht-Transistor (100), der mit
mindestens einer der Gate-Leitungen (121) und
der Datenleitung (171) verbunden ist und eine
Drain-Elektrode (175) einschließt, und
eine Pixelelektrode (190), **dadurch gekennzeichnet, dass** die Pixelelektrode (190) eine erste und eine zweite Lücke (93a, 93b) einschließt, welche die Pixelelektrode (190) in erste, zweite beziehungsweise mittlere Subpixel-
elektroden (190a1, 190a2, 190b) unterteilen, wobei die ersten und zweiten Subpixelelektroden (190a1, 190a2) mindestens eine erste Subpixel-
elektroden-Einheit (190a1, 190a2) bilden, die mit der Drain-Elektrode (175) des Dünnschicht-
Transistors (100) verbunden ist, wobei die mittlere Subpixelelektrode (190b) eine zweite Sub-
pixelelektroden-Einheit (190b) bildet, die kapazitiv mit der mindestens einen ersten Subpixel-
elektroden-Einheit (190a1, 190a2) gekoppelt ist, und wobei die erste Subpixelelektroden-Einheit und die zweiten Subpixelelektroden (190a1, 190a2, 190b) Abschnitte haben, welche nicht mit der Drain-Elektrode (175) überlappend sind und im Wesentlichen symmetrisch zu einer Referenzlinie angeordnet sind, die äquidistant von den Gate-Leitungen (121) ist.
2. Das Dünnschicht-Transistor-Matrix-Panel gemäß Anspruch 1, worin die Drain-Elektrode (175) erste und zweite Abschnitte (177a1, 177a2) umfasst, die mit den ersten beziehungsweise den zweiten Subpixelelektroden (190a1, 190a2) verbunden sind und im Wesentlichen symmetrisch zur Referenzlinie angeordnet sind.
 3. Das Dünnschicht-Transistor-Matrix-Panel gemäß Anspruch 2, das weiter erste und zweite Speicherelektroden (137a1, 137a2) umfasst, die mit den ersten beziehungsweise den zweiten Abschnitten (177a1, 177a2) der Drain-Elektrode (175) überlappend sind.
 4. Das Dünnschicht-Transistor-Matrix-Panel gemäß Anspruch 3, worin die ersten und die zweiten Speicherelektroden (137a1, 137a2) im Wesentlichen symmetrisch zur Referenzlinie angeordnet sind.
 5. Das Dünnschicht-Transistor-Matrix-Panel gemäß Anspruch 2, worin die ersten und die zweiten Subpixelelektroden (190a1, 190a2) einander gegenüberliegend mit Bezug auf die zweite Subpixelelektroden-Einheit (190b) angeordnet sind.
 6. Das Dünnschicht-Transistor-Matrix-Panel gemäß Anspruch 2, worin die ersten und die zweiten Subpixelelektroden (190a1, 190a2) im Wesentlichen symmetrisch zur Referenzlinie angeordnet sind.
 7. Das Dünnschicht-Transistor-Matrix-Panel gemäß Anspruch 2, worin die Drain-Elektrode (175) eine Querverbindung (178a1, 178a2) umfasst, welche mit dem ersten Abschnitt und dem zweiten Abschnitt (177a1, 177a2) verbunden ist.
 8. Das Dünnschicht-Transistor-Matrix-Panel gemäß Anspruch 7, worin die Querverbindung (178a1, 178a2) angrenzend an die Datenleitung (171) und im Wesentlichen parallel zur Datenleitung (171) angeordnet ist.
 9. Das Dünnschicht-Transistor-Matrix-Panel gemäß Anspruch 2, worin die Drain-Elektrode (175) weiter eine Kopplungselektrode (136, 176) umfasst, die mit der zweiten Subpixelelektroden-Einheit (190b) überlappend ist.
 10. Das Dünnschicht-Transistor-Matrix-Panel gemäß Anspruch 9, das weiter eine kapazitive Elektrode (136) umfasst, welche mit der zweiten Subpixelelektroden-Einheit (190b) verbunden ist und welche mit der Kopplungselektrode (136, 176) überlappend ist.
 11. Das Dünnschicht-Transistor-Matrix-Panel gemäß Anspruch 10, worin die Kopplungselektrode (136, 176) oder die kapazitive Elektrode (136) im Wesentlichen symmetrisch zur Referenzlinie angeordnet sind.
 12. Das Dünnschicht-Transistor-Matrix-Panel gemäß Anspruch 10, worin die Kopplungselektrode (136, 176) ein durchgehendes Loch (176H) hat und worin die kapazitive Elektrode (136) und die zweite Subpixelelektroden-Einheit (190b) durch das durchgehende Loch (176H) miteinander verbunden sind.
 13. Das Dünnschicht-Transistor-Matrix-Panel gemäß Anspruch 1, das weiter eine Abschirmelektrode (88) umfasst, welche von der Pixelelektrode (190) getrennt ist und zumindest teilweise mit der Datenleitung (171) überlappend ist.
 14. Das Dünnschicht-Transistor-Matrix-Panel gemäß Anspruch 13, worin die Pixelelektrode (190) und die Abschirmelektrode (88) dieselbe Schicht umfassen.
 15. Das Dünnschicht-Transistor-Matrix-Panel gemäß Anspruch 13, worin die Abschirmelektrode (88) sich entlang der Datenleitung (171) oder den Gate-Leitungen (121) erstreckt.
 16. Das Dünnschicht-Transistor-Matrix-Panel gemäß Anspruch 15, worin die Abschirmelektrode (88) im Wesentlichen die gesamte Datenleitung (171) bedeckt.
 17. Das Dünnschicht-Transistor-Matrix-Panel gemäß

Anspruch 1, das weiter eine Abschirmelektrode (88) umfasst, welche von der Pixelelektrode (190) getrennt ist und welche zumindest teilweise mit der Gate-Leitung (121) überlappend ist.

18. Das Dünnschicht-Transistor-Matrix-Panel gemäß Anspruch 1, worin die Vielzahl von Gate-Leitungen (121) Gate-Elektroden (124) und Endabschnitte (129) umfasst, wobei das Dünnschicht-Transistor-Matrix-Panel weiter Folgendes umfasst:

eine Vielzahl von Speicherelektrodenleitungen (131), eine Vielzahl von Speicherelektroden (137a1, 137a2) und eine Vielzahl kapazitiver Elektroden (136), die auf einem TFT-Panet-Substrat (110) angeordnet sind,
eine Vielzahl der Datenleitungen (171), die SourceElektroden (173) und Endabschnitte (179) haben und die Vielzahl von Gate-Leitungen (121) schneiden,
eine Vielzahl der Dünnschicht-Transistoren, die eine Vielzahl der Drain-Elektroden (175) haben, wobei die Vielzahl von Dünnschicht-Transistoren (100) mit jeder der Vielzahl von Gate-Leitungen (121) und Datenleitungen (171) verbunden ist, wobei jeder der Vielzahl von Drain-Elektroden (175) eine Vielzahl von Erweiterungen (177a1, 177a2, 176) und eine Vielzahl von Querverbindungen (178a1, 178a2) hat,
eine Vielzahl der Pixelelektroden (190), wobei jeder der Subpixel eine Vielzahl von Ausschnitten (91, 92, 93a, 93b, 94a, 94b, 95a, 95b, 71, 72, 73, 74a, 74b, 75a, 76b) hat und jede der Pixelelektroden (190) mit den Gate-Leitungen (121) überlappend ist, wobei die Ausschnitte jede der Subpixelelektroden in eine Vielzahl von Abschnitten unterteilen, wobei die Speicherelektrodenleitungen (131), die Erweiterungen (177a1, 177a2, 176) und die Querverbindungen (178a1, 178a2) der Drain-Elektroden (175) und die Vielzahl von Pixelelektroden (190) mit den Lücken (93a, 93b) symmetrisch zu den kapazitiven Elektroden (136) angeordnet sind.

19. Das Dünnschicht-Transistor-Matrix-Panel (100) gemäß Anspruch 18, das weiter eine Vielzahl von Farbfiltern (230) umfasst, welche operativ mit dem Dünnschicht-Transistor-(100)-Matrix-Panel (100) verbunden sind.

20. Das Dünnschicht-Transistoranordnungstafel (100) gemäß Anspruch 19, worin jeder der Vielzahl von Farbfiltern (230) eine der folgenden Farben darstellt, die Rot, Grün oder Blau umfassen.

Revendications

1. Panneau à réseau de transistors à couche mince (100) pour un dispositif d'Affichage à Cristaux Liquides (LCD), comprenant :

une pluralité de lignes de grille (121),
une ligne de données (171) coupant la pluralité de lignes de grille (121) ;
un transistor à couche mince (100), connecté à au moins l'une des lignes de grille (121) et des lignes de données (171) et comprenant une électrode de drain (175) ; et
une électrode de pixel (190), **caractérisé en ce que** ladite électrode de pixel (190) comprend un premier et un deuxième intervalle (93a, 93b) divisant l'électrode de pixel (190) en des première, deuxième électrodes de sous-pixel (190a1, 190a2) et électrode de sous-pixel centrale (190b), respectivement, lesdites première et deuxième électrodes de sous-pixel (190a1, 190a2) formant au moins une première unité d'électrode de sous-pixel (190a1, 190a2) connectée à l'électrode de drain (175) du transistor à couche mince (100), ladite électrode de sous-pixel centrale (190b) formant une deuxième unité d'électrode de sous-pixel (190b), couplée capacitivement à la au moins une première unité d'électrode de sous-pixel (190a1, 190a2), et ladite première unité d'électrode de sous-pixel et deuxièmes électrodes de sous-pixel (190a1, 190a2, 190b) ayant des parties ne chevauchant pas l'électrode de drain (175) et sont disposées sensiblement symétriquement à une ligne de référence équidistante des lignes de grille (121).

2. Panneau à réseau à couche mince selon la revendication 1, dans lequel l'électrode de drain (175) comprend des première et deuxième parties (177a1, 177a2) connectées aux première et deuxième électrodes de sous-pixel (190a1, 190a2), respectivement, et disposées sensiblement symétriquement à la ligne de référence.

3. Panneau à réseau à couche mince selon la revendication 2, comprenant en outre comprend des première et deuxième électrodes de stockage (137a1, 137a2) chevauchant les première et deuxième parties (177a1, 177a2) de l'électrode de drain (175), respectivement.

4. Panneau à réseau à couche mince selon la revendication 3, dans lequel les première et deuxième électrodes de stockage (137a1, 137a2) sont disposées sensiblement symétriquement à la ligne de référence.

5. Panneau à réseau à couche mince selon la reven-

- dication 2, dans lequel les première et deuxième électrodes de sous-pixel (190a1, 190a2) sont disposées à l'opposé de chaque autre par rapport à la deuxième unité d'électrode de sous-pixel (190b).
6. Panneau à réseau à couche mince selon la revendication 2, dans lequel les première et deuxième électrodes de sous-pixel (190a1, 190a2) sont disposées sensiblement symétriquement à la ligne de référence.
7. Panneau à réseau à couche mince selon la revendication 2, dans lequel l'électrode de drain (175) comprend une interconnexion (178a1, 178a2) connectant les première et deuxième parties (177a1, 177a2).
8. Panneau à réseau à couche mince selon la revendication 7, dans lequel l'interconnexion (178a1, 178a2) est disposée de manière adjacente à la ligne de données (171) et sensiblement parallèlement à la ligne de données (171).
9. Panneau à réseau à couche mince selon la revendication 29, dans lequel l'électrode de drain (175) comprend en outre une électrode de couplage (136, 176) chevauchant la deuxième unité d'électrode de sous-pixel (190b).
10. Panneau à réseau à couche mince selon la revendication 9, comprenant en outre une électrode capacitive (136), connectée à la deuxième unité d'électrode de sous-pixel (190b) et chevauchant l'électrode de couplage (136, 176).
11. Panneau à réseau à couche mince selon la revendication 10, dans lequel l'électrode de couplage (136, 176) ou l'électrode capacitive (136) est disposée sensiblement symétriquement à la ligne de référence.
12. Panneau à réseau à couche mince selon la revendication 10, dans lequel l'électrode de couplage (136, 176) présente un trou traversant (176H) et l'électrode capacitive (136) et la deuxième unité d'électrode de sous-pixel (190b) sont connectées à chaque autre par le trou traversant (176H).
13. Panneau à réseau à couche mince selon la revendication 1, comprenant en outre une électrode de blindage (88), séparée de l'électrode de pixel (190) et chevauchant au moins en partie la ligne de données (171).
14. Panneau à réseau à couche mince selon la revendication 13, dans lequel l'électrode de pixel (190) et l'électrode de blindage (88) comprennent la même couche.
15. Panneau à réseau à couche mince selon la revendication 13, dans lequel électrode de blindage (88) s'étend le long de la ligne de données (171) ou des lignes de grille (121).
16. Panneau à réseau à couche mince selon la revendication 15, dans lequel l'électrode de blindage (88) couvre pratiquement la totalité de la ligne de données (171).
17. Panneau à réseau à couche mince selon la revendication 1, comprenant en outre une électrode de blindage (88), séparée de l'électrode de pixel (190) et chevauchant au moins en partie la ligne de grille (121).
18. Panneau à réseau à couche mince selon la revendication 1, dans lequel ladite pluralité de lignes de grille (121) comprend des électrodes de grille (124) et des parties d'extrémité (129), le panneau à réseau à couche mince comprenant en outre :
- une pluralité de lignes d'électrode de stockage (131), une pluralité d'électrodes de stockage (137a1, 137a2), et une pluralité d'électrodes capacitives (136), disposées sur un substrat de panneau TFT (110) ;
- une pluralité desdites lignes de données (171) ayant des électrodes de source (173) et des parties d'extrémité (179) et coupant la pluralité de lignes de données (121),
- une pluralité desdits transistors à couche mince comprenant une pluralité desdites électrodes de drain (175), ladite pluralité de transistors à couche mince (100) étant connectée à chacune de la pluralité de lignes de grille (121) et de lignes de données (171), ladite pluralité d'électrodes de drain (175) comprenant chacune une pluralité d'extensions (177a1, 177a2, 176) et une pluralité d'interconnexions (178a1, 178a2);
- une pluralité desdites électrodes de pixel (190), chacun desdits sous-pixels ayant une pluralité de découpages (91, 92, 93a, 93b, 94a, 95a, 95b, 71, 72, 73, 74a, 75a, 76b), chacune desdites électrodes de pixel (190) chevauchant lesdites lignes de grille (121), lesdites découpages subdivisant chacune desdites électrodes de sous-pixel en une pluralité de partitions, dans lequel lesdites lignes d'électrode de stockage (131), lesdites extensions (177a1, 177a2, 176) et lesdites interconnexions (178a1, 178a2) des électrodes de drain (175), et ladite pluralité d'électrodes de pixel (190) ayant lesdits intervalles (93a, 93b) sont agencés symétriquement par rapport aux électrodes capacitives (136).
19. Panneau à réseau de transistors à couche mince (100) selon la revendication 18, comprenant en outre

une pluralité de filtre de couleur (230), connectés fonctionnellement audit panneau à réseau (100) de transistors à couche mince (100).

- 20.** Panneau à réseau de transistors à couche mince (100) selon la revendication 198, dans lequel chacun de la pluralité des filtres de couleur (230) représente l'une des couleurs suivantes, comprenant le rouge, le vert ou le bleu.

5

10

15

20

25

30

35

40

45

50

55

FIG.1

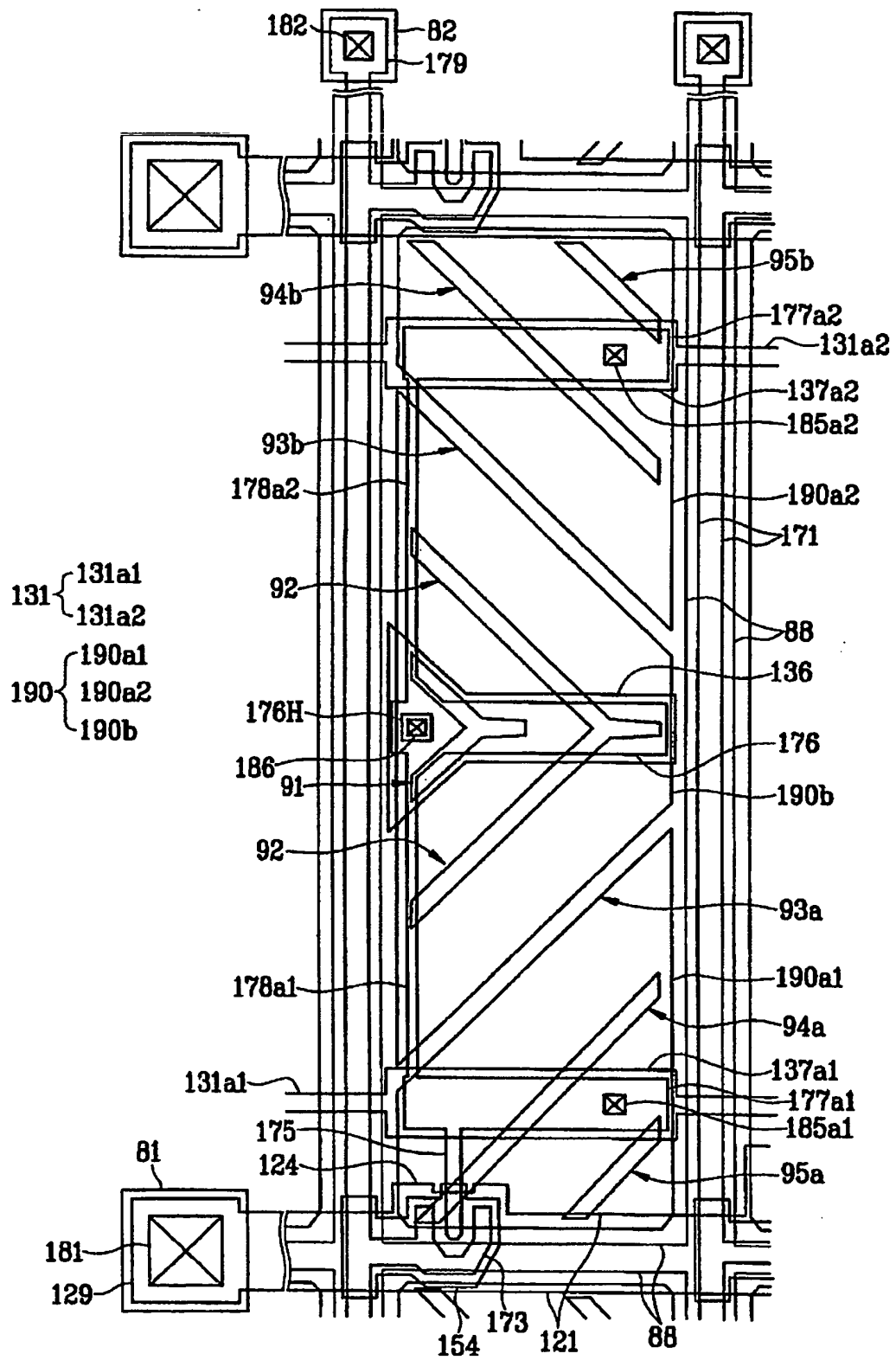


FIG. 2

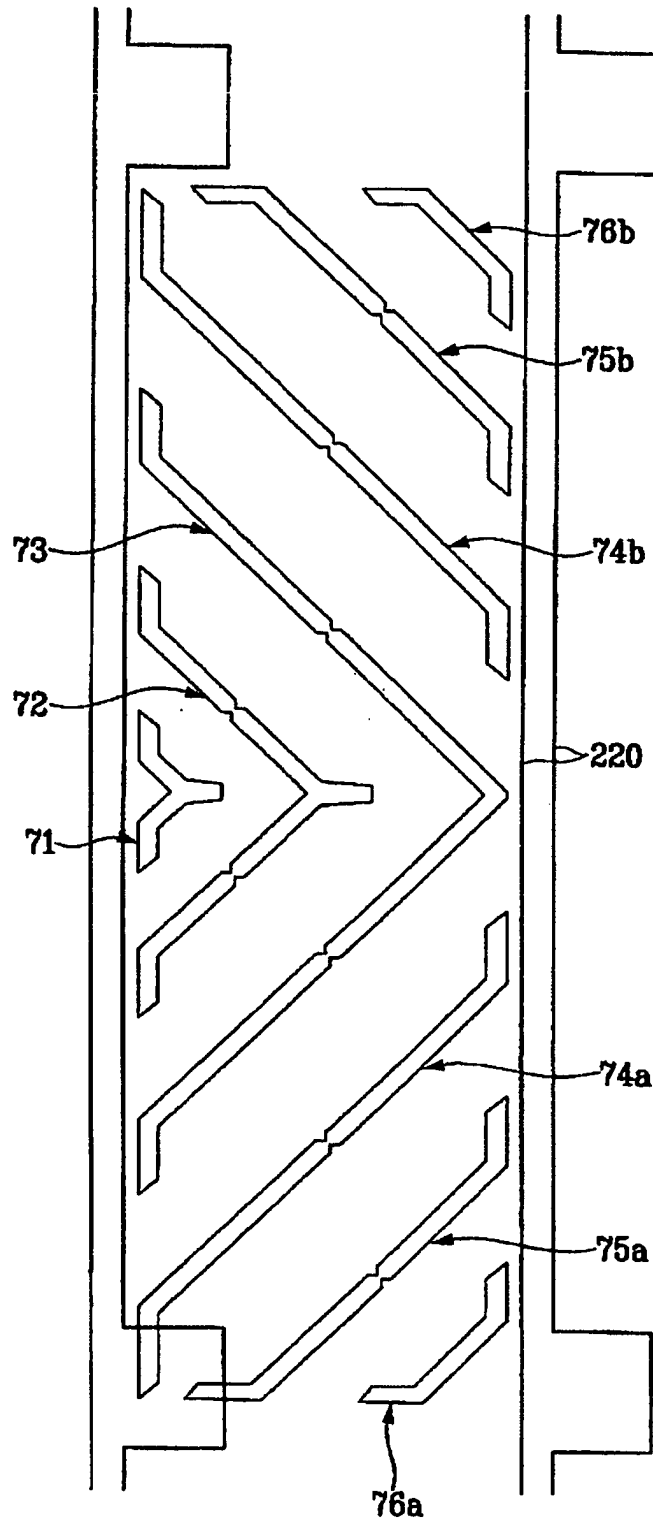


FIG.3

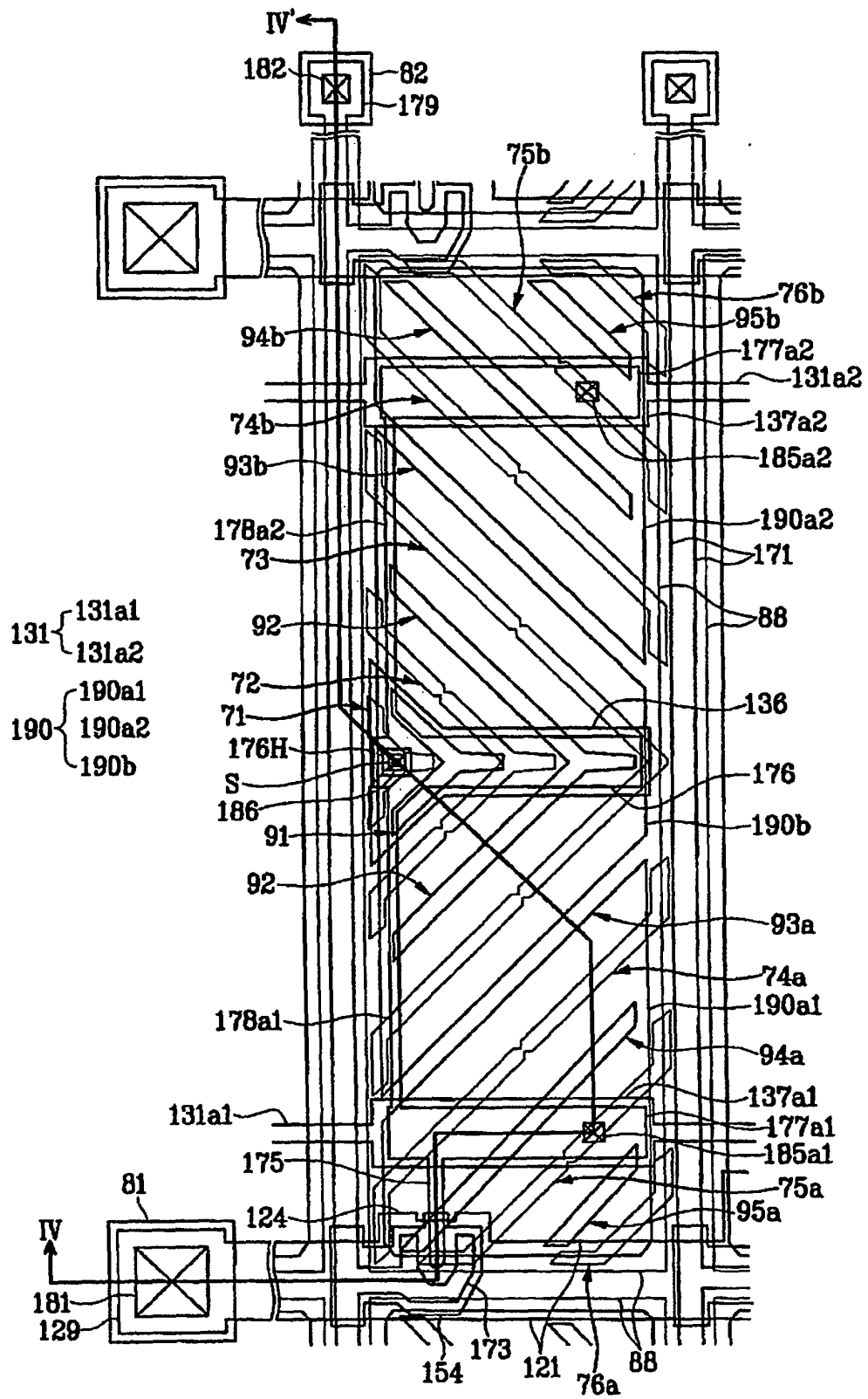


FIG. 4

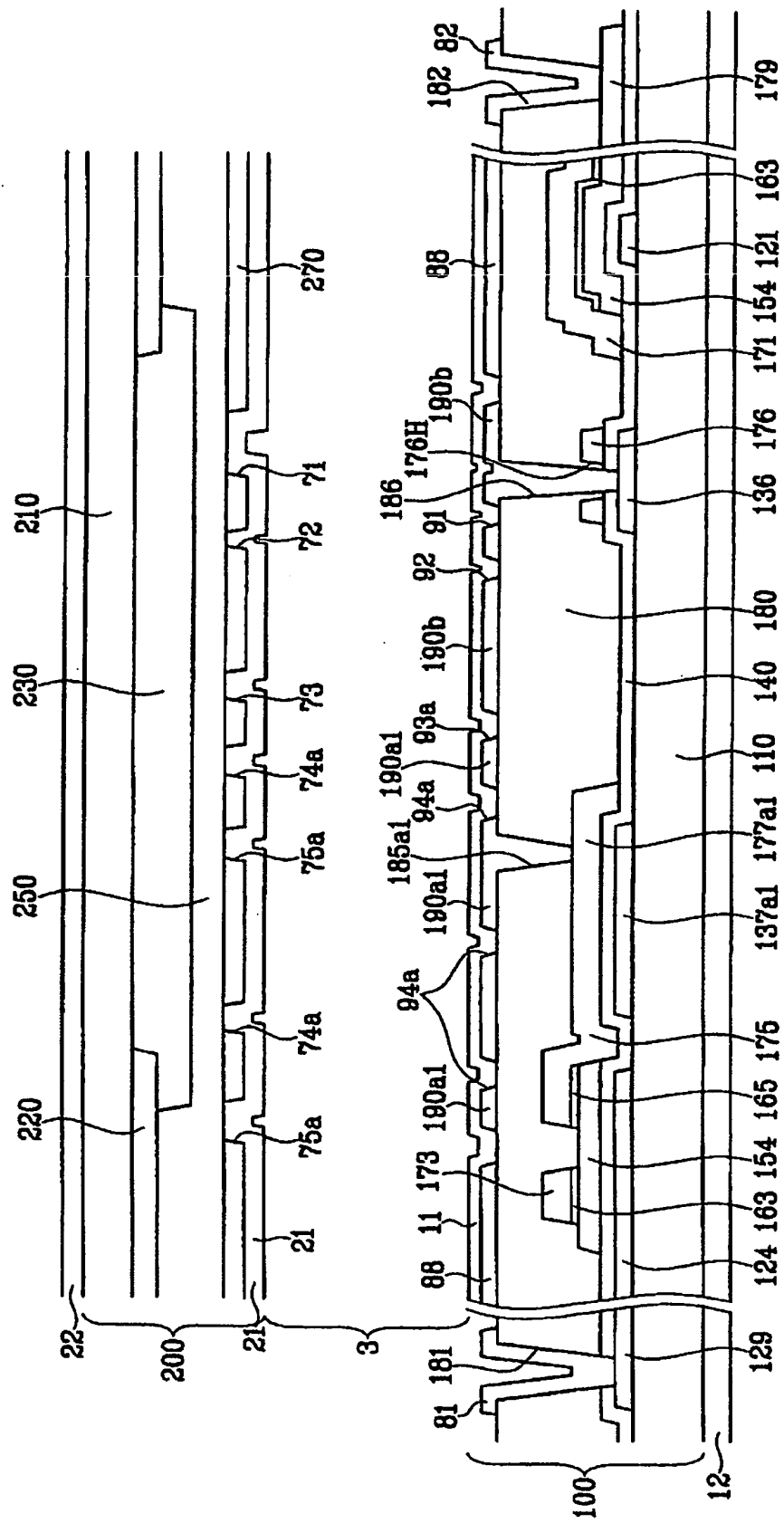


FIG.5

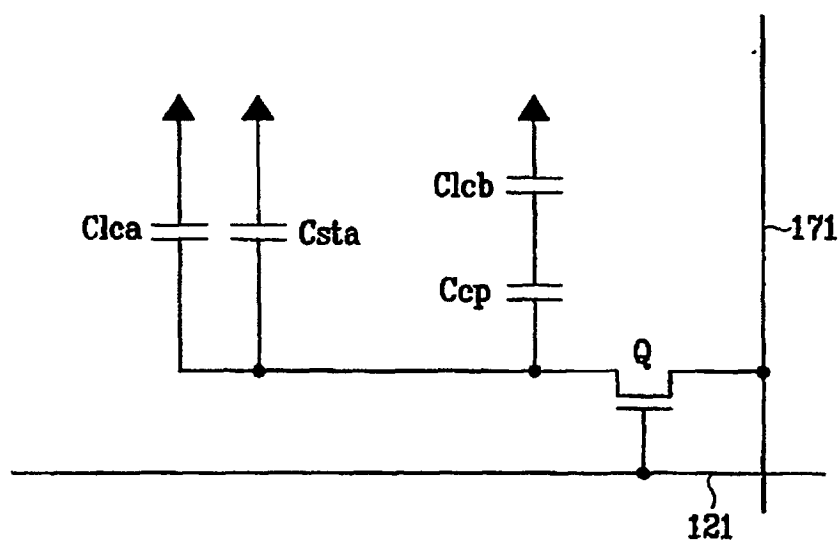


FIG. 6

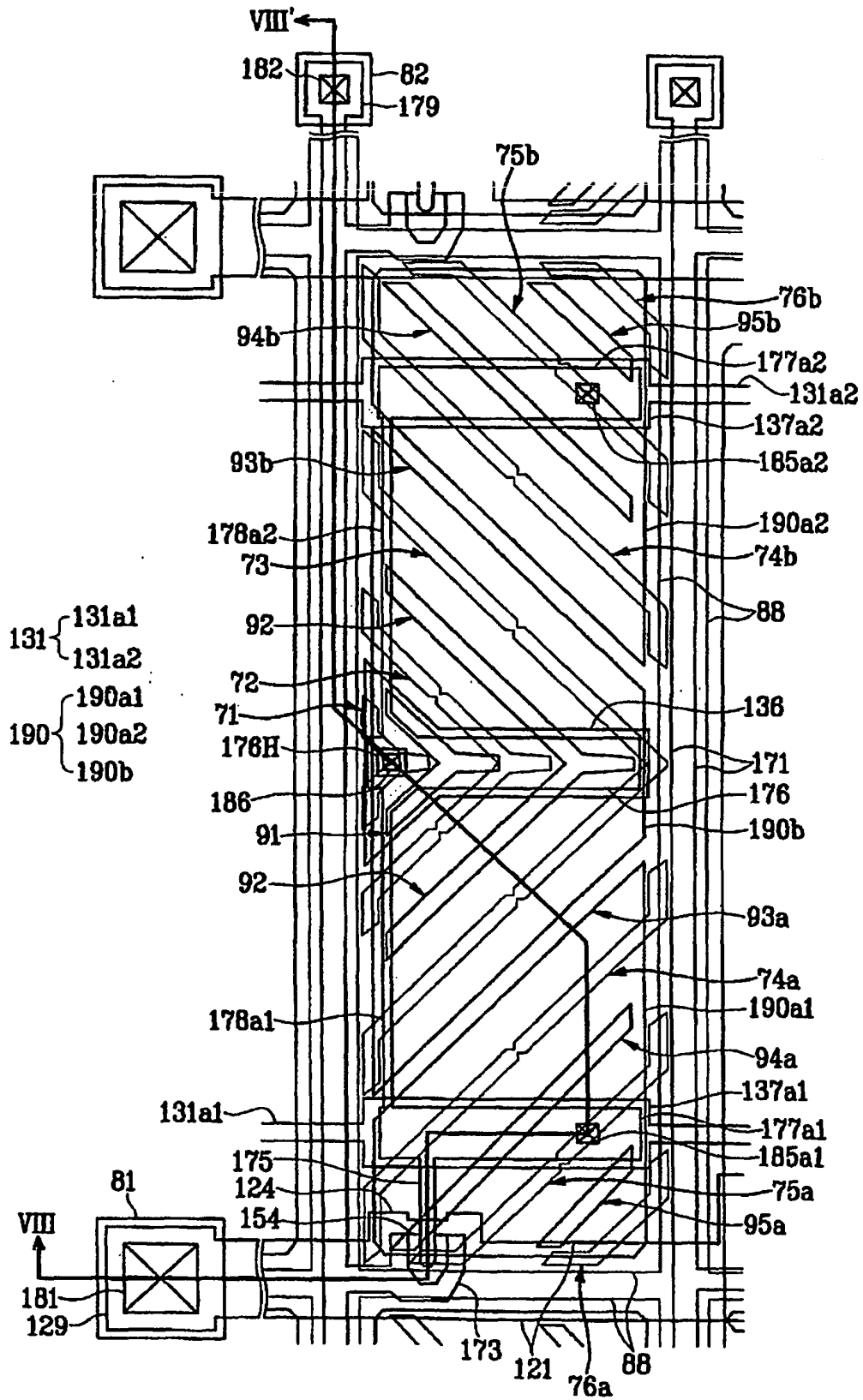


FIG. 7

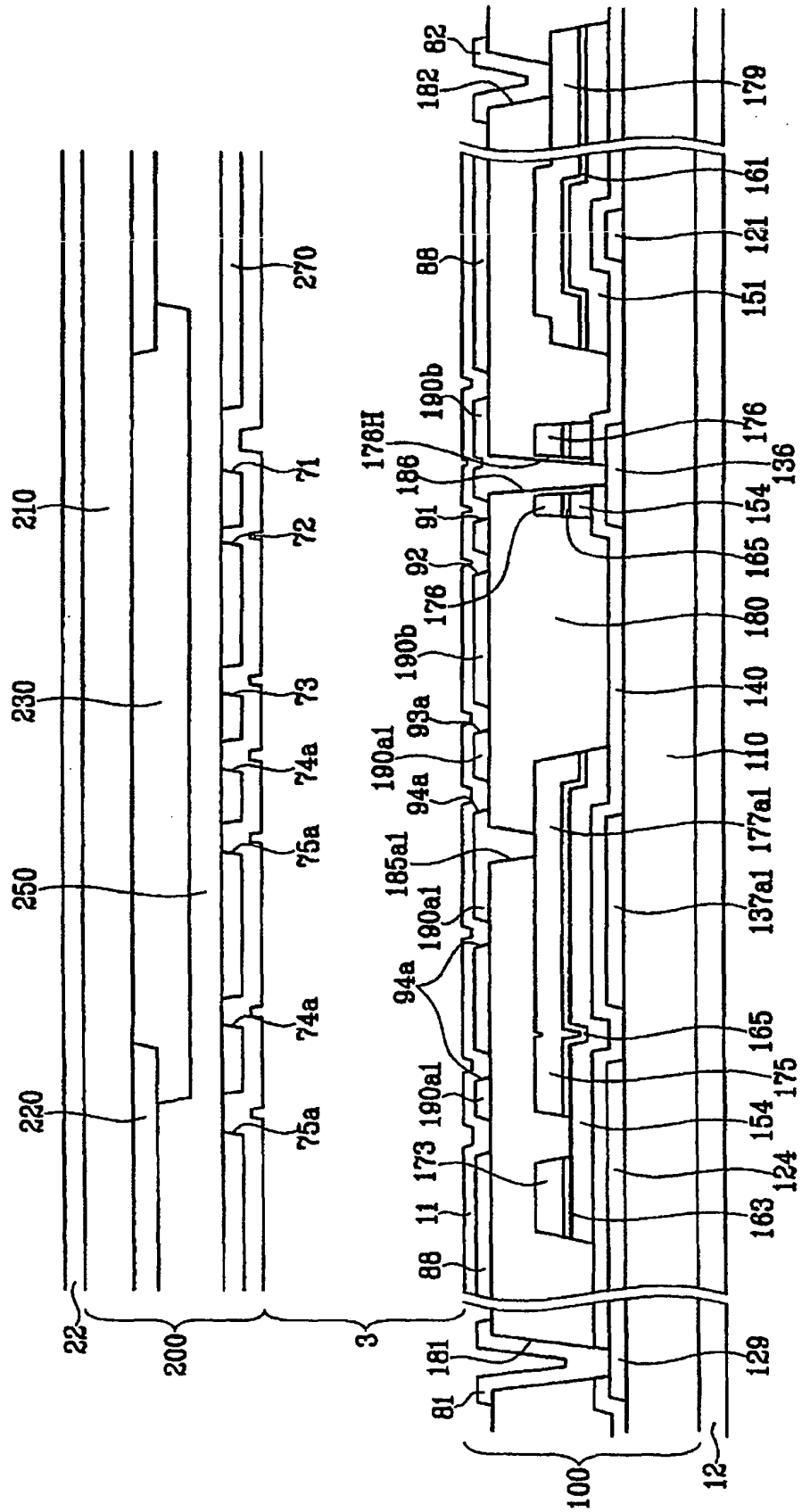
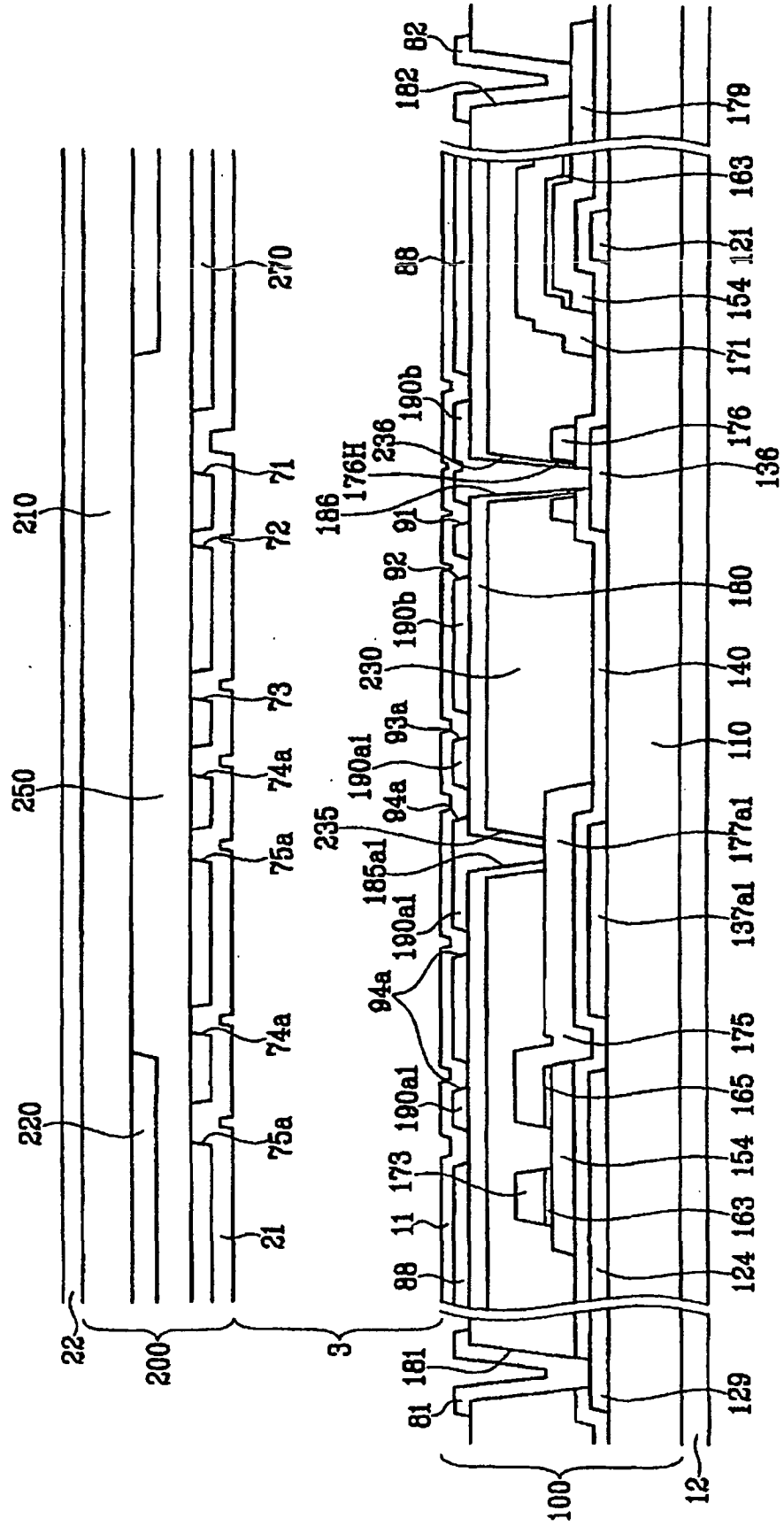


FIG. 8



REFERENCES CITED IN THE DESCRIPTION

This list of references cited by the applicant is for the reader's convenience only. It does not form part of the European patent document. Even though great care has been taken in compiling the references, errors or omissions cannot be excluded and the EPO disclaims all liability in this regard.

Patent documents cited in the description

- US 2004085272 A1 [0005]
- US 2004160560 A1 [0005]
- EP 1605511 A [0006]
- WO 2004029709 A [0007]

专利名称(译)	薄膜晶体管阵列面板		
公开(公告)号	EP1655632B1	公开(公告)日	2011-03-02
申请号	EP2005110301	申请日	2005-11-03
[标]申请(专利权)人(译)	三星电子株式会社		
申请(专利权)人(译)	SAMSUNG ELECTRONICS CO. , LTD.		
当前申请(专利权)人(译)	SAMSUNG ELECTRONICS CO. , LTD.		
[标]发明人	SHIN KYOUNG JU PARK CHEOL WOO LYU JAE JIN CHAI CHONG CHUL		
发明人	SHIN, KYOUNG-JU PARK, CHEOL-WOO LYU, JAE-JIN CHAI, CHONG-CHUL		
IPC分类号	G02F1/13 G02F1/1333 G02F1/1343		
CPC分类号	G02F1/133707 G02F1/134336 G02F1/1393 G02F2001/134345		
优先权	1020040089246 2004-11-04 KR		
其他公开文献	EP1655632A1		
外部链接	Espacenet		

摘要(译)

提供一种用于液晶显示装置 (LCD) 的薄膜晶体管 (TFT) 阵列面板。TFT阵列面板包括多条栅极线，与多条栅极线交叉的至少一条数据线和连接到栅极线和至少一条数据线中的至少一条的至少一个薄膜晶体管。至少一个薄膜晶体管包括漏电极。另外，TFT阵列面板还包括至少一个像素电极，该至少一个像素电极包括连接到薄膜晶体管的漏电极的至少一个第一子像素电极和电容性地耦合到至少一个第一子像素电极的第二子像素电极。此外，像素电极具有用于将像素电极分隔成至少两个分区的分隔构件，所述分区具有不与漏电极重叠的部分。所述至少两个分区对称于与所述多条栅极线等距的参考线对称设置。

$$V_b = V_a \times [C_{cp} / (C_{cp} + C_{icb})],$$