(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 398 658 B1

(12) **EUROPEAN PATENT SPECIFICATION**

(45) Date of publication and mention of the grant of the patent:
24.01.2007 Bulletin 2007/04

(51) Int Cl.:
G02F 1/1343 *(2006.01)* ***G02F 1/1337*** *(2006.01)*
G02F 1/1333 *(2006.01)* ***G09G 3/36*** *(2006.01)*

(21) Application number: **03020606.4**

(22) Date of filing: **10.09.2003**

(54) **Color active matrix type vertically aligned mode liquid cristal display and driving method thereof**

Farbige Flüssigkristallanzeige mit aktiver Matrix und Betriebsmodus mit vertikaler Flüssigkristallausrichtung, sowie Methode zu dessen Ansteuerung

Ecran à cristaux liquides couleur à mode d'alignement vertical et matrice active, et sa méthode de commande

(84) Designated Contracting States:
GB

(30) Priority: **10.09.2002 JP 2002316865**
26.02.2003 JP 2003110895

(43) Date of publication of application:
17.03.2004 Bulletin 2004/12

(73) Proprietor: **Obayashiseikou Co., Ltd.**
Toyokawa-City,
Aichi-Pref. 442-0068 (JP)

(72) Inventor: **Hirota, Naoto**
Toyokawa-City
Aichi-Pref., 442-0068 (JP)

(74) Representative: **Hofer, Dorothea et al**
Prüfer & Partner GbR
Patentanwälte
Sohnckestrasse 12
81479 München (DE)

(56) References cited:
US-A1- 2001 013 852
US-A1- 2003 112 397
US-B1- 6 407 791

- **PATENT ABSTRACTS OF JAPAN vol. 2002, no. 04, 4 August 2002 (2002-08-04) -& JP 2001 343647 A (SHARP CORP), 14 December 2001 (2001-12-14)**

EP 1 398 658 B1

Printed by Jouve, 75001 PARIS (FR)

Description

[Field of the Invention]

[0001] The present invention relates to a big screen active matrix type liquid crystal TV viewing display having a wide viewing angle, high brightness, and high speed of response by low cost, and to a driving method thereof.

[Background of the Invention]

[0002] As shown in Fig. 1, in conventional type vertically aligned mode liquid crystal displays, a mode is adopted in which bumps 5 for controlling a motion direction of liquid crystal molecules 14 are formed on a transparent common electrode 4 of a color filter side substrate 1, and slits 9 for controlling a motion direction of the liquid crystal molecules 14 are provided in transparent pixel electrodes 8 of an active matrix substrate 13, the bumps 5 and the slits 9 determine the motion direction of the liquid crystal molecules 14 serving as one set. There is also provided a method in which slits for controlling a motion direction of liquid crystal molecules 14 in place of bumps 5 are formed on a transparent common electrode 4 on a color filter side substrate 1. Both of these modes are put in practical use for mass-production.

[Disclosure of the Invention]

PROBLEMS TO BE SOLVED BY THE INVENTION

[0003] In conventional type multi-domain vertically aligned mode liquid crystal displays, it has been necessary that bumps or slits are formed on a transparent common electrode in a color filter side substrate, which required one excessive photo mask process. Therefore, cost rise became unavoidable.

[0004] Moreover, in vertically aligned mode liquid crystal displays with bumps 5 formed in color filter layer 3 side, as shown in Fig. 1, when a width, a pitch, and an angle of slope of the bumps 5 are not precisely controlled, variation in tilting degree of liquid crystal molecules 14 was caused, which easily generated unevenness in half tone area.

[0005] Since bumps are made of positive type photoresists, perfect removal of organic solvents, and furthermore hardening by baking at high temperatures of no less than 200 degrees are furthermore required, leading difficulty in shortening of processes. When contaminants are eluted out into liquid crystals from the bumps of positive type photoresists, a phenomenon of afterimage will occur, leading to problems in respect of reliability.

[0006] In color filter substrates using conventional bumps, positive type photoresists are used as materials for bumps, and therefore, when a defect occurs in application process of a vertical alignment film 6 and reworking is required, a dry ashing method using oxygen plasma can not be used. Therefore, a wet remove method requiring high running cost using organic solvents had to be used, which caused a defect requiring a very high reworking cost.

[0007] In vertically aligned mode liquid crystal displays using conventional type bumps and slits, when a display switchovered to a half tone display from a black display, or to a half tone display from a white display, there has been defects that liquid crystals showed a slow response speed.

[0008] US 6,407,791 shows a multi-domain liquid crystal display device composed of a control electrode connected to a source terminal being one of terminals of a thin film transistor serving as a switching device, and a picture electrode having an aperture section provided with one coupling capacitor connected between the pixel electrode and the control electrode. A partial voltage of a signal voltage is applied to the pixel electrode through the other coupling capacitor.

[0009] JP 2001-343647 shows a liquid crystal display device carrying out displaying by applying voltage to a liquid crystal layer which is in a vertical aligned state with no voltage applied to first and second electrodes. The first electrode is provided with a lower conductive layer, a dielectric layer covering at least a part of the lower conductive layer and an upper conductive layer arranged on the liquid crystal layer side of the dielectric layer. The upper conductive layer is provided with conductive layer opening parts and further the lower conductive layer is arranged opposite to at least a part of the conductive layer opening part via the dielectric layer. The dielectric layer is provided with a recessing part in a region corresponding to the conductive layer opening part. The dielectric layer includes a second dielectric layer formed on a first dielectric layer and the recessing part has an opening part formed on the first dielectric layer.

[0010] US 2001/013852 shows a liquid crystal display device that includes a liquid crystal between a substrate having gate buslines, source buslines, switching elements, pixel electrode array, gate driver, source driver, etc., and a substrate having a counter electrode, etc. In this liquid crystal display device, the gate driver performs simultaneous two-line scanning by applying a scanning signal to two gate buslines simultaneously. The source driver feeds video signals of opposite polarities to adjacent source buslines, respectively. The video signals are inverted every vertical scanning period.

[0011] The present invention solves the above-mentioned problems, and an object of the present invention is to improve reliability of a large-sized vertically aligned mode liquid crystal display and to realize a liquid crystal display that may be manufactured at low cost in a short time, and moreover that has high brightness and high-speed of response.

MEANS FOR SOLVING THE PROBLEMS

[0012] The object is attained by a display according to claim 1, 15 or 16. Further developments of the invention

are specified in the dependent claims, respectively.

[Method 1]

[0013] In order to impress a voltage to anisotropic liquid crystal molecules that are vertically aligned to an active matrix substrate and a color filter substrate and have a negative dielectric constant, and to make the liquid crystal molecules tilt in different two directions or four directions, two kinds of following electrode structures were formed in one pixel of the active matrix substrate.

i) A transparent flat common electrode is used in a color filter substrate side, and for transparent pixel electrodes countering the transparent flat common electrode in the active matrix substrate side, patterns (no transparent electrode in a slit part) having a shape of a long and slender slit are formed.
ii) a transparent flat common electrode is used in a color filter substrate side, and for transparent pixel electrodes countering the transparent flat common electrode in the active matrix substrate side, patterns having a shape of a long and slender slit are formed, two rows of liquid crystal alignment direction control electrodes that are mutually separated and set as potentials different from each other exist in a lower layer of the transparent pixel electrode via an insulated film, either of the liquid crystal alignment direction control electrodes have almost the same shape as a shape of a pattern of the shape of long and slender slits, and a larger dimension than a dimension of the slit; and two rows of the liquid crystal alignment direction control electrodes mutually separated are arranged in a direction of a scan signal wire in a lower layer of the long and slender slits that are formed, mutually exchanged in an every fixed pixel cycle, in the transparent pixel electrode.

[Method 2]

[0014] A following drive system is used as a method for driving the vertically aligned mode liquid crystal display having the electrode structure by the method 1.

[0015] There is used a drive system in which: when a potential of the transparent pixel electrode separated for every pixel of an active matrix substrate side is lower than a potential of the countering flat common electrode on a color filter substrate side, a potential of the liquid crystal alignment direction control electrode currently placed in a lower layer of the slit of the transparent pixel electrode is set lower than a potential of the transparent pixel electrode; and when a potential of the transparent pixel electrode is higher than a potential of the countering flat common electrode of the color filter substrate side, a potential of the liquid crystal alignment direction control electrode placed in a lower layer of the slit of the transparent pixel electrode is set higher than a potential of the transparent pixel electrode, and potentials of the liquid crystal alignment direction control electrodes arranged in the vicinity of both sides of the scan signal wiring are set as polar potentials different from each other, and polarities of the potential of the transparent pixel electrode, and each of the potential of the two rows of the liquid crystal alignment direction control electrodes mutually separated in one pixel are reversed to a polarity of a polarity of the potential of the flat common electrode in a color filter substrate side every vertical scanning period.

[Method 3]

[0016] In a color active matrix type vertically aligned mode liquid crystal display in which adjacent transparent pixel electrodes in a direction of a scan signal wiring are connected to a thin film transistor component controlled by mutually different scan signal wirings, in order to impress a voltage to liquid crystal molecules that are vertically aligned between an active matrix substrate and a color filter substrate and to make the liquid crystal molecules tilt in different two directions or different four directions, two kinds of following electrode structures were formed in one pixel of the active matrix substrate.

i) A transparent flat common electrode is used in a color filter substrate side, and for transparent pixel electrodes countering the transparent flat common electrode in the active matrix substrate side, patterns (no transparent electrode in a slit part) having a shape of a long and slender slit are formed.
ii) A transparent flat common electrode is used in a color filter substrate side, and for transparent pixel electrodes countering the transparent flat common electrode in the active matrix substrate side, patterns having a shape of a long and slender slit are formed, and a liquid crystal alignment direction control electrode having almost the same shape as a shape of the slit, and a larger dimension than a dimension of the slit are formed in a lower layer of the slit via an insulated film.

[Method 4]

[0017] A following drive system is used as a method for driving the vertically aligned mode liquid crystal display having the electrode structure by the method 3.

[0018] There is used a drive system in which: when a potential of the transparent pixel electrode separated for every pixel of an active matrix substrate side is lower than a potential of the countering flat common electrode on a color filter substrate side, a potential of the liquid crystal alignment direction control electrode currently placed in a lower layer of the slit of the transparent pixel electrode is set lower than a potential of the transparent pixel electrode; and when a potential of the transparent pixel electrode is higher than a potential of the countering flat common electrode of the color filter substrate side, a potential of the liquid crystal alignment direction control

electrode placed in a lower layer of the slit of the transparent pixel electrode is set higher than a potential of the transparent pixel electrode; and polarities of the potential of the transparent pixel electrode, and of the potential of the liquid crystal alignment direction control electrode are reversed to a polarity of a potential of the flat common electrode in a color filter substrate side every vertical scanning period.

[Method 5]

[0019] In order to impress a voltage to anisotropic liquid crystal molecules that are vertically aligned to an active matrix substrate and a color filter substrate and have a negative dielectric constant, and to make the liquid crystal molecules tilt in many directions, two kinds of following electrode structures were formed in one pixel of the active matrix substrate.

i) A transparent flat common electrode is used in a color filter substrate side, and for transparent pixel electrodes countering the transparent flat common electrode on the active matrix substrate side, many circular or polygonal holes (no transparent electrodes in a portion of a hole) are formed.
ii) A transparent flat common electrode is used in a color filter substrate side, and for transparent pixel electrodes countering the transparent flat common electrode in the active matrix substrate side, patterns having a shape of a long and slender slit are formed, two rows of liquid crystal alignment direction control electrodes that are mutually separated and set as potentials different from each other exist in a lower layer of the transparent pixel electrode via an insulated film, either of the liquid crystal alignment direction control electrodes has almost the same shape as a shape of a pattern of the shape of long and slender slits, and a larger dimension than a dimension of the slit, and two rows of the liquid crystal alignment direction control electrodes mutually separated are arranged in a direction of a scan signal wiring in a lower layer of the long and slender slits that are formed, mutually exchanged in an every fixed pixel cycle, in the transparent pixel electrode.

[Method 6]

[0020] A following drive system is used as a method for driving the vertically aligned mode liquid crystal display having the electrode structure by the method 5.
[0021] There is used a drive system in which: when a potential of the transparent pixel electrode separated for every pixel of an active matrix substrate side is lower than a potential of the countering flat common electrode on a color filter substrate side, a potential of the liquid crystal alignment direction control electrode currently placed in a lower layer of a slit of the transparent pixel electrode is set lower than a potential of the transparent pixel electrode; and when a potential of the transparent pixel electrode is higher than a potential of the countering flat common electrode of the color filter substrate side, a potential of the liquid crystal alignment direction control electrode placed in a lower layer of the slit of the transparent pixel electrode is set higher than a potential of the transparent pixel electrode; and potentials of the liquid crystal alignment direction control electrodes arranged in the vicinity of both sides of the scan signal wiring are set as polar potentials different from each other, and polarities of the potential of the transparent pixel electrode, and of each of the potential of the two rows of the liquid crystal alignment direction control electrodes mutually separated in one pixel are reversed to a polarity of a potential of the flat common electrode in a color filter substrate side every vertical scanning period.

[Method 7]

[0022] In an active matrix type vertically aligned mode liquid crystal display in which adjacent transparent pixel electrodes in a direction of a scan signal wiring are connected to a thin film transistor component controlled by mutually different scan signal wirings, in order to impress a voltage to liquid crystal molecules that are vertically aligned between an active matrix substrate and a color filter substrate and to make the liquid crystal molecules tilt in many directions, two kinds of following electrode structures were formed in one pixel of the active matrix substrate.

i) A transparent flat common electrode is used in a color filter substrate side, and for transparent pixel electrodes countering the transparent flat common electrode in the active matrix substrate side, many circular or polygonal holes (no transparent electrodes in a portion of a hole) are formed.
ii) A transparent flat common electrode is used in a color filter substrate side, and for transparent pixel electrodes countering the transparent flat common electrode in the active matrix substrate side, patterns having a shape of a long and slender slit are formed, a liquid crystal alignment direction control electrode having almost the same shape as a shape of the slit, and a larger dimension than a dimension of the slit are formed in a lower layer of the slit via an insulated film.

[Method 8]

[0023] A following drive system is used as a method for driving the vertically aligned mode liquid crystal display having the electrode structure by the method 7.
[0024] There is used a drive system in which: when a potential of the transparent pixel electrode separated for every pixel on an active matrix substrate side is lower than a potential of the countering flat common electrode on a color filter substrate side, a potential of the liquid

crystal alignment direction control electrode currently placed in a lower layer of a slit of the transparent pixel electrode is set lower than a potential of the transparent pixel electrode; and when a potential of the transparent pixel electrode is higher than a potential of the countering flat common electrode of the color filter substrate side, a potential of the liquid crystal alignment direction control electrode placed in a lower layer of the slit of the transparent pixel electrode is set higher than a potential of the transparent pixel electrode; and polarities of the potential of the transparent pixel electrode, and of the potential of the liquid crystal alignment direction control electrode are reversed to a polarity of a potential of the flat common electrode in a color filter substrate side every vertical scanning period.

[Method 9]

[0025] In the method 1 and 3, the slit formed in the transparent pixel electrode in an active matrix substrate side and extending long and slender, and the slit forming a group with the liquid crystal alignment direction control electrode are arranged alternately, maintaining an almost parallel relationship in a direction making about ±45 degrees to a direction of the scan signal wiring; and polarization axes of two polarizing plates placed in exterior of a liquid crystal cell are arranged in a direction of the scan signal wiring and in a direction of the video signal wiring, and are arranged so that they may perpendicularly mutually intersect.

[Method 10]

[0026] In the method 1 and 3, there was adopted a structure that the slit formed in the transparent pixel electrode in an active matrix substrate side and extending long and slender is arranged in a direction making ±45 degrees to a direction of a scan signal wiring; and the slit forming a group with the liquid crystal alignment direction control electrode are arranged in a parallel direction and in a perpendicular direction to a direction of the scan signal wirings; and the liquid crystal alignment direction control electrode encloses a periphery of the transparent pixel electrode while overlapping with the transparent pixel electrode via the insulated film; and polarization axes of two polarizing plates placed in exterior of a liquid crystal cell are arranged in the direction of the scan signal wiring and in a direction of the video signal wiring, and are arranged so that they may perpendicularly mutually intersect.

[Method 11]

[0027] In the method 1 and 3, there was adopted a structure that the slit formed in a transparent pixel electrode in an active matrix substrate side and extending long and slender is arranged in a parallel direction and in a perpendicular direction to the direction of the scan signal wiring; and the slit forming a group with the liquid crystal alignment direction control electrode is arranged in parallel to a direction of the scan signal wiring; and the liquid crystal alignment direction control electrode encloses a periphery of the transparent pixel electrode while overlapping with the transparent pixel electrode via the insulated film; and polarization axes of two polarizing plates placed in exterior of a liquid crystal cell are arranged a direction of the scan signal wiring and in a direction of the video signal wiring, and are arranged so that they may perpendicularly mutually intersect.

[Method 12]

[0028] In the method 1 and 3, the slit formed in a transparent pixel electrode in an active matrix substrate side and extending long and slender is arranged in a parallel direction and in a perpendicular direction to a direction of the scan signal wiring; and the slit forming a group with the liquid crystal alignment direction control electrode have a structure arranged in directions making ±45 degrees to a direction of the scan signal wiring; and polarization axes of two polarizing plates placed in exterior of a liquid crystal cell are arranged in a direction of the scan signal wiring and in a direction of the video signal wiring, and are arranged so that they may perpendicularly mutually intersect.

[Method 13]

[0029] In the method 5 and 7, there was adopted a structure that the slit forming a group with the liquid crystal alignment direction control electrode are arranged in a parallel direction and in a perpendicular direction to a direction of the scan signal wiring so as to enclose two or more of circular or polygonal holes currently formed in the transparent pixel electrode in an active matrix substrate side; and the liquid crystal alignment direction control electrode encloses a periphery of the transparent pixel electrode while overlapping with the transparent pixel electrode via the insulated film; and polarization axes of two polarizing plates placed in exterior of a liquid crystal cell are arranged in a direction of the scan signal wiring and in a direction of the video signal wiring, and are arranged so that they may perpendicularly mutually intersect.

[Method 14]

[0030] In the method 1, 3, 5, and 7, the liquid crystal alignment direction control electrode formed in a lower layer of the slit of the transparent pixel electrode via the insulated film is simultaneously formed in the same layer at the time of formation of the scan signal wiring.

[Method 15]

[0031] In the methods 1, 3, 5, and 7, an additional ca-

pacitance was formed with the liquid crystal alignment direction control electrode formed in a lower layer of the slit of the transparent pixel electrode via the insulated film, and the transparent pixel electrode.

[Method 16]

[0032] In the method 1 and 5, all of the scan signal wirings and the liquid crystal alignment direction control electrodes are completely separated, and are connected to output terminals of different drive ICs, respectively; and contact buttons of the two rows of liquid crystal alignment direction control electrodes for controlling one row of pixels are arranged so that they may be sandwiched between contact buttons of different scan signal wirings.

[Method 17]

[0033] In the method 3 and 7, all of the scan signal wirings and the liquid crystal alignment direction control electrodes are completely separated and independent, and are connected to output terminals of different drive ICs, respectively; and contact buttons of the one row of liquid crystal alignment direction control electrodes for controlling one row of pixels are arranged so that they may be sandwiched between contact buttons of different scan signal wirings.

[Method 18]

[0034] In the method 1, 3, 5, and 7, contact buttons of the scan signal wiring are arranged in either of right side or left side of a display screen part, and contact buttons of the liquid crystal alignment direction control electrode are arranged on another side different from a side of the contact buttons of the scan signal wiring, each contact button is mutually completely separated and independent, and is connected to output terminals of different drive ICs, respectively.

[Method 19]

[0035] In the method 1 and 5, the scan signal wirings and the liquid crystal alignment direction control electrodes are completely separated and independent, each contact button is arranged on both of right and left sides of a display screen part, and contact buttons of the two rows of the liquid crystal alignment direction control electrodes for controlling one row of pixels are arranged so that they may be sandwiched between contact buttons of different scan signal wirings.

[Method 20]

[0036] In the method 3 and 7, all of scan signal wirings and liquid crystal alignment direction control electrodes are completely separated and independent, each contact button is arranged on both of right and left sides of a display screen part, and contact buttons of the one row of liquid crystal alignment direction control electrodes for controlling one row of pixels are arranged so that they may be sandwiched between contact buttons of different scan signal wirings.

[Method 21]

[0037] In the methods 2, 4, 6, and 8, at the time of moving image displaying, a bias voltage impressed between the liquid crystal alignment direction control electrode currently formed in a lower layer of the slit of the transparent pixel electrode and the transparent pixel electrode is set higher than a voltage at the time of still picture displaying, and thereby, a tilting speed of anisotropic liquid crystal molecules having a negative dielectric constant are set higher.

[Method 22]

[0038] In order to impress a voltage to anisotropic liquid crystal molecules having a negative dielectric constant that are vertically aligned to an active matrix substrate and a color filter substrate and to make the liquid crystal molecules tilt in different two directions or different four directions, two kinds of following electrode structure and structure arrangement were formed in one pixel of the active matrix substrate.

i) A transparent flat common electrode is used in a color filter substrate side, and for transparent pixel electrodes countering the transparent flat common electrode in the active matrix substrate side, patterns (no transparent electrode in a slit part) having a shape of a long and slender slit are formed.

ii) A transparent flat common electrode is used in a color filter substrate side, and for transparent pixel electrodes countering the transparent flat common electrode in the active matrix substrate side, patterns having a shape of a long and slender slit are formed, and a liquid crystal alignment direction control electrode having almost the same shape as a shape of the slit, and a larger dimension than a dimension of the slit are formed in a lower layer of the slit via an insulated film.

iii) In a pixel of n row m column, a thin film transistor element is formed in a position where a scan signal wiring of (n-1) row and a video signal wiring of (m+1) column intersect with each other, and a video signal wiring of (m+1) column and a liquid crystal alignment direction control electrode used for a pixel of n row m column are connected via the thin film transistor element; and a thin film transistor element is formed in a position where a scan signal wiring of n row and a video signal wiring of m column intersect, and a video signal wiring of m column and a transparent pixel electrode used for a pixel of n row m column are connected via the thin film transistor element.

[Method 23]

[0039] In order to impress a voltage to anisotropic liquid crystal molecules having a negative dielectric constant that are vertically aligned to an active matrix substrate and a color filter substrate and to make the liquid crystal molecules tilt in different two directions or different four directions, two kinds of following electrode structure and structure arrangement were formed in one pixel of the active matrix substrate.

i) A transparent flat common electrode is used in a color filter substrate side, and for transparent pixel electrodes countering the transparent flat common electrode in the active matrix substrate side, patterns (no transparent electrode in a slit part) having a shape of a long and slender slit are formed.
ii) A transparent flat common electrode is used in a color filter substrate side, and for transparent pixel electrodes countering the transparent flat common electrode in the active matrix substrate side, patterns having a shape of a long and slender slit are formed, and a liquid crystal alignment direction control electrode having almost the same shape as a shape of the slit, and a larger dimension than a dimension of the slit is formed in a lower layer of the slit via an insulated film.
iii) In a pixel of n row m column, a thin film transistor element is formed on a scan signal wiring of (n-1) row, a common electrode of n row, and a liquid crystal alignment direction control electrode used for a pixel of n row m column are connected via the thin film transistor element, and a thin film transistor element is formed in a position where a scan signal wiring of n row and a video signal wiring of m column intersect with each other, and the video signal wiring of m column, and a transparent pixel electrode used for a pixel of n row m column are connected via the thin film transistor element.

[Method 24]

[0040] In order to impress a voltage to liquid crystal molecules that are vertically aligned to an active matrix substrate and a color filter substrate and to make the liquid crystal molecules tilt in many directions, two kinds of following electrode structure and structure arrangement were formed in one pixel of the active matrix substrate.

i) A transparent flat common electrode is used in a color filter substrate side, and for transparent pixel electrodes countering the transparent flat common electrode in the active matrix substrate side, circular or polygonal holes (no transparent electrodes in a portion of a hole) are formed.
ii) A transparent flat common electrode is used in a color filter substrate side, and for transparent pixel electrodes countering the transparent flat common electrode in the active matrix substrate side, patterns having a shape of a long and slender slit are formed, a liquid crystal alignment direction control electrode having almost the same shape as a shape of the slit, and a larger dimension than a dimension of the slit are formed in a lower layer of the slit via the insulated film.
iii) In a pixel of n row m column, a thin film transistor element is formed in a position where a scan signal wiring of (n-1) row and a video signal wiring of (m+1) column intersect with each , and a video signal wiring of (m+1) column and a liquid crystal alignment direction control electrode used for a pixel of n row m column are connected via the thin film transistor element; and a thin film transistor element is formed in a position where a scan signal wiring of n row and a video signal wiring of m column intersect with each other, and the video signal wiring of m column and a transparent pixel electrode used for pixel of n row m column are connected via the thin film transistor element.

[Method 25]

[0041] In order to impress a voltage to liquid crystal molecules that are vertically aligned between an active matrix substrate and a color filter substrate and to make the liquid crystal molecules tilt in many directions, two kinds of following electrode structures and structure arrangements were formed in one pixel of the active matrix substrate.

i) A transparent flat common electrode is used in a color filter substrate side, and for transparent pixel electrodes countering the transparent flat common electrode in the active matrix substrate side many circular or polygonal holes (no transparent electrodes in a portion of a hole) are formed.
ii) A transparent flat common electrode is used in a color filter substrate side, and for transparent pixel electrodes countering the transparent flat common electrode in the active matrix substrate side, patterns having a shape of a long and slender slit are formed, and a liquid crystal alignment direction control electrode having almost the same shape as a shape of the slit, and a larger dimension than a dimension of the slit are formed in a lower layer of the slit via an insulated film.
iii) In a pixel of n row m column, a thin film transistor element is formed on a scan signal wiring of (n-1) row, a common electrode of n row and a liquid crystal alignment direction control electrode used for a pixel of n row m column are connected via the thin film transistor element, and a thin film transistor element is formed in a position where a scan signal wiring of n row and a video signal wiring of m column intersect with each other, and the video signal wiring of m

column and a transparent pixel electrode used for a pixel of n row m column are connected via the thin film transistor element.

[Method 26]

[0042] In the methods 22, 23, 24, and 25, a time width of a scan signal waveform in the scan signal wiring is no less than two times of a horizontal period, a scan signal waveform in a scan signal wiring of (n-1) th row and a scan signal waveform in a scan signal wiring of (n) th row overlap one another by no less than one time of a horizontal period; and polarities of a video signal voltage of a video signal wiring of m column, and a video signal voltage of a video signal wiring of (m+1) column are different from each other, and the polarities being mutually exchanged every horizontal period, and the polarities being mutually exchanged every vertical period.

[Method 27]

[0043] In the methods 22 and 24, a channel length (L_2) of a thin film transistor element that is formed in a position where a scan signal wiring of (n-1) row and a video signal wiring of column (m+1) intersect, and is connected with the liquid crystal alignment direction control electrode was set larger than a channel length (L_1) of a thin film transistor element that is formed in a position where a scan signal wiring of n row and a video signal wiring of m column intersect, and is connected with the transparent pixel electrode ($L_1 < L_2$) .

[Method 28]

[0044] In the methods 23 and 25, a channel length (L_2) of a thin film transistor element that is formed on a scan signal wiring of (n-1) row, and is connected with the liquid crystal alignment direction control electrode was set larger than a channel length (L_1) of a thin film transistor element that is formed in a position where a scan signal wiring of n row and a video signal wiring of m column intersect, and is connected with the transparent pixel electrode ($L_1 < L_2$).

[Method 29]

[0045] In the methods 22, 23, 24, and 25, a double transistor element structure or an offset channel element structure was used for a thin film transistor element connected with the liquid crystal alignment direction control electrode.

[Method 30]

[0046] In the methods 22 and 23, a slit formed in the transparent pixel electrode in the active matrix substrate side and extending long and slender, and a slit forming a group with the liquid crystal alignment direction control electrode are arranged alternately, maintaining a relationship almost parallel to each other in an angle direction of about $\pm$45 degrees to an extending direction of the scan signal wiring; polarization axes of two polarizing plates placed in exterior of a liquid crystal cell are arranged in a direction of the scan signal wiring and in a direction of the video signal wiring, and are arranged so that they may perpendicularly mutually intersect.

[Method 31]

[0047] In the methods 22 and 23, a slit formed in a transparent pixel electrode in the active matrix substrate side and extending long and slender are arranged in a parallel direction and in a perpendicular direction to an extending direction of the scan signal wiring; and a slit forming a group with the liquid crystal alignment direction control electrode is arranged in a angle direction of about $\pm$45 degrees to a direction of the scan signal wirings; and polarization axes of two polarizing plates placed in exterior of a liquid crystal cell are arranged in a direction of the scan signal wiring and in a direction of the video signal wiring, and are arranged so that they may perpendicularly mutually intersect.

[Method 32]

[0048] In methods 22 and 23, there was adopted a structure that a slit formed in the transparent pixel electrode in the active matrix substrate side and extending long and slender is arranged in a angle direction of about $\pm$45 degrees to an extending direction of the scan signal wiring; and a slit forming a group with the liquid crystal alignment direction control electrode is arranged in a parallel direction and in a perpendicular direction to an extending direction of the scan signal wiring; and the liquid crystal alignment direction control electrode encloses a periphery of the transparent pixel electrode while overlapping with the transparent pixel electrode via the insulated film; and polarization axes of two polarizing plates placed in exterior of a liquid crystal cell are arranged in a direction of the scan signal wiring and in a direction of the video signal wiring, and are arranged so that they may perpendicularly mutually intersect.

[Method 33]

[0049] In methods 24 and 25, there was adopted a structure that a slit forming a group with the liquid crystal alignment direction control electrode is arranged in a direction perpendicular to a direction parallel to an extending direction of the scan signal wiring so that two or more circular or polygonal holes currently formed in the transparent pixel electrode in the active matrix substrate side may be surrounded; and the liquid crystal alignment direction control electrode encloses a periphery of the transparent pixel electrode while overlapping with the transparent pixel electrode via the insulated film; and po-

larization axes of two polarizing plates placed in exterior of a liquid crystal cell are arranged in a direction of the scan signal wiring and in a direction of the video signal wiring, and are arranged so that they may perpendicularly mutually intersect.

[Method 34]

[0050] In the methods 22, 23, 24, and 25, the liquid crystal alignment direction control electrode formed in a lower layer of a slit of the transparent pixel electrode via the insulated film is simultaneously formed in the same layer at the time of formation of the scan signal wiring.

[Method 35]

[0051] In the methods 22 and 23, the liquid crystal alignment direction control electrode formed in a lower layer of a slit of the transparent pixel electrode via the insulated film is simultaneously formed in the same layer at the time of formation of the video signal wiring.

[Method 36]

[0052] In the method 22, two thin film transistor elements are required in one pixel in order to drive the one pixel and only one contact hole exists for electrically connecting a drain electrode of a thin film transistor element formed in a position where a scan signal wiring of n row and a video signal wiring of m column intersect with each other, and the transparent pixel electrode.

[Method 37]

[0053] In the methods 22 and 24, two thin film transistor elements are required in one pixel in order to drive the one pixel and two contact holes exist for electrically connecting a drain electrode of a thin film transistor element formed in a position where a scan signal wiring of (n-1) row and a video signal wiring of (m+1) column intersect with each other, and the liquid crystal alignment direction control electrode; and only one contact hole exists for electrically connecting a drain electrode of a thin film transistor element formed in a position where a scan signal wiring of n row and a video signal wiring of m column intersect with each other, and the transparent pixel electrode.

[Method 38]

[0054] In the methods 22, 23, 24, and 25, two thin film transistor elements are required in one pixel in order to drive the one pixel and one thin film transistor element is connected to the transparent pixel electrode, another remaining thin film transistor element is connected to the liquid crystal alignment direction control electrode, and the transparent pixel electrode and the liquid crystal alignment direction control electrode were overlapped via the insulated film to form a capacitance.

[Method 39]

[0055] In the methods 22, 23, 24, and 25, an intermediate electrode of a thin film transistor element connected with the liquid crystal alignment direction control electrode and having a double transistor structure and the transparent pixel electrode overlap via the insulated film to form a capacitance.

[Method 40]

[0056] In the methods 22 and 24, a transparent pixel electrode of n row and m column and a scan signal wiring of (n-1) th row may overlap one another via an insulated film to form a storage capacitor.

[Method 41]

[0057] In the methods 23 and 25, a transparent pixel electrode of n row and m column and a common electrode of n row may overlap one another via the insulated film to form a storage capacitor.

[Effect of the Invention]

[0058] Use of the methods 1, 2, 3, 4, 5, 6, 7, and 8, enables anisotropic liquid crystal molecules having a negative dielectric constant in a state of being vertically aligned to tilt in a target direction, as shown in Fig. 2, Fig. 3, Fig. 5, and Fig. 6.

[0059] This makes unnecessary formation of a bump 5 that had to be formed on a color filter side substrate of a vertically aligned mode liquid crystal display, for motion directional control of liquid crystal molecules, as is shown in conventional method Fig. 1. Moreover, this enables manufacture of a multi-domain vertically aligned mode liquid crystal display using a cheap color filter, as shown in Fig. 4.

[0060] Furthermore, only alignment layers 6 and 7 and anisotropic liquid crystal molecules having a negative dielectric constant 14 exist between a flat common electrode 4 in a color filter side, and a transparent pixel electrode 8 of an active matrix substrate as shown in Fig. 4, which completely solves problems, such as diffusion of contaminants from the bump 5, and remarkably improves reliability.

[0061] Additionally, even in case of failure in application of an alignment layer, omission of bump 5 enables simple and short time regeneration with oxygen plasma by a dry-asher. That is, in surface treatment process before alignment layer application, a plasma treatment with oxygen and argon using a dry-asher becomes usable, which remarkably decrease repelling and generation of pinhole in alignment layer application process.

[0062] Use of the methods 9, 10, 11, 12, and 13 may sharply improve effective use efficiency of polarizing

plates, and thereby may reduce a cost of polarizing plates used for very large-sized liquid crystal displays. In addition, effective use efficiency of a polarizer having reflexibility comprising multilayer laminated body of two kinds of materials used for a backlight may also be sharply improved, which may also reduce cost of a backlight for very large-sized liquid crystals display. Moreover, possibility of control for a motion direction of liquid crystal molecules in four directions may provide wide viewing angles.

[0063] Use of the methods 14 and 15 enables manufacture of an active matrix substrate of the present invention using completely same processes, without changing manufacturing processes of conventional active matrix substrate.

[0064] In addition, since a liquid crystal alignment direction control electrode is arranged close to both sides of a video signal wiring and, as shown in Fig. 7, Fig. 8, Fig. 9, Fig. 10, Fig. 14, Fig. 16, Fig. 17, Fig. 18, and Fig. 25, a potential variation of a video signal wiring is easily shielded, which may completely control a cross talk generation in a perpendicular direction.

[0065] Use of the methods 16, 17, 18, 19, and 20 enables separate drive for every row of liquid crystal alignment direction control electrodes currently formed in a lower layer of slits of transparent pixel electrodes of each row, enabling uniform display by same conditions in all portions of upper part, central part, and lower part of a display screen.

[0066] Use of the methods 2, 4, 6, 8, and 21 enables anisotropic liquid crystal molecules having a negative dielectric constant in a state of being vertically aligned to tilt in a target direction, preventing generation of disclination to enable uniform half tone display. Additionally, use of the method of the present invention may sharply improve a late response speed, in a change to a half tone display from a black display, and to a half tone display from a white display, that has been a problem in a conventional vertically aligned mode liquid crystal display mode. In case of responding animated pictures, increase of a bias voltage impressed between a certain transparent pixel electrode and a liquid crystal alignment direction control electrode formed in a lower layer of slits of the transparent pixel electrode may further improve a speed of response. In the present invention, since a display approaches closer to black display and the above-mentioned bias voltage may become larger, a speed of response is improvable in all regions.

[0067] Use of the methods 22, 23, 24, 25, and 26 makes unnecessary formation of a bump 5 in a color filter (CF) substrate 3 for motion directional control of liquid crystal molecules as is shown in Fig. 1 of conventional methods, which may enable a simple color filter structure as is shown in Fig. 34, Fig. 40, Fig. 45, and Fig. 46 to realize low price. Furthermore, a problem of diffusion into liquid crystals of contaminant from bumps, which conventionally has been a problem, may completely be solved, and also a problem of unevenness in a half tone area induced from heterogeneity of shape of the bumps may completely be wiped away, leading to simultaneous realization of remarkable improvement in yield, and improvement in reliability.

[0068] Moreover, since a method of the present invention does not require bumps, in failure in application of an alignment layer, regeneration can be easily performed in a short time using oxygen plasma by a dry-asher. In surface treatment process before alignment layer application, a plasma treatment with oxygen and argon using a dry-asher becomes usable, which remarkably decrease repelling and generation of pinhole in alignment layer application process.

[0069] Use of the methods 22, 23, 24, 25, 26, 27, 28, 29, and 39 makes unnecessary special drive ICs for driving liquid crystal alignment direction control electrodes, and contact button parts, which may realize low price products. Furthermore, use of a double transistor structure, or an offset transistor structure may reduce leakage current. Since electric field is dispersed and concentration is prevented, even if a large voltage is impressed between a source and a drain electrode of a transistor, shift of a threshold voltage (Vth) of thin film transistors is reduced, leading to realization of a reliable liquid crystal panel. Increase in a channel length (L_2) of thin film transistor elements connected to liquid crystal alignment direction control electrodes may reduce a leakage current.

[0070] Use of the methods 22, 23, 24, 25, 26, 30, 31, 32, and 33 may sharply improve effective use efficiency of a polarizing plate compared with conventional liquid crystal panels in TN (Twisted Nematic) mode, which may reduce a cost of a polarizing plate used in very large-sized liquid crystal displays. In addition, effective use efficiency of a polarizer having reflexibility comprising multilayer laminated body of two kinds of materials (brand name: DBEF by 3M Inc.) used for a backlight may also be sharply improved, which may also reduce a cost of a backlight for very large-sized liquid crystal displays.

[0071] Since use of the methods 22, 23, 24, 25, 34, and 35 enables manufacture of active matrix liquid crystal panels of the present invention using same processes, without changing most of conventional manufacturing processes of an active matrix substrate and manufacturing processes of a color filter in TN mode, leading to demonstration of predominancy in respect of yield and low cost.

[0072] Use of the methods 22, 23, 24, 25, 26, 36, 37, and 38 may realize vertically aligned mode liquid crystal display having a simplest structure. This method does not have excessive and unnecessary thin film transistor elements in one pixel, but an aperture ratio may be set large in the highest, being able to realize a bright display.

[0073] Since use of the methods 22, 23, 24, 25, 26, 27, 28, 29, and 39 enables impression of a large voltage between a transparent pixel electrode and a liquid crystal alignment direction control electrode, deformation of an electric field for driving vertically aligned liquid crystal molecules may be set significantly large. This may im-

prove a rate of reaction of the liquid crystal molecules, and even in moving image displaying, a flow of image and a residual image phenomenon are scarcely generated.

[0074] When a scanning line of n row is set as OFF, use of the methods 22, 23, 24, 25, 40, and 41 may decrease a potential variation of a transparent pixel electrode, and reduce flicker.

[0075] Use of the methods 22, 23, 24, 25, and 26 may provide vertically aligned liquid crystal molecules with alignment almost perpendicular in all areas at the time of black display, which reduces light leakage more than in conventional methods using bumps, and may realize completely uniform black display also in a dark room.

[Best Mode of Carrying Out the Invention]

[0076] Hereinafter, with reference to accompanying drawings, description about desirable Example of the present invention will be provided.

[Example 1]

[0077] Figs. 4, 5, and 6 show sectional views of Example 1 of the present invention. A color filter substrate 1 has a flat transparent common electrode 4, and an active matrix substrate 13 is arranged facing the substrate 1 and in parallel.

[0078] In the active matrix substrate 13, firstly, a scan signal wiring 17 and a liquid crystal alignment direction control electrode 15 are simultaneously formed in the same layer, and subsequently, a gate insulator film 12, an amorphous silicone layer, and an n^+ amorphous silicone layer for ohmic contacts are deposited.

[0079] After formation of a thin film transistor element part, a video signal wiring 11 and a drain electrode are formed.

[0080] Next, a contact hole 18 is formed in a portion of a drain electrode after deposition of a passivation film 10, and then a transparent electric conductive film is deposited. In the transparent electric conductive film, as shown in Fig. 7, some slits are formed and each pixel is completely separated for every pixel to provide a transparent pixel electrode 8.

[0081] An electrode structure of the present invention has following special features: there exist one another in one pixel a portion in which a long and slender slit 9, or a circular or polygonal hole is formed facing a flat transparent common electrode 4 on a color filter side, as shown in Fig. 2; and a portion in which a long and slender slit and a liquid crystal alignment direction control electrode 15 having almost the same shape as the slit, and having a larger dimension than a dimension of the slit are formed facing the flat transparent common electrode 4 on a color filter side, as shown in Fig. 3.

[0082] As shown in Fig. 5 and Fig. 6, these two kinds of electrode structures control to tilt correctly anisotropic liquid crystal molecules having a negative dielectric constant 14 in two directions, four directions, or many directions, that is, in target directions within one pixel. Distribution of equipotential lines is shown in Fig. 2 and Fig. 3.

[0083] As shown in Fig. 4, Fig. 5, and Fig. 6, in Example 1, liquid crystal alignment direction control electrodes 15 are arranged close to both of right and left sides of a video signal wiring 11. Since the liquid crystal alignment direction control electrode 15 shields a signal voltage variation of the video signal wiring 11, effect of the video signal wiring 11 is not transmitted to the transparent pixel electrode 8. As compared with conventional vertically aligned mode liquid crystal displays shown in Fig. 1, a vertically aligned mode liquid crystal display of the present invention of Fig. 4 generates very little perpendicular stroke. Since a width of BM (shading film (Black Matrix)) 2 of a color filter may also be set more narrowly than in conventional products, a vertically aligned mode liquid crystal display with a large aperture ratio may be realizable.

[Example. 2]

[0084] Fig. 30, Fig. 31, and Fig. 32 show sectional views of Example 2 of the present invention. In fundamental aspect, almost the same structure as in Example 1 is used for Example 2. An electrode structure of the Example has special features that two kinds of electrode structures as shown in Fig. 2 and Fig. 3 exist together in one pixel.

[0085] As shown in Fig. 30, Fig. 31, and Fig. 32, since a video signal wiring 11 is only sandwiched by transparent pixel electrodes 8 from both of right and left sides, capacitance of a video signal wiring 11 can be designed minimal, and accordingly, even if a resistance of the video signal wiring 11 is high, a problem of signal delay is hard to be generated.

[0086] Fig. 24 shows a plan view of Example 2. Only one row of liquid crystal alignment direction control electrode 15 exists in one pixel. Adjacent transparent pixel electrodes 8 are connected to a thin film transistor element 16 controlled by a different scan signal wiring 17, respectively.

[0087] As a plan view of Fig. 24 shows, since an area in which the liquid crystal alignment direction control electrode 15 exists close to a scan signal wiring 17 is small, even if the scan signal wiring 17 and the liquid crystal alignment direction control electrode 15 are simultaneously formed in the same layer, a probability that a defect in which electric short-circuit is provided by a connection of each other will occur is extremely small.

[0088] Slits 9 are formed in a direction parallel direction and a perpendicular direction to the scan signal wiring 17, and slits forming a group with a liquid crystal alignment direction control electrode 15 are extended in angle directions of ± 45 degrees to the scan signal wiring direction. Slits forming a group with a liquid crystal alignment direction control electrode may have a form like connected diamond-shapes, and may have a form like

squares located in a line as shown in Fig. 28 and Fig. 29.

[Example 3]

[0089] Fig. 7 shows a plan view of Example 3 of the present invention. The Example has a structure where two kinds of structures, a structure shown in a cross section structural figure of Example 1 and a structure shown in a cross section structural figure of Example 2, are mixed inside one pixel. In one pixel, two rows of liquid crystal alignment direction control electrodes of an upper liquid crystal alignment direction control electrode 19 and a lower liquid crystal alignment direction control electrode 20 are arranged, each potential is set as positive electrode potential and negative electrode potential on the basis of a potential of a countering flat common electrode 4 of a color filter side substrate. Adjacent transparent pixel electrodes 8 are controlled by a different liquid crystal alignment direction control electrode, respectively.

[0090] Fig. 11 and Fig. 12 show a transparent common electrode potential 21, a video signal wiring waveform 22 of odd number column, a scanning line signal waveform 23 of n row, a scanning line signal waveform 24 of (n+1) row, an upper liquid crystal alignment direction control electrode signal waveform 25 of n row, a lower liquid crystal alignment direction control electrode signal waveform 26 of n row, an upper liquid crystal alignment direction control electrode signal wave form 27 of (n+1) row, a lower liquid crystal alignment direction control electrode signal wave form 28 of (n+1) row, and a video signal wiring waveform 29 of even number column.

[0091] As shown in Fig. 11 and Fig. 12, when a signal having a positive polarity is written in a transparent pixel electrode 8, a potential of a liquid crystal alignment direction control electrode currently formed via an insulator film 12 in a lower layer of a slit 9 of the transparent pixel electrode 8 has a positive polar potential higher than a potential of the transparent pixel electrode 8, and when a signal having a negative polarity is written in the transparent pixel electrode 8, a potential of a liquid crystal alignment direction control electrode currently formed via an insulator film 12 in a lower layer of a slit 9 of the transparent pixel electrode 8 has a negative polar potential lower than a potential of the transparent pixel electrode 8.

[0092] Transparent pixel electrode 8, and liquid crystal alignment direction control electrodes 19 and 20 of two rows arranged in one pixel have exchanged polarity, respectively, every perpendicular period.

[0093] As shown in Fig. 7, slits 9 currently formed in a transparent pixel electrode 8 and liquid crystal alignment direction control electrodes 19 and 20 arranged in a lower layer of the slit are arranged so as to make angles of ± 45 degrees to a direction of a scan signal wiring 17.

[0094] In an upper half and a lower half in one pixel, the slit 9 and the liquid crystal alignment direction control electrodes 19 and 20 of a lower layer of the slit, respectively, are arranged alternately and almost in parallel each other. Special feature is that a liquid crystal alignment direction control electrode is arranged in a central part of the pixel so as to divide the upper half and the lower half. Polarizing plates are arranged so that polarization axes may become parallel and perpendicular to the scan signal wiring 17 and may have a relationship of intersecting mutually perpendicular, in an exterior of the liquid crystal cell.

[Example 4]

[0095] Fig. 8, Fig. 9, and Fig. 10 show a plan view of Example 4 of the present invention. This Example adopts a cross section structural figure of Example 1, and liquid crystal alignment direction control electrodes 19 and 20 enclose periphery of a transparent pixel electrode 8, which makes it difficult that the transparent pixel electrode 8 is influenced by a potential variation of a video signal wiring 11, and thus hardly generates a perpendicular cross talk. Moreover, since liquid crystal alignment direction control electrodes 19 and 20 and the transparent pixel electrode 8 are overlapped, a width of a shading film 2 of a color filter (BM) may be narrowed, and an aperture ratio may be increased.

[0096] In addition, liquid crystal alignment direction control electrodes 19 and 20 of two rows exist in one pixel, and thereby almost the same system as the drive system in Example 3 may be used.

[0097] In Fig. 8, slits 9 formed in the transparent pixel electrode 8 are arranged in directions of ± 45 degrees to a direction of the scan signal wirings. In Fig. 9, slits 9 formed in the transparent pixel electrode 8 are arranged in two directions perpendicular and horizontal to a direction of the scan signal wirings. In Fig. 10, fine notches of slit are formed in motion directions of liquid crystal molecules in the transparent pixel electrode 8. Arrangement of polarizing plates may be completely the same arrangement as an arrangement in Example 3.

[Example 5]

[0098] Fig. 14 shows a plan view of Example 5 of the present invention. This Example adopts a cross section structural figure of Example 1, and liquid crystal alignment direction control electrodes 19 and 20 enclose periphery of a transparent pixel electrode 8, which makes it difficult that the transparent pixel electrode 8 is influenced by a potential variation of a video signal wiring 11, and thus hardly generates a perpendicular cross talk. This Example differs from Example 4 in a point that many circular holes 37 are formed in the transparent pixel electrode 8. As long as they are holes, polygonal forms may be of any kinds other than a circular form. Liquid crystal alignment direction control electrodes 19 and 20 of two rows exist in one pixel, and the same drive system as in Example 3 may be used. Arrangement of polarizing plates may be the same arrangement as an arrangement in Example 3.

[Example 6]

[0099] Fig. 16 shows a plan view of Example 6 of the present invention. This Example has a structure where two kinds, a cross section structural figure of Example 1 and a cross section structural figure of Example 2, are mixed inside one pixel. A liquid crystal alignment direction control electrode 15 of one row is arranged in one pixel, and adjacent transparent pixel electrodes 8 are connected, respectively, with a thin film transistor element 16 currently controlled by a different scan signal wiring 17. Forms of a long and slender slit 9 currently formed in the transparent pixel electrode 8 and of the liquid crystal alignment direction control electrode 15 currently formed in a lower layer of the slit via an insulator film 12 are almost the same as in Example 3, and are arranged to make angles of $\pm$45 degrees to the direction of scan signal wiring 17.

[0100] In an upper half and a lower half in one pixel, the slit 9 and the liquid crystal alignment direction control electrode 15 formed in a lower layer of the slit, respectively, are arranged alternately and almost in parallel each other. A liquid crystal alignment direction control electrode 15 is arranged that divides an upper half and a lower half in a central part of a pixel. Polarizing plates are arranged so that polarization axes may become parallel and perpendicular to the scan signal wiring 17 and may have a relationship of intersecting mutually perpendicular, in an exterior of the liquid crystal cell.

[0101] In all Examples of the present invention, a transparent pixel electrode 8, and liquid crystal alignment direction control electrodes 15, 19, and 20 overlap mutually via the insulator film 12, and form an additional capacity (storage capacitor) . When a larger additional capacity is required, an overlapping area may be set larger. When a smaller additional capacity is required, an overlapping area may be set smaller. In an usual range, an overlapping width of about 2 micron (2 micrometers) provides a sufficient additional capacity.

[0102] Fig. 22 and Fig. 23 show a driving method of Example 6. A driving method of the Example differs from a driving method of Example 3 a little.

[0103] Fig. 22 and Fig. 23 show a transparent common electrode potential 21, a video signal wiring waveform of odd number column 22, a scanning line signal waveform of n row 23, a scanning line signal waveform of row (n+1) 24, a video signal wiring waveform of even number column 29, and a scanning line signal waveform of (n-1) row 43.

[0104] In Example 3, there is used a method that adjacent transparent pixel electrodes 8 are controlled by the same scan signal wiring 17 in Example 3, and video signals having different polarity, respectively, are written in from a video signal wiring 11. In Example 6, there is used a method that adjacent transparent pixel electrodes 8 are controlled by a different scan signal wiring 17, and video signals having the same polarity are written in after a shift of one horizontal scanning-period from a video signal wiring 11. As Fig. 22 and Fig. 23 show, when a positive signal is written in a transparent pixel electrode, a potential of a liquid crystal alignment direction control electrode has a positive polar potential higher than the transparent pixel electrode, and when a negative signal is written in the transparent pixel electrode, a potential of the liquid crystal alignment direction control electrode has a negative polar potential lower than the transparent pixel electrode. The transparent pixel electrode and the liquid crystal alignment direction control electrode reverse each polarity for every perpendicular period.

[0105] In all Examples of the present invention, it is possible to tilt molecules of anisotropic liquid crystal having a negative dielectric constant 14 in a target direction from a perpendicular direction by setting a potential difference between a transparent pixel electrode 8 and liquid crystal alignment direction control electrodes 15, 19, and 20. In this case tilt angle may only be one - two degrees from a perpendicular direction (90 degrees). Usually, a bias potential of no less than 4 - 5 V is impressed. When a high-speed response is required, it is necessary to set a tilt angle as no less than 10 degrees, and a bias potential of no less than 6 - 8 V is impressed in this case. When the present invention is used for a liquid crystal TV, it is effective to set a bias potential between a transparent pixel electrode 8 and liquid crystal alignment direction control electrodes 15, 19, and 20 larger. When the present invention is made to serve a double purpose for a viewing display for computers, and for a moving image displaying apparatus for TV, it is effective to perform a circuit design so that this bias potential may be variable.

[Example 7]

[0106] Fig. 17 and Fig. 18 show plan view of Example 7 of the present invention. This Example adopts a cross section structural figure of Example 1, a liquid crystal alignment direction control electrode 15 encloses a periphery of a transparent pixel electrode 8, which makes it difficult that the transparent pixel electrode 8 is influenced by a potential variation of a video signal wiring 11, and hardly generates a perpendicular cross talk. One row of liquid crystal alignment direction control electrode 15 exists in one pixel, and adjacent transparent pixel electrodes 8 are connected to a thin film transistor element 16 controlled by a different scan signal wiring 17, respectively. A driving method of this Example is same as in Example 6. Arrangement of polarizing plate is also same as in Example 6.

[Example 8]

[0107] Fig. 25 shows a plan view of Example 8 of the present invention. This Example adopts a cross section structural figure of Example 1, and a liquid crystal alignment direction control electrode 15 encloses a periphery of a transparent pixel electrode 8, which makes it difficult

that the transparent pixel electrode 8 is influenced by a potential variation of a video signal wiring 11, and hardly generates a perpendicular cross talk. One row of liquid crystal alignment direction control electrode 15 exists in one pixel, and adjacent transparent pixel electrodes 8 are connected to a thin film transistor element 16 controlled by a different scan signal wiring 17, respectively. A driving method of this Example is same as in Example 6. Many circular holes are formed in the transparent pixel electrode 8. As long as they are holes, polygonal forms may be of any kinds other than a circular form. A rotatory polarization liquid crystal display mode may be realizable by blending one of chiral material of left-handed rotation or right-handed rotation to an anisotropic liquid crystal having a negative dielectric constant. In this case, a value of product of a liquid crystal cell gap d and a refractive index anisotropy An should just be in a range of 0.30 - 0.60 micrometer. Molecules of anisotropic liquid crystal having a negative dielectric constant tilt aligning in a shape of a swirl, while performing a left slewing motion or a right slewing motion centering on a circular hole, can pass a light from a backlight from perpendicularly arranged polarizing plates.

[Example 9]

[0108] Fig. 20 shows a plan view of active matrix substrate of Example 9 of the present invention. Both of contact button parts of contact buttons 30, 33, and 36 of a scan signal wiring and contact buttons 38 and 39 of a liquid crystal alignment direction control electrode are gathered a in left side of a display screen. Fig. 19 shows an expansion plan view of the contact button part.

[0109] Fig. 13 shows an expansion plan view of a contact button part in the case where liquid crystal alignment direction control electrodes of two rows exist in one pixel. Fig. 13 shows an upper liquid crystal alignment direction control electrode contact button 31 of n row, a lower liquid crystal alignment direction control electrode contact button 32 of n row, an upper liquid crystal alignment direction control electrode contact button 34 of (n+1) row, and a lower liquid crystal alignment direction control electrode contact button 35 of (n+1) row. One scan signal wiring is sandwiched from both of upper side and lower side by liquid crystal alignment direction control electrodes of different rows. Polarity switching of upper-side and lower-side liquid crystal alignment direction control electrodes is simultaneously performed based on a timing as shown in Fig. 33, and thereby a potential variation of the scan signal wiring may be controlled minimal, which suppresses generation of horizontal periodic unevenness in a display screen. As Fig. 13 show, a short-circuit between contact buttons may be prevented by providing a distance between the contact buttons 30, 33, and 36 of the can signal wiring, and the contact buttons 31, 32, 34, and 35 of the liquid crystal alignment direction control electrode.

[Example 10]

[0110] Fig. 15 and Fig. 21 show a plan view of an active matrix substrate of Example 10 of the present invention. Contact buttons 30, 33, and 36 of a scan signal wiring and contact buttons 38 and 39 of a liquid crystal alignment direction control electrode are separately divided into left side and right side of a display screen, respectively. A driving method of this Example may be methods as shown in Fig. 11 and Fig. 12, and may be a method as shown in Fig. 33. In Example of the present invention, since a distance between contact buttons is expandable by adopting arrangements shown in Fig. 15 and Fig. 21, a short-circuit between contact buttons can be prevented. Furthermore, usual scan signal wiring drive IC in TN mode may be used, which enable cost reduction in development and production.

[Example 11]

[0111] Fig. 26 and Fig. 27 show a plan view of an active matrix substrate of Example 11 of the present invention. Contact buttons 30, 33, and 36 of a scan signal wiring and contact buttons 31, 32, 34, 35, 38, and 39 of a liquid crystal alignment direction control electrode are provided in both of right and left ends of a display screen, which may solve easily a problem of delay of scan signal waveform, a largest problem when driving a large-sized liquid crystal display.

[0112] In addition, Fig. 15, Fig. 20, Fig. 21, Fig. 26, and Fig. 27 show a video signal wiring terminal area 40, a pixel circumference common electrode terminal area 41, and a protection network 42 for static electricity countermeasure.

[Example 12]

[0113] Fig. 34, Fig. 35, and Fig. 38 show a sectional view, a model view, and a plan view of Example 12 of the present invention. Fig. 51 and Fig. 52 show a manufacturing process flow of a TFT (Thin Film Transistor) array substrate of Example 12 of the present invention. Fig. 63 and Fig. 64 show an expanded sectional view of the TFT array substrate.

[0114] Color filter substrate 1 has a flat transparent common electrode 4, and an active matrix substrate 13 is arranged in parallel countering this substrate 1. Although bumps 5 for controlling a motion direction of a liquid crystal are formed on a flat transparent common electrode 4 as shown in Fig. 1 in conventional liquid crystal panel in vertically aligned mode, a liquid crystal panel in vertically aligned mode of the present invention does not require such bumps.

[0115] In the active matrix substrate 1, after formation of the scan signal wiring 17, an insulator film 12 and an amorphous silicone layer (non doped layer) 65 and an n^+ amorphous silicone layer 66 for ohmic contacts are deposited. A video signal wiring 11, a drain electrode,

and a liquid crystal alignment direction control electrode 15 are simultaneously formed in the same layer after formation of a thin film transistor element part. A thin film transistor element, a video signal wiring 11, a drain electrode, and a liquid crystal alignment direction control electrode 15 are possible to be prepared in the same layer simultaneously, using a half-tone exposure technique currently disclosed in Japanese Patent Laid-Open No. 2000-066240. Fig. 64 shows a sectional view of a thin film transistor element and an active matrix substrate of Example 12 of the present invention using the half-tone exposure. In addition, Figs. 63 and 64 show a scanning line terminal area 64.

[0116] As shown in Fig. 38, in Example 12 of the present invention, a number of thin film transistor elements required in one pixel is only two. A transparent pixel electrode 8 of n row and m column is connected with a thin film transistor element 16 formed in a position where a scan signal wiring of n row 17 and a video signal wiring of m column 11 intersect with each other, and a liquid crystal alignment direction control electrode 15 is connected with a thin film transistor element 49 formed in a position where a scan signal wiring of (n-1) row 17 and a video signal wiring of (m+1) column 11 intersect with each other. Two kinds of slits are formed in the transparent pixel electrode 8, and Fig. 99 and Fig. 100 show a cross section enlargement of the slits.

[0117] In a slit 9 of type in Fig. 99, when a voltage is impressed, vertically aligned liquid crystal molecules 14 tilt in directions shown in Fig. 99. In a slit of a type in Fig. 100, a liquid crystal alignment direction control electrode 15 is arranged via an insulator film on a lower layer of the slit. In a slit of a type in Fig. 100, when a voltage is impressed, vertically aligned liquid crystal molecules 14 tilt in directions shown in Fig. 100. Fig. 41 and Fig. 42 show modified methods of Fig. 99 and Fig. 100. Fig. 41 and Fig. 42 show an opening 59 currently formed in a transparent pixel electrode on a liquid crystal alignment direction control electrode 15. In Fig. 100, the liquid crystal alignment direction control electrode 15 has a larger size than that of a slit of the transparent pixel electrode 8, and overlaps each other via an insulator film. An important point of the present invention is a point that the transparent pixel electrode 8 and the liquid crystal alignment direction control electrodes 15 overlap one another via an insulator film 12 to form a capacitance.

[0118] Molecules of anisotropic liquid crystal having a negative dielectric constant 14 may be made to move in same directions as in Fig. 100 also in an electrode structure arrangement as shown in Fig. 101, in a planar structure as shown in Fig. 93, a transparent.pixel electrode 8 and a liquid crystal alignment direction control electrodes 15 do not overlap one another, and a capacitance formed by the transparent pixel electrode 8 and the liquid crystal alignment direction control electrode 15 is small, but problems will be caused if a drive system of the present invention is used.

[0119] As shown in Fig. 94 and Fig. 95, it is particularly important in a drive system of the present invention that a transparent pixel electrode 8 and a liquid crystal alignment direction control electrodes 15 overlap at least in some area via an insulator film.

[Example 13]

[0120] Fig. 40 and Fig. 43 show a sectional view and a plan view of Example 13 of the present invention. Fig. 53 and Fig. 54 show a manufacturing process flow of a TFT array substrate of Example 13 of the present invention. Fig. 61 and Fig. 62 show an expanded sectional view of the TFT array substrate.

[0121] A color filter substrate 1 has a flat transparent common electrode 4, and does not have bumps as in Example 12.

[0122] In an active matrix substrate 13, after a scan signal wiring 17 and a liquid crystal alignment direction control electrode 15 are first formed in the same layer simultaneously, an insulator film 12, an amorphous silicone layer 65 (non doped layer), and n^+ amorphous silicone layer 66 for ohmic contacts are deposited. A video signal wiring 11 and a drain electrode are simultaneously formed after formation of a thin film transistor element part.

[0123] A thin film transistor element, a video signal wiring 11, and a drain electrode are possible to be prepared in the same layer simultaneously, using a half-tone exposure technique currently disclosed in Japanese Patent Laid-Open No.2000-066240. Fig. 62 shows a sectional view of a thin film transistor element and an active matrix substrate of Example 13 of the present invention using the half-tone exposure.

[0124] As shown in Fig. 43, in Example 13 of the present invention, a number of thin film transistor elements required in one pixel is only two. A transparent pixel electrode 8 of n row and m column is connected with a thin film transistor element 16 formed in a position where a scan signal wiring of n row 17 and a video signal wiring of m column 11 intersect with each other, and a liquid crystal alignment direction control electrode 15 is connected with a thin film transistor element 49 formed in a position where a scan signal wiring of (n-1) row 17 and a video signal wiring of (m+1) column 11 intersect with each other. In Example 12, since a drain electrode of this thin film transistor element and a liquid crystal alignment direction control electrode 15 are simultaneously formed in the same layer, these are connected automatically, but in Example 13, since a drain electrode of this thin film transistor element and a liquid crystal alignment direction control electrode 15 are not formed in the same layer, two contact holes 61 and 62 must be provided in order to electrically connect these two electrodes. Although existence of two thin film transistor elements 16 and 49 and one contact hole 56 was enough for Example 12, Example 13 requires two thin film transistor elements 16 and 49 and three contact holes 56, 61, and 62, as shown in Fig. 43.

[Example 14]

[0125] Fig. 34, Fig. 36, and Fig. 39 show a sectional view, a model view, and a plan view of Example 14 of the present invention. Fig. 55 and Fig. 56 show a manufacturing process flow of a TFT array substrate of Example 14 of the present invention.

[0126] Fig. 67 and Fig. 68 show an expanded sectional view of the TFT array substrate.

[0127] A color filter substrate 1 has a flat transparent common electrode 4, and does not have bumps as in Example 12.

[0128] In an active matrix substrate 13, after a scan signal wiring 17 and a common electrode 48 in an active matrix side are first formed in the same layer simultaneously, an insulator film 12, an amorphous silicone layer 65 (non doped layer), and n^+ amorphous silicone layer 66 for ohmic contacts are deposited. A video signal wiring 11 and a drain electrode are simultaneously formed after formation of a thin film transistor element part.

[0129] A thin film transistor element, a video signal wiring, a drain electrode, and a liquid crystal alignment direction control electrode are possible to be prepared in the same layer simultaneously, using a half-tone exposure technique currently disclosed in Japanese Patent Laid-Open No.2000-066240. Fig. 68 shows a sectional view of a thin film transistor element and an active matrix substrate of Example 14 of the present invention using the half-tone exposure.

[0130] As shown in Fig. 39, in Example 14 of the present invention, a number of thin film transistor elements required in one pixel is only two. A transparent pixel electrode 8 of n row and m column is connected with a thin film transistor element 16 formed in a position where a scan signal wiring of n row 17 and a video signal wiring of m column 11 intersect with each other, and a liquid crystal alignment direction control electrode 15 is connected with a thin film transistor element 50 formed on a scan signal wiring top 17 of (n-1) row. Although a structure of transparent pixel electrode 8 may also have forms as in Example 12 and Example 13, in Fig. 39, slits 9 formed in a transparent pixel electrode 8 are arranged horizontally and vertically to an extending direction of a scan signal wiring 17, and slits forming a group with the liquid crystal alignment direction control electrode 15 are arranged so as to make an angle of ± 45 degrees to an extending direction of the scanning line. Since a source electrode 69 of a thin film transistor element 50 formed on the scan signal wiring 17 of (n-1) row and a common electrode 48 of n row are not formed in the same layer in case of Example 14, two contact holes must be formed in order to electrically connect these two electrodes. Accordingly, like Example 13, Example 14 requires two thin film transistor elements 16 and 50 and three contact holes 56, 57, and 58, as shown in Fig. 39.

[Example 15]

[0131] Fig. 40 and Fig. 96 show a sectional view and a plan view of Example 15 of the present invention. Fig. 57 and Fig. 58 show a manufacturing process flow of a TFT array substrate of Example 15 of the present invention. Fig. 65 and Fig. 66 show an expanded sectional view of the TFT array substrate. A color filter substrate 1 has a flat transparent common electrode 4, and does not have bumps as in Example 12.

[0132] In an active matrix substrate 13, after a scan signal wiring 17, a common electrode 48, and a liquid crystal alignment direction control electrode 15 are first formed in the same layer simultaneously, an insulator film 12, an amorphous silicone layer (non doped layer) 65, and an n^+ amorphous silicone layer 66 for ohmic contacts are deposited. A video signal wiring 11 and a drain electrode are simultaneously formed after formation of a thin film transistor element part. A thin film transistor element, a video signal wiring 11, and a drain electrode are possible to be prepared in the same layer simultaneously, using a half-tone exposure technique currently disclosed in Japanese Patent Laid-Open No.2000-066240. Fig. 66 shows a sectional view of a thin film transistor element and an active matrix substrate of Example 14 of the present invention using the half-tone exposure.

[0133] As shown in Fig. 96, in Example 15 of the present invention, a number of thin film transistor elements required in one pixel is only two. A transparent pixel electrode 8 of n row and m column is connected with a thin film transistor element 16 formed in a position where a scan signal wiring of n row 17 and a video signal wiring of m column 11 intersect with each other, and a liquid crystal alignment direction control electrode 15 is connected with a thin film transistor element 50 formed on a scan signal wiring 17 top of (n-1) row. In Example 15, in order to electrically connect a source electrode 69 of the thin film transistor element formed on the scan signal wiring of (n-1) row 17, and a drain electrode 70 with a common electrode 48 and the liquid crystal alignment direction control electrode 15, respectively, contact holes 57, 58, 71, and 72, respectively, must be provided. Accordingly, Example 15 requires two thin film transistor elements 16 and 50 and five contact holes 56, 57, 58, 71, and 72 as shown in Fig. 96.

[Example 16]

[0134] Fig. 37 shows a timing chart about drive waveform that is Example 16 of the present invention. This is a drive waveform for driving a vertically aligned mode liquid crystal display described in Examples 12, 13, 14, and 15. Here may be given an important aspect of the present invention that:

a scan signal waveform of a scan signal wiring of (n-1) row (address signal width) 52 and a signal waveform of a scan signal wiring of n row (address signal width 55 have a time width of at least no less than twice of a hor-

izontal period, and mutually overlap by a time width no less than one horizontal period; and a polarity of a video signal voltage of a video signal wiring of m column and a polarity of a video signal voltage of a video signal wiring of (m+1) column have a polarity different from each other and have polarities mutually reversed every horizontal period.

[0135] Fig. 37 shows a common electrode potential 51, a video signal wiring of m column signal waveform 53, and a video signal wiring of (m+1) column signal waveform 54.

[0136] When a drive system of the present invention is used, charging may be enabled to a capacitance C2 of a circuit model figure (capacitance C2 is a capacitance formed when a transparent pixel electrode and a liquid crystal alignment direction control electrodes mutually overlap via an insulator film), when a signal waveform of a scan signal wiring of (n-1) row and a signal waveform of a scan signal wiring of n row mutually overlap, as shown in Fig. 47, Fig. 48, Fig. 49, and Fig. 50. Here, Fig. 48 shows a potential of a position shown by A and B in a circuit model figure of Fig. 47, and Fig. 50 shows a potential of a position shown by A and B in a circuit model figure of Fig. 49.

[0137] In Fig. 47 and Fig. 48 a liquid crystal alignment direction control electrode is connected with a thin film transistor element formed in a position where a video signal wiring of (m+1) column intersects a scan signal wiring of (n-1) row, a transparent pixel electrode is connected with a thin film transistor element formed in a position where a scan signal wiring of n row and a video signal wiring of m column intersect with each other. When both of scanning lines of (n-1) row and n row are addressed in case of a video signal wiring of m column having +7 V and a video signal wiring of (m+1) column having -7 V, the above-mentioned two thin film transistor elements operate, and a capacitance C2 is charged and potentials of A and B obtain +7 V and -7 V, respectively. After the scanning line of (n-1) row is closed, when a polarity of a voltage of the video signal wiring of m column is changed to -7 V from +7 V and a polarity of a voltage of the video signal wiring of (m+1) column is changed to +7 V from -7 V, since a thin film transistor element of n row is operating, a potential of A of capacitance C2 varies to -7 V from +7 V. Since a thin film transistor element of (n-1) row is not operating at this time, a potential of B of capacitance C2 varies to -21 V from -7 V. Next, when the scanning line of n row is closed, in potential of pixel of n row m column capacitance C2, A is fixed to -7 V and B to -21 V.

[0138] Same operation is performed after one perpendicular period, and since a polarity of the signal voltage of video signal wiring of m column and a polarity of the signal voltage of video signal wiring of (m+1) column are reversed, in potential of capacitance C2 after one perpendicular period, A is fixed to +7V, and B to +21V. Such potential relationship occurs, thereby a distribution of equipotential line as shown in figure are realized, and a motion direction of liquid crystal molecules may be determined. Since a large electric field is generated between the transparent pixel electrode and the liquid crystal alignment direction control electrode, large motion speed of liquid crystal molecule may be realized.

[0139] In Fig. 49 and Fig. 50, a liquid crystal alignment direction control electrode is connected with a thin film transistor element formed on a scan signal wiring of (n-1) row, and a source electrode of this thin film transistor element is connected with a common electrode of n rows. A transparent pixel electrode is connected with a thin film transistor element formed in a position where a scan signal wiring of n row and a video signal wiring of m column intersect with each other. When both of scanning lines of (n-1) row and n row are addressed in case of a video signal wiring of m column having +7 V and a video signal wiring of (m+1) column having -7 V, the above-mentioned two thin film transistor elements operate, and a capacitance C2 is charged and potentials of A and B obtain +7 V and 0 V, respectively. After the scanning line of (n-1) row is closed, when a polarity of a voltage of the video signal wiring of m column is changed to -7V from +7V and a polarity of a voltage of the video signal wiring of (m+1) column is changed to +7V from -7V, since a thin film transistor element of n row is operating, a potential of A of capacitance C2 varies to -7V from +7V. Since a thin film transistor element of (n-1) row is not operating at this time, a potential of B of capacitance C2 varies to -14V from 0 V. Next, when the scanning line of n row is closed, in potential of pixel of n row m column capacitance C2, A is fixed to -7 V and B to -21 V.

[0140] Same operation is performed after one perpendicular period, and since a polarity of the signal voltage of video signal wiring of m column and a polarity of the signal voltage of video signal wiring of (m+1) column are reversed, in potential of capacitance C2 after one perpendicular period, A is fixed to +7 V, and B to +14 V. Such potential relationships occur, thereby a distribution of equipotential line as shown in figure may be realized, and a motion direction of liquid crystal molecules may be determined.

[Example 17]

[0141] Fig. 44, Fig. 59, Fig. 60, Fig. 45, and Fig. 46 show a plan view and a sectional view of Example 17 of the present invention. Fig. 53 and Fig. 54 show a manufacturing process flow of a TFT array substrate of Example 17 of the present invention. Fig. 61 and Fig. 62 show an expanded sectional view of the TFT array substrate.

[0142] A color filter substrate 1 has a flat transparent common electrode 4, and does not have bumps as in Example 12. A connection method of a liquid crystal alignment direction control electrode 15 and a thin film transistor element is completely same as in Example 13.

[0143] In Example 17, slits formed in a transparent pixel electrode 8 has different forms from that in Example

13, they comprise a form arranged at ±45 degrees to a direction of the scan signal wirings, a form arranged horizontally or vertically, or a form having circular of polygonal openings 63, as shown in Fig. 44, Fig. 59, and Fig. 60. A liquid crystal alignment direction control electrode 15 encloses periphery of a transparent pixel electrode 8, as shown in Fig. 44, Fig. 59, and Fig. 60, and the liquid crystal alignment direction control electrode 15 forming a group with a slit is arranged horizontally or vertically to a direction of a scan signal wiring 17.

[Example 18]

[0144] Fig. 69, Fig. 70, Fig. 71, Fig. 72, Fig. 73, and Fig. 74; and Fig. 77, Fig. 78, Fig. 79, Fig. 80, Fig. 83, Fig. 84, Fig. 85, Fig. 86; and Fig. 91 and Fig. 92 show a circuit model figure of Example 18 of the present invention, and a plan view and sectional view of a thin film transistor.

[0145] Here, C1 is a capacitance formed with a transparent pixel electrode 8 and a flat transparent common electrode 4 in a CF (color filter) substrate side; C2 is a capacitance formed with the transparent pixel electrode 8 and a liquid crystal alignment direction control electrode 15; C3 is a capacitance formed with the transparent pixel electrode 8 and a scanning line; C4 is a capacitance formed with an intermediate electrode 67 of a double thin film transistor, and the transparent pixel electrode 8; and C5 is a capacitance formed with the transparent pixel electrode 8, and a common electrode 48 in an active matrix substrate side.

[0146] As already described in Example 16 of the present invention, when a drive system of the present invention is used, since a voltage impressed between electrodes of a video signal wiring of (m+1) column connected with a thin film transistor element formed on a scan signal wiring of (n-1) row and a liquid crystal alignment direction control electrode reaches about 28 V at the maximum, a problem occurs that a leakage current between these two electrodes increases. Accordingly, in Example 18 of the present invention, a double transistor structure is adopted as a structure of a thin film transistor element that is formed on a scan signal wiring 17 of (n-1) row, and is connected with a liquid crystal alignment direction control electrode 15. As shown in Fig. 91 and Fig. 92, the double transistor structure has a channel length longer than usual single transistor element, and even if a high voltage is impressed between a source electrode and a drain electrode, it can suppress increase in a leakage current. When not using a double transistor structure, it is also effective for reduction of a leakage current to lengthen a channel length of a transistor. As shown in Fig. 61 or Fig. 65, a channel length (L_2) of a thin film transistor element connected with a liquid crystal alignment direction control electrode is set larger than a channel length (L_1) of a thin film transistor element connected with a transparent pixel electrode, and thereby a leakage current may be reduced.

[0147] As a method for reducing a leakage current between a source electrode and a drain electrode, offset transistor structure as shown in Fig. 88, Fig. 89, and Fig. 90 may also be conceivable. In this case, a thin film transistor structure of a planar structure as shown in Fig. 87 is adopted. Here, notation F in Fig. 88, Fig. 89, and Fig. 90 shows amount of offset of an offset thin film transistor element. Moreover, an etching stopper layer 68 is shown in Fig. 90.

[Example 19]

[0148] Fig. 41, Fig. 42, Fig. 94, and Fig. 95 show a plan view of Example 19 of the present invention. This Example relates to a form of a transparent pixel electrode 8 and a liquid crystal alignment direction control electrode 15 used for Examples 12, 13, 14, 15, and 17. Molecules of anisotropic liquid crystal having a negative dielectric constant 14 has a property to arrange a direction of extended shaft of liquid crystal molecules 14 in a direction extending lengthwise of a wedge of a transparent pixel electrode 8 when a voltage is impressed, generation of disclination may be suppressed by adopting a form of Example 19 of the present invention.

[0149] Generation of disclination has a tendency for a transmittance of a liquid crystal panel and also for a speed of response to be reduced. A seed of response and a transmittance may be improved by adopting a form of the present invention.

[0150] Besides, as structures of a thin film transistor element of the present invention, two kinds of structures as Fig. 97 and Fig. 98 show may be conceivable. A type shown in Fig. 97 has a structure arrangement that: in a pixel of n row m column, a thin film transistor element is formed in a position where a scan signal wiring of (n-1) row and a video signal wiring of (m+1) column intersect with each other, a video signal wiring of (m+1) column, and a liquid crystal alignment direction control electrode used for the pixel of n row m column are connected via this thin film transistor element; and a thin film transistor element is formed in a position where a scan signal wiring of n row and a video signal wiring of m column intersect with each other, and the video signal wiring of m column, and a transparent pixel electrode used for the pixel of n row m column are connected via this thin film transistor element.

[0151] On the contrary, B type shown in Fig. 98 has a structure arrangement that: in a pixel of n row m column, a video signal wiring of m column and a liquid crystal alignment direction control electrode used for the pixel of n row m column are connected via a thin film transistor element in a position where a scan signal wiring of (n-1) row and a video signal wiring of m column intersect with each other; and a video signal wiring of (m+1) column and a transparent pixel electrode used for the pixel of n row m column are connected via a thin film transistor element in a position

where a scan signal wiring of n row and a video signal wiring of (m+1) column intersect with each other. The

present invention includes both of A type structure and B type structure.

[0152] Use of the present invention does not require use of color filter substrates with bumps or slits that have been used for conventional multi-domain vertically aligned mode liquid crystal displays, but enables reduction of cost. In addition, it may also cancel simultaneously display unevenness induced by variation accompanying bumps or processing of slits, and extremely improves yield.

[0153] Furthermore, it suppresses problems of unevenness, or residual image (image burn-in) caused by diffusion of impurities in pigments of a color filter, or impurities in bumps from crevices of bumps or slits into liquid crystals, and thereby realizes extremely reliable vertically aligned mode liquid crystal displays.

[0154] Since possibility of reworking may easily be realized with oxygen plasma treatment irrespective of defects generation in a polyimide alignment layer application process, reduction of reworking costs may be realized.

[0155] Use of electrode structures, structure arrangements, and driving methods of the present invention may enable production of active matrix substrates having a large aperture ratio, and may provide bright viewing displays. Furthermore, since it may improve a speed of response of liquid crystal molecules, very large-sized liquid crystal TVs responding animated pictures may be realized. In addition, it may realize a uniform black display with little light leakage in a dark room as compared with conventional vertically aligned mode liquid crystal displays using bumps.

BRIEF DESCRIPTION OF THE DRAWINGS

[0156]

Fig. 1 shows a cross section structural figure of a conventional multi-domain vertically aligned mode liquid crystal panel;

Fig. 2 shows a motion direction of molecules of anisotropic liquid crystal having a negative dielectric constant vertically aligned by an electric field formed with a flat electrode and a slit electrode;

Fig. 3 shows a motion direction of molecules of anisotropic liquid crystal having a negative dielectric constant vertically aligned by an electric field formed with a flat electrode, a slit electrode, and liquid crystal alignment direction control electrode;

Fig. 4 shows a cross section structural figure of a multi-domain vertically aligned mode liquid crystal panel of the present invention;

Fig. 5 shows a drive principle cross section structural figure of a multi-domain vertically aligned mode liquid crystal panel of the present invention (when a pixel electrode has a negative data);

Fig. 6 shows a .drive principle cross section structural figure of a multi-domain vertically aligned mode liquid crystal panel of the present invention (when a pixel electrode has a positive data);

Fig. 7 shows a plane structural figure of a multi-domain vertically aligned mode liquid crystal panel of the present invention;

Fig. 8 shows a plane structural figure of a multi-domain vertically aligned mode liquid crystal panel of the present invention;

Fig. 9 shows a plane structural figure of a multi-domain vertically aligned mode liquid crystal panel of the present invention;

Fig. 10 shows a plane structural figure of a multi-domain vertically aligned mode liquid crystal panel of the present invention;

Fig. 11 shows a waveform chart of a voltage impressed to a thin film transistor element of an odd number column of (n) th row and (n+1)th row of a multi-domain vertically aligned mode liquid crystal panel of the present invention;

Fig. 12 shows a waveform chart of a voltage impressed to a thin film transistor element of an even number column of (n)th row and (n+1) th row of a multi-domain vertically aligned mode liquid crystal panel of the present invention;

Fig. 13 shows a plan view of contact button parts of scanning lines and liquid crystal alignment direction control electrodes of a multi-domain vertically aligned mode liquid crystal panel of the present invention;

Fig. 14 shows a plane structural figure of a vertically aligned mode liquid crystal panel of the present invention;

Fig. 15 shows a plan view of a vertically aligned mode active matrix substrate of the present invention;

Fig. 16 shows a plane structural figure of a multi-domain vertically aligned mode liquid crystal panel of the present invention;

Fig. 17 shows a plane structural figure of a multi-domain vertically aligned mode liquid crystal panel of the present invention;

Fig. 18 shows a plane structural figure of a multi-domain vertically aligned mode liquid crystal panel of the present invention;

Fig. 19 shows a plan view of contact button parts of scanning lines and liquid crystal alignment direction control electrodes of a multi-domain vertically aligned mode liquid crystal panel of the present invention;

Fig. 20 shows a plan view of a vertically aligned mode active matrix substrate of the present invention;

Fig. 21 shows a plan view of a vertically aligned mode active matrix substrate of the present invention;

Fig. 22 shows a waveform of a voltage impressed to a thin film transistor element corresponding to a pixel of an odd number column of (n)th row and of (n+1) th row of a multi-domain vertically aligned mode liquid crystal panel of the present invention;

Fig. 23 shows a waveform of a voltage impressed to

a thin film transistor element corresponding to a pixel of an even number column of (n)th row and of (n+1) th row of a multi-domain vertically aligned mode liquid crystal panel of the present invention;

Fig. 24 shows a plane structural figure of a multi-domain vertically aligned mode liquid crystal panel of the present invention;

Fig. 25 shows a plane structural figure of a multi-domain vertically aligned mode liquid crystal panel of the present invention;

Fig. 26 shows a plan view of a vertically aligned mode active matrix substrate of the present invention;

Fig. 27 shows a plan view of a vertically aligned mode active matrix substrate of the present invention;

Fig. 28 shows a plan view and a cross section structural figure of slits formed in a liquid crystal alignment direction control electrode and a transparent pixel electrode of the present invention;

Fig. 29 shows a plan view and a cross section structural figure of slits formed in a liquid crystal alignment direction control electrode and a transparent pixel electrode of the present invention;

Fig. 30 shows a cross section structural figure of a multi-domain vertically aligned mode liquid crystal panel of the present invention;

Fig. 31 shows a drive principle cross section structural figure of a multi-domain vertically aligned mode liquid crystal panel of the present invention (when a pixel electrode has a negative data);

Fig. 32 shows a drive principle cross section structural figure of a multi-domain vertically aligned mode liquid crystal panel of the present invention (when pixel electrode has a positive data);

Fig. 33 shows a waveform chart of a voltage impressed to a thin film transistor element of an odd number column (n)th row, and (n+1)th row of a multi-domain vertically aligned mode liquid crystal panel of the present invention;

Fig. 34 shows a cross section structural figure of a multi-domain vertically aligned mode liquid crystal panel of the present invention;

Fig. 35 shows a plane structural figure of a multi-domain vertically aligned mode liquid crystal panel of the present invention;

Fig. 36 shows a plane structural figure of a multi-domain vertically aligned mode liquid crystal panel of the present invention;

Fig. 37 shows a drive voltage waveform of a multi-domain vertically aligned mode liquid crystal panel of the present invention;

Fig. 38 shows a plane structural figure of a multi-domain vertically aligned mode liquid crystal panel of the present invention;

Fig. 39 shows a plane structural figure of a multi-domain vertically aligned mode liquid crystal panel of the present invention;

Fig. 40 shows a cross section structural figure of a multi-domain vertically aligned mode liquid crystal panel of the present invention;

Fig. 41 shows a plane structural figure of slits formed in a liquid crystal alignment direction control electrode and a transparent pixel electrode of the present invention;

Fig. 42 shows a plane structural figure of slits formed in a liquid crystal alignment direction control electrode and a transparent pixel electrode of the present invention;

Fig. 43 shows a plane structural figure of a multi-domain vertically aligned mode liquid crystal panel of the present invention;

Fig. 44 shows a plane structural figure of a multi-domain vertically aligned mode liquid crystal panel of the present invention;

Fig. 45 shows a cross section structural figure of a multi-domain vertically aligned mode liquid crystal panel of the present invention;

Fig. 46 shows a cross section structural figure of a multi-domain vertically aligned mode liquid crystal panel of the present invention;

Fig. 47 shows a circuit model figure of a multi-domain vertically aligned mode liquid crystal panel of the present invention;

Fig. 48 shows a table showing potentials of A and B in the circuit model figure of Fig. 47;

Fig. 49 shows a circuit model figure of a multi-domain vertically aligned mode liquid crystal panel of the present invention;

Fig. 50 shows a table showing potentials of A and B in the circuit model figure of Fig. 47;

Fig. 51 shows a description of a flow of five-photo-mask-process for a multi-domain vertically aligned mode liquid crystal panel manufacturing of the present invention;

Fig. 52 shows a description of a flow of four-photo-mask-process for a multi-domain vertically aligned mode liquid crystal panel manufacturing of the present invention;

Fig. 53 shows a description of a flow of five-photo-mask-process for a multi-domain vertically aligned mode liquid crystal panel manufacturing of the present invention;

Fig. 54 shows a description of a flow of four-photo-mask-process for a multi-domain vertically aligned mode liquid crystal panel manufacturing of the present invention;

Fig. 55 shows a description of a flow of five-photo-mask-process for a multi-domain vertically aligned mode liquid crystal panel manufacturing of the present invention;

Fig. 56 shows a description of a flow of four-photo-mask-process for a multi-domain vertically aligned mode liquid crystal panel manufacturing of the present invention;

Fig. 57 shows a description of a flow of five-photo-mask-process for a multi-domain vertically aligned mode liquid crystal panel manufacturing of the

present invention;
Fig. 58 shows a description of a flow of four-photo-mask-process for a multi-domain vertically aligned mode liquid crystal panel manufacturing of the present invention;
Fig. 59 shows a plane structural figure of a multi-domain vertically aligned mode liquid crystal panel of the present invention;
Fig. 60 shows a plane structural figure of a multi-domain vertically aligned mode liquid crystal panel of the present invention;
Fig. 61 shows a cross section structural figure of a multi-domain vertically aligned mode liquid crystal panel of the present invention;
Fig. 62 shows a cross section structural figure of a multi-domain vertically aligned mode liquid crystal panel of the present invention;
Fig. 63 shows a cross section structural figure of a multi-domain vertically aligned mode liquid crystal panel of the present invention;
Fig. 64 shows a cross section structural figure of a multi-domain vertically aligned mode liquid crystal panel of the present invention;
Fig. 65 shows a cross section structural figure of a multi-domain vertically aligned mode liquid crystal panel of the present invention;
Fig. 66 shows a cross section structural figure of a multi-domain vertically aligned mode liquid crystal panel of the present invention;
Fig. 67 shows a cross section structural figure of a multi-domain vertically aligned mode liquid crystal panel of the present invention;
Fig. 68 shows a cross section structural figure of a multi-domain vertically aligned mode liquid crystal panel of the present invention;
Fig. 69 shows a circuit model figure of a multi-domain vertically aligned mode liquid crystal panel of the present invention;
Fig. 70 shows a circuit model figure of a multi-domain vertically aligned mode liquid crystal panel of the present invention;
Fig. 71 shows a circuit model figure of a multi-domain vertically aligned mode liquid crystal panel of the present invention;
Fig. 72 shows a circuit model figure of a multi-domain vertically aligned mode liquid crystal panel of the present invention;
Fig. 73 shows a circuit model figure of a multi-domain vertically aligned mode liquid crystal panel of the present invention;
Fig. 74 shows a circuit model figure of a multi-domain vertically aligned mode liquid crystal panel of the present invention;
Fig. 75 shows a partial plan view of a multi-domain vertically aligned mode liquid crystal panel of the present invention;
Fig. 76 shows a partial plan view of a multi-domain vertically aligned mode liquid crystal panel of the present invention;
Fig. 77 shows a partial plan view of a multi-domain vertically aligned mode liquid crystal panel of the present invention;
Fig. 78 shows a partial plan view of a multi-domain vertically aligned mode liquid crystal panel of the present invention;
Fig. 79 shows a partial plan view of a multi-domain vertically aligned mode liquid crystal panel of the present invention;
Fig. 80 shows a partial plan view of a multi-domain vertically aligned mode liquid crystal panel of the present invention;
Fig. 81 shows a partial plan view of a multi-domain vertically aligned mode liquid crystal panel of the present invention;
Fig. 82 shows a partial plan view of a multi-domain vertically aligned mode liquid crystal panel of the present invention;
Fig. 83 shows a partial plan view of a multi-domain vertically aligned mode liquid crystal panel of the present invention;
Fig. 84 shows a partial plan view of a multi-domain vertically aligned mode liquid crystal panel of the present invention;
Fig. 85 shows a partial plan view of a multi-domain vertically aligned mode liquid crystal panel of the present invention;
Fig. 86 shows a partial plan view of a multi-domain vertically aligned mode liquid crystal panel of the present invention;
Fig. 87 shows a plan view of an offset thin film transistor element for multi-domain vertically aligned mode liquid crystal panels of the present invention;
Fig. 88 shows a sectional view of an offset thin film transistor element for multi-domain vertically aligned mode liquid crystal panels of the present invention;
Fig. 89 shows a sectional view of an offset thin film transistor element for multi-domain vertically aligned mode liquid crystal panels of the present invention;
Fig. 90 shows a sectional view of an offset thin film transistor element for multi-domain vertically aligned mode liquid crystal panels of the present invention;
Fig. 91 shows a sectional view of a double gate thin film transistor element for multi-domain vertically aligned mode liquid crystal panels of the present invention;
Fig. 92 shows a sectional view of a double gate thin film transistor element for multi-domain vertically aligned mode liquid crystal panels of the present invention;
Fig. 93 shows a plane structural figure of slits formed in a liquid crystal alignment direction control electrode and a transparent pixel electrode of the present invention;
Fig. 94 shows a plane structural figure of slits formed in a liquid crystal alignment direction control electrode and a transparent pixel electrode of the present

invention;

Fig. 95 shows a plane structural figure of slits formed in a liquid crystal alignment direction control electrode and a transparent pixel electrode of the present invention;

Fig. 96 shows a plane structural figure of a multi-domain vertically aligned mode liquid crystal panel of the present invention;

Fig. 97 shows a plane structural figure of a multi-domain vertically aligned mode liquid crystal panel of the present invention;

Fig. 98 shows a plane structural figure of a multi-domain vertically aligned mode liquid crystal panel of the present invention;

Fig. 99 shows a motion direction of molecules of anisotropic liquid crystal having a negative dielectric constant vertically aligned by an electric field formed with a flat electrode and a slit electrode;

Fig. 100 shows a motion direction of molecules of anisotropic liquid crystal having a negative dielectric constant vertically aligned by an electric field formed with a flat electrode, a slit electrode, and a liquid crystal alignment direction control electrode; and

Fig. 101 shows a motion direction of molecules of anisotropic liquid crystal having a negative dielectric constant vertically aligned by an electric field formed with a flat electrode, a slit electrode, and a liquid crystal alignment direction control electrode.

[Description of Notations]

[0157]

1 Color filter side glass substrate.
2 Black mask (shading film).
3 Color filter layer.
4 Color filter side transparent electric conductive film (transparent common electrode).
5 Bump for directional control of vertically aligned liquid crystal molecule.
6 Color filter side vertical alignment film.
7 Active matrix substrate side vertical alignment film.
8 Transparent pixel electrode.
9 Slit opening formed in pixel electrode side.
10 Passivation film.
11 Video signal wiring.
12 Gate insulator film.
13 Active matrix element side glass substrate.
14 Anisotropic liquid crystal molecules having a negative dielectric constant.
15 Liquid crystal alignment direction control electrode.
16 Thin film transistor element connected to a transparent pixel electrode.
17 Scan signal wiring.
18 Contact through hole.
19 Upper liquid crystal alignment direction control electrode.
20 Lower liquid crystal alignment direction control electrode.
21 Transparent common electrode potential.
22 Odd number column video signal wiring waveform.
23 Scanning line signal wave type of n row.
24 Scanning line signal wave type of (n+1) row.
25 Upper liquid crystal alignment direction control electrode signal waveform of n row.
26 Lower liquid crystal alignment direction control electrode signal waveform of n row.
27 Upper liquid crystal alignment direction control electrode signal waveform of (n+1) row.
28 Lower liquid crystal alignment direction control electrode signal waveform of (n+1) row.
29 Even number column video signal wiring waveform.
30 Scanning line contact button of (n-1) row.
31 Upper liquid crystal alignment direction control electrode contact button n row.
32 Lower liquid crystal alignment direction control electrode contact button of n row.
33 Scanning line contact button of n row.
34 Upper liquid crystal alignment direction control electrode contact button of (n+1) row.
35 Lower liquid crystal alignment direction control electrode contact button of (n+1) row.
36 Scanning line contact button of (n+1) row.
37 Hole opening formed in pixel electrode side.
38 Liquid crystal alignment direction control electrode contact button of (n-1) row.
39 Liquid crystal alignment direction control electrode contact button n row.
40 Video signal wiring terminal.
41 Pixel circumference common electrode terminal.
42 Protection network for static electricity measure.
43 Scanning line signal waveform of (n-1) row.
44 Liquid crystal alignment direction control electrode signal waveform of n row.
45 Liquid crystal alignment direction control electrode signal waveform of (n+1) row.
48 Common electrode of active matrix substrate side.
49 Thin film transistor element connected to liquid crystal alignment direction control electrode.
50 Thin film transistor connected to common electrode and liquid crystal alignment direction control electrode.
51 Common electrode potential.
52 Scanning line signal waveform of (n-1) row.
53 Video signal wiring signal waveform of m column.
54 Video signal wiring signal waveform of (m+1) column.
55 Scanning line signal waveform of n row.
56 Contact hole for connecting transparent pixel electrode and drain electrode of transistor.
57 Contact hole for connecting common electrode and source electrode of transistor.

58 Contact hole for connecting common electrode and source electrode of transistor.
59 Opening formed in transparent pixel electrode on liquid crystal alignment direction control electrode.
60 Drain electrode of thin film transistor element.
61 Contact hole for connecting liquid crystal alignment direction control electrode and drain electrode of transistor.
62 Contact hole for connecting liquid crystal alignment direction control electrode and drain electrode of transistor.
63 Square opening formed in transparent pixel electrode.
64 Scanning line terminal.
65 Non doped thin film semiconductor layer.
66 n+a-Si layer (ohmic contact layer).
C1 Capacitance formed by transparent pixel electrode and flat transparent common electrode of CF (color filter) substrate side.
C2 Capacitance formed by transparent pixel electrode and liquid crystal alignment direction control electrode.
C3 Capacitance formed by transparent pixel electrode and scanning line.
C4 Capacitance formed by intermediate electrode and transparent pixel electrode of double thin film transistor.
C5 Capacitance formed by transparent pixel electrode and common electrode of active matrix substrate side.
67 Intermediate electrode of double thin film transistor.
68 Etching stopper layer.
F Amount of offset of offset thin film transistor element.
69 Source electrode (connected with common electrode).
70 Drain electrode (connected with liquid crystal alignment direction control electrode).
71 Contact hole for connecting liquid crystal alignment direction control electrode and drain electrode of transistor.
72 Contact hole for connecting liquid crystal alignment direction control electrode and drain electrode of transistor.

Claims

1. A color active matrix type vertically aligned mode liquid crystal display comprising an active matrix substrate (13) having formed thereon:

a scan signal wiring (17);
a video signal wiring (11);
a thin film transistor (16) which is provided at an intersection of the scan signal wiring and the video signal wiring;
a transparent pixel electrode (8) which is connected to the thin film transistor element and in which two or more long and slender slits (9) are provided; and
a liquid crystal alignment direction control electrode (15) arranged in a layer below the transparent pixel electrode provided via an insulator film (12);
the liquid crystal display further comprising:

a color filter substrate (1) facing the active matrix substrate, and
an anisotropic liquid crystal layer having a negative dielectric constant sandwiched by the active matrix substrate and the color filter substrate,
wherein a transparent flat common electrode (4) is provided on the color filter substrate side; and wherein,
in order to impress a voltage to liquid crystal molecules (14) vertically aligned between the active matrix substrate and the color filter substrate, and to make the liquid crystal molecules tilt in two or four different directions, two kinds of the following electrode structures are provided in a pixel of the active matrix substrate:

a first electrode structure facing the transparent flat common electrode and formed on the active matrix substrate side by those of the long and slender slits in the transparent pixel electrode under which no liquid crystal alignment direction control electrode is formed;
a second electrode structure facing the transparent flat common electrode and formed on the active matrix substrate side by those of the long and slender slits in the transparent pixel electrode under which a liquid crystal alignment direction control electrode is formed and by the corresponding liquid crystal alignment direction control electrode (15) which has a larger dimension than the dimension of the slits;
characterized in that
for each row of pixels, one or two rows of crystal alignment direction control electrodes are provided,
the different rows of liquid crystal alignment direction control electrodes are connected to output terminals of different drive ICs, respectively; and
separate drive for every row of liquid crystal alignment direction control electrodes is provided.

2. The display according to claim 1, **characterized in that**
for the second electrode structure, two rows of liquid crystal alignment direction control electrodes (19, 20) that are mutually separated and arranged to be set to electric potentials different from each other exist in a layer below the transparent pixel electrode (8) via the insulated film (12),
either of the liquid crystal alignment direction control electrodes has a larger dimension than the dimension of the slits (9), and
the two rows of the liquid crystal alignment direction control electrodes are arranged in the direction of the scan signal wiring (17).

3. The display according to claim 1, **characterized in that**
the transparent pixel electrode (8) has two or more of circular or polygonal holes (37) and two or more long and slender slits (9) provided therein,
the two kinds of electrode structures are provided in order to make the liquid crystal molecules tilt in many directions, and
the first electrode structure is formed by circular or polygonal holes in the transparent electrodes.

4. The display according to claim 3, **characterized in that** for the second electrode structure, two rows of liquid crystal alignment direction control electrodes (19,20) that are mutually separated and arranged to be set to electric potentials different from each other exist in a layer below the transparent pixel electrode (8) via the insulated film (12),
either of the liquid crystal alignment direction control electrodes have a larger dimension than the dimension of the slit (9); and
the two rows of the liquid crystal alignment direction control electrodes are arranged in the direction of the scan signal wiring (17).

5. The display according to any one of claims 1 to 4, **characterized in that**
adjacent transparent pixel electrodes (8) in the direction of the scan signal wiring (17) are connected to thin film transistor components (16) controlled by different scan signal wirings, respectively.

6. The display according to any one of the preceding claims,
characterized in that
a slit (9) provided in the transparent pixel electrode (8) on the active matrix substrate (13) side and extending long and slender, and a slit belonging to the second electrode structure are arranged alternately, maintaining a parallel relationship in a direction making about ±45 degrees to the direction of the scan signal wiring (17); or
characterized in that
there is adopted a structure that slits (9) provided in the transparent pixel electrode (8) on the active matrix substrate (13) side and extending long and slender are arranged in a direction making ±45 degrees to the direction of the scan signal wiring (17);
slits belonging to the second electrode structure are arranged in a parallel direction and in a perpendicular direction to the direction of the scan signal wiring; and
the liquid crystal alignment direction control electrode encloses a periphery of the transparent pixel electrode while overlapping with the transparent pixel electrode via the insulated film (12); or
characterized in that
there is adopted a structure that a slit (9) provided in a transparent pixel electrode (8) on an active matrix substrate (13) side and extending long and slender is arranged in a parallel direction and in a perpendicular direction to the scan signal wiring direction (17);
a slit belonging to the second electrode structure is arranged in parallel to the scan signal wiring direction; and
the liquid crystal alignment direction control electrode encloses a periphery of the transparent pixel electrode while overlapping with the transparent pixel electrode via the insulated film (12); or
characterized in that
there is adopted a structure that slits (9) provided in the transparent pixel electrode (8) on the active matrix substrate side (13) and extending long and slender are arranged in a parallel direction and in a perpendicular direction to the scan signal wiring direction (17); and
slits belonging to the second electrode structure are arranged in a direction making ±45 degrees to the direction of a scan signal wiring.

7. The display according to claim 3, 4 or 5, **characterized in that**
there is adopted a structure that slits (9) belonging to the second electrode structure are arranged in a parallel direction and in a perpendicular direction to the direction of the scan signal wiring so as to enclose two or more of circular or polygonal holes (37) provided in the transparent pixel electrode on the active matrix substrate side (13); and
the liquid crystal alignment direction control electrode encloses a periphery of the transparent pixel electrode (8) while overlapping with the transparent pixel electrode via the insulated film (12).

8. The display according to any one of the preceding claims,
characterized in that
the liquid crystal alignment direction control electrode (15) is provided in the same layer as the scan signal wiring (17); and/or
characterized in that

additional capacitance is provided with the liquid crystal alignment direction control electrode and the transparent pixel electrode.

9. The display according to claim 2 or 4, **characterized in that**
both of contact buttons (30, 33, 36, 38, 39) of the scan signal wiring (17) and the liquid crystal alignment direction control electrodes (15) are arranged on either of a first side or a second side of the display screen part, and contact buttons of two rows of the liquid crystal alignment direction control electrode for controlling one row of pixels are arranged so that they may be sandwiched between the contact buttons of the scan signal wiring; or
characterized in that
contact buttons (30, 33, 36, 38, 39) for both of the scan signal wiring (17) and the liquid crystal alignment direction control electrodes (15) are arranged on both of the second and the first sides of the display screen part, and contact buttons of two rows of the liquid crystal alignment direction control electrode for controlling one row of pixels are arranged so that they may be sandwiched between the contact buttons of the scan signal wiring.

10. The display according to claim 5, **characterized in that**
both of contact buttons (30, 33, 36, 38, 39) of the scan signal wiring (17) and the liquid crystal alignment direction control electrodes (15) are arranged on either of a first side or a second side of the display screen part, and contact buttons of one row of the liquid crystal alignment direction control electrode for controlling one row of pixels are arranged so that they may be sandwiched between the contact buttons of the scan signal wiring; or
characterized in that
contact buttons (30, 33, 36, 38, 39) for both of the scan signal wiring (17) and the liquid crystal alignment direction control electrodes (15) are arranged on both of the second and the first sides of the display screen part, and contact buttons of one row of the liquid crystal alignment direction control electrode for controlling one row of pixels are arranged so that they may be sandwiched between the contact buttons of the scan signal wiring.

11. The display according to any one of claims 1 to 5, **characterized in that**
contact buttons (30, 33, 36,) of the scan signal wiring are arranged on either of a first side or a second side of the display screen part, and contact buttons (38, 39) of the liquid crystal alignment direction control electrode (15) are arranged on another side different from the side of the contact buttons of the scan signal wiring.

12. A method of driving the display according to claim 11, **characterized in that**
at the time of moving image displaying, a bias voltage impressed between the liquid crystal alignment direction control electrode (15) and the transparent pixel electrode is set higher than a voltage at the time of still picture displaying, and thereby, a tilting speed of the anisotropic liquid crystal molecules having a negative dielectric constant are set higher.

13. A method of driving the display according to any one of claims 1 to 5, **characterized in that**
when the electric potential of the transparent pixel electrode (8) separated for every pixel on the active matrix substrate (13) side is lower than the electric potential of the facing flat common electrode (4) on the color filter substrate (1) side, the electric potential of the liquid crystal alignment direction control electrode (15) is set lower than the electric potential of the transparent pixel electrode;
when the electric potential of the transparent pixel electrode is higher than the electric potential of the facing flat common electrode on the color filter substrate side, the electric potential of the liquid crystal alignment direction control electrode is set higher than the electric potential of the transparent pixel electrode; and
the polarities of the electric potential of the transparent pixel electrode, and the electric potential of the liquid crystal alignment direction control electrode are reversed to the polarity of the electric potential of the flat common electrode on the color filter substrate side every vertical scanning period.

14. The method according to claim 13 for driving the display according to claim 2 or 4, **characterized in that**
the electric potentials of the liquid crystal alignment direction control electrodes arranged in the vicinity of both sides of the scan signal wiring are set as electric potentials with a polarity different from each other; and
each of the electric potentials of the two rows of the liquid crystal alignment direction control electrodes mutually separated in one pixel are reversed to the polarity of the electric potential of the flat common electrode on the color filter substrate side every vertical scanning period.

15. A color active matrix type vertically aligned mode liquid crystal display comprising an active matrix substrate (13) having formed thereon:

a scan signal wiring (17);
a video signal wiring (11);
a thin film transistor (16) which is provided at an intersection of the scan signal wiring and the video signal wiring;
a transparent pixel electrode (8) which is con-

nected to the thin film transistor element and in which two or more long and slender slits (9) are provided; and
a liquid crystal alignment direction control electrode (15) in a layer below the transparent pixel electrode provided via an insulator film (12);
the liquid crystal display further comprising:

a color filter substrate (1) facing the active matrix substrate, and
an anisotropic liquid crystal layer having a negative dielectric constant sandwiched by the active matrix substrate and the color filter substrate,
wherein a transparent flat common electrode (4) is provided on the color filter substrate side; and wherein,
in order to impress a voltage to liquid crystal molecules (14) vertically aligned between the active matrix substrate and the color filter substrate, and to make the liquid crystal molecules tilt in two or four different directions, two kinds of the following electrode structures are provided in a pixel of the active matrix substrate:

a first electrode structure facing the transparent flat common electrode and formed on the active matrix substrate side by those of the long and slender slits in the transparent pixel electrode under which no liquid crystal alignment direction control electrode is formed;
a second electrode structure facing the transparent flat common electrode and formed on the active matrix substrate side by those of the long and slender slits in the transparent pixel electrode under which a liquid crystal alignment direction control electrode is formed and by the corresponding liquid crystal alignment direction control electrode (15) which has a larger dimension than the dimension of the slits;
characterized in that
in a pixel of n row m column, a first thin film transistor element (49) is formed in a position where the scan signal wiring (17) of (n-1) row and the video signal wiring (11) of (m+1) column intersect with each other, and the video signal wiring of (m+1) column and the liquid crystal alignment direction control electrode (15) used for the pixel of n row m column are connected via the first thin film transistor element; and
a second thin film transistor element (16) is formed in a position where the scan signal wiring of n row and the video signal wiring of m column intersect with each other, and the video signal wiring of m column and the transparent pixel electrode used for the pixel of n row m column are connected via the second thin film transistor element.

16. A color active matrix type vertically aligned mode liquid crystal display comprising an active matrix substrate (13) having formed thereon:

a scan signal wiring (17);
a video signal wiring (11);
a thin film transistor (16) which is provided at an intersection of the scan signal wiring and the video signal wiring;
a transparent pixel electrode (8) which is connected to the thin film transistor element and in which two or more long and slender slits (9) are provided; and
a liquid crystal alignment direction control electrode (15) in a layer below the transparent pixel electrode provided via an insulator film (12);
the liquid crystal display further comprising:

a color filter substrate (1) facing the active matrix substrate and
an anisotropic liquid crystal layer having a negative dielectric constant sandwiched by the active matrix substrate and the color filter substrate,
wherein a transparent flat common electrode (4) is provided on the color filter substrate side; and wherein,
in order to impress a voltage to liquid crystal molecules (14) vertically aligned between the active matrix substrate and the color filter substrate, and to make the liquid crystal molecules tilt in two or four different directions, two kinds of the following electrode structures are provided in a pixel of the active matrix substrate:

a first electrode structure facing the transparent flat common electrode and formed on the active matrix substrate side by those of the long and slender slits in the transparent pixel electrode under which no liquid crystal alignment direction control electrode is formed;
a second electrode structure facing the transparent flat common electrode and formed on the active matrix substrate side by those of the long and slender slits in the transparent pixel electrode under which a liquid crystal alignment direction control electrode is formed

and by the corresponding liquid crystal alignment direction control electrode (15) which has a larger dimension than the dimension of the slits;
characterized in that
a common electrode wiring (48) is provided on the active matrix substrate side extending in a direction parallel to the scan signal wiring (17),
in the pixel of n row m column, a first thin film transistor element (50) is formed on the scan signal wiring (17) of (n-1) row, and the common electrode wiring (48) of n row and the liquid crystal alignment direction control electrode (15) used for the pixel of n row m column are connected via the first thin film transistor element, and
a second thin film transistor element (16) is formed in a position where the scan signal wiring of n row and the video signal wiring (11) of m column intersect with each other, and the video signal wiring of m column and the transparent pixel electrode (8) used for the pixel of n row m column are connected via the second thin film transistor element.

17. The display according to claim 15, **characterized in that**
the transparent pixel electrode (8) has two or more of circular or polygonal holes (37) and two or more long and slender slits (9) provided therein,
the two kinds of electrode structures are provided in order to make the liquid crystal molecules tilt in many directions, and
the first electrode structure is formed by circular or polygonal holes in the transparent electrodes.

18. The display according to claim 16, **characterized in that**
the transparent pixel electrode (8) has two or more of circular or polygonal holes (37) and two or more long and slender slits (9) provided therein,
the two kinds of electrode structures are provided in order to make the liquid crystal molecules tilt in many directions, and
the first electrode structure is formed by circular or polygonal holes in the transparent electrodes.

19. A method of driving the display according to any one of claims 15 to 18, **characterized in that**
the time width of the scan signal waveform in the scan signal wiring (17) is no less than twice of the horizontal period,
the scan signal waveform in the scan signal wiring of (n-1)th row and the scan signal waveform in the scan signal wiring of (n)th row overlap one another by no less than one time of the horizontal period, and the polarities of the video signal voltage of the video signal wiring (11) of m column, and the video signal voltage of the video signal wiring of (m+1) column are different from each other, and the polarities being mutually exchanged every horizontal period, and the polarities being mutually reversed every vertical period.

20. The display according to claim 15 or 17, **characterized in that**
the channel length (L_2) of the first thin film transistor element (49) that is formed in a position where the scan signal wiring (17) of (n-1) row and the video signal wiring (11) of column (m+1) intersect with each other, and is connected with the liquid crystal alignment direction control electrode (15) is larger than a channel length (L_1) of the second thin film transistor element (16) that is formed in a position where the scan signal wiring of n row and the video signal wiring of m column intersect with each other, and is connected with the transparent pixel electrode ($L_1 < L_2$).

21. The display according to claim 16 or 18, **characterized in that**
the channel length (L_2) of the first thin film transistor element (50) that is formed on the scan signal wiring of (n-1) row, and is connected with the liquid crystal alignment direction control electrode (15) is larger than the channel length (L_1) of the second thin film transistor element (16) that is formed in a position where the scan signal wiring of n row and the video signal wiring of m column intersect with each other, and is connected with the transparent pixel electrode ($L_1 < L_2$).

22. The display according to any one of claims 15 to 21, **characterized in that**
a double transistor element structure or an offset channel element structure is used for the thin film transistor element (16) connected with the liquid crystal alignment direction control electrode (15).

23. The display according to claim 15 or 16, **characterized in that**
a slit (9) formed in the transparent pixel electrode (8) on the active matrix substrate (13) side and extending long and slender, and a slit belonging to the second electrode structure are arranged alternately, maintaining a relationship parallel to each other in an angle direction of about $\pm$45 degrees to the extending direction of the scan signal wiring (17); or
characterized in that
a slit (9) formed in the transparent pixel electrode (8) on the active matrix substrate (13) side and extending long and slender are arranged substantially in a parallel direction and in a perpendicular direction to

the extending direction of the scan signal wiring (17); and a slit belonging to the second electrode structure is arranged in a angle direction of about ±45 degrees to the direction of the scan signal wirings; or
characterized in that
a slit (9) formed in the transparent pixel electrode (8) on the active matrix substrate (13) side and extending long and slender is arranged in an angle direction of about ±45 degrees to the extending direction of the scan signal wiring (17); and a slit belonging to the second electrode structure is arranged in a parallel direction and in a perpendicular direction to the extending direction of the scan signal wiring; and the liquid crystal alignment direction control electrode encloses a periphery of the transparent pixel electrode while overlapping with the transparent pixel electrode via the insulated film (12).

24. The display according to claim 17 or 18, **characterized in that**
a slit (9) belonging to the second electrode structure is arranged in a parallel direction and in a perpendicular direction to the extending direction of the scan signal wiring (17) so that two or more circular or polygonal holes (37) formed in the transparent pixel electrode (8) in the active matrix substrate side are surrounded; and the liquid crystal alignment direction control electrode encloses a periphery of the transparent pixel electrode while overlapping with a he transparent pixel electrode via the insulated film (12).

25. The display according to any one of claims 15 to 24, **characterized in that**
the liquid crystal alignment direction control electrode (15) is formed in the same layer as the scan signal wiring (17) ; or
characterized in that
the liquid crystal alignment direction control electrode (15) is formed in the same layer as the video signal wiring (11).

26. The display according to any one of claims 15 to 18, **characterized in that**
two thin film transistor elements (16) are required in one pixel in order to drive the one pixel and only one contact hole (18) exists for electrically connecting the drain electrode of a thin film transistor element formed in a position where the scan signal wiring (17) of n row and the video signal wiring (11) of m column intersect with each other, and the transparent pixel electrode (8); or
characterized in that
two thin film transistor elements (16) are required in one pixel in order to drive the one pixel; two contact holes (61, 62) exist for electrically connecting the drain electrode of a thin film transistor element formed in a position where the scan signal wiring (17) of (n-1) row and the video signal wiring (11) of (m+1) column intersect with each other, and the liquid crystal alignment direction control electrode (15); and only one contact hole (18) exists for electrically connecting the drain electrode of a thin film transistor element formed in a position where the scan signal wiring of n row and the video signal wiring of m column intersect with each other, and the transparent pixel electrode (8); or
characterized in that
two thin film transistor elements (16) are required in one pixel in order to drive the one pixel; and one thin film transistor element is connected to the transparent pixel electrode (8), another remaining thin film transistor element is connected to the liquid crystal alignment direction control electrode (15), and the transparent pixel electrode and the liquid crystal alignment direction control electrode are overlapped via the insulated film (12) to form a capacitance.

27. The display according to any one of claims 15 to 26, **characterized in that**
an intermediate electrode (67) of the first thin film transistor element connected with the liquid crystal alignment direction control electrode (15) and the transparent pixel electrode (8) overlap via the insulated film (12) to form a capacitance, and the first thin film transistor is having a double transistor structure.

28. The display according to claim 15 or 17, **characterized in that**
the transparent pixel electrode (8) of n row and m column and the scan signal wiring (17) of (n-1)th row overlap one another via the insulated film (12) to form a storage capacitor.

29. The display according to claim 16 or 18, **characterized in that**
the transparent pixel electrode (8) of n row and m column and the common electrodes wiring (48) of n row overlap one another via the insulated (12) film to form a storage capacitor.

30. A display according to any one of claims 15 to 29, **characterized in that**
the thin film transistor element, the video signal wiring, and the liquid crystal alignment direction control electrode are provided in the same layer.

31. A method for manufacturing a display according to claim 30, **characterized in that**
the thin film transistor element, the video signal wiring, and the liquid crystal alignment direction control electrode are prepared simultaneously, using a halftone exposure technique.

Patentansprüche

1. Flüssigkristallanzeige der vertikal ausgerichteten Art vom aktiven Farbmatrixtyp mit einem Aktivmatrixsubstrat (13), auf dem gebildet ist:

eine Abtastsignalverdrahtung (17),
eine Videosignalverdrahtung (11),
ein Dünnfilmtransistor (16), der an einer Kreuzung der Abtastsignalverdrahtung und der Videosignalverdrahtung bereitgestellt ist,
eine transparente Pixelelektrode (8), die mit dem Dünnfilmtransistorelement verbunden ist und in der zwei oder mehr lange schmale Schlitze (9) bereitgestellt sind, und
eine Flüssigkristallausrichtungsrichtungssteuerelektrode (15), die in einer Schicht angeordnet ist, die über eine Isolierschicht (12) unterhalb der transparenten Pixelelektrode bereitgestellt ist;
wobei die Flüssigkristallanzeige weiter enthält:

ein Farbfiltersubstrat (1), das dem Aktivmatrixsubstrat gegenüberliegt, und
eine anisotrope Flüssigkristallschicht mit einer negativen Dielektrizitätskonstante, die zwischen dem Aktivmatrixsubstrat und dem Farbfiltersubstrat eingebettet ist;
wobei eine transparente flache gemeinsame Elektrode (4) auf der Seite des Farbfiltersubstrats bereitgestellt ist und
wobei zum Anlegen einer Spannung an die Flüssigkristallmoleküle (14), die vertikal zwischen dem Aktivmatrixsubstrat und dem Farbfiltersubstrat ausgerichtet sind, und zum Kippenlassen der Flüssigkristallmoleküle in zwei oder vier verschiedene Richtungen zwei Arten der folgenden Elektrodenstrukturen in einem Pixel des Aktivmatrixsubstrats bereitgestellt sind:

eine erste Elektrodenstruktur, die der transparenten flachen gemeinsamen Elektrode gegenüberliegt und auf der Seite des Aktivmatrixsubstrats gebildet ist durch diejenigen der langen schmalen Schlitze in der transparenten Pixelelektrode, unter denen keine Flüssigkristallausrichtungsrichtungssteuerelektrode gebildet ist, und
eine zweite Elektrodenstruktur, die der transparenten flachen gemeinsamen Elektrode gegenüberliegt und auf der Seite des Aktivmatrixsubstrats gebildet ist durch diejenigen der langen schmalen Schlitze in der transparenten Pixelelektrode, unter denen eine Flüssigkristallausrichtungsrichtungssteuerelektrode gebildet ist, und durch die entsprechende Flüssigkristallausrichtungsrichtungssteuerelektrode (15), die eine größere Abmessung aufweist als die Abmessung der Schlitze;
dadurch gekennzeichnet, dass
für jede Zeile von Pixeln eine oder zwei Zeilen von Kristallausrichtungsrichtungssteuerelektroden bereitgestellt sind,
die verschiedenen Zeilen von Flüssigkristallausrichtungsrichtungssteuerelektroden jeweils mit Ausgangsanschlüssen verschiedener Treiber-ICs verbunden sind; und
eine getrennte Ansteuerung für jede Zeile von Flüssigkristallausrichtungsrichtungssteuerelektroden bereitgestellt ist.

2. Anzeige nach Anspruch 1, **dadurch gekennzeichnet, dass**
für die zweite Elektrodenstruktur zwei Zeilen von Kristallausrichtungsrichtungssteuerelektroden (19, 20), die voneinander getrennt und so angeordnet sind, dass sie auf voneinander verschiedene elektrische Potentiale gelegt werden, über die Isolierschicht (12) in einer Schicht unter der transparenten Pixelelektrode (8) existieren,
jede der Kristallausrichtungsrichtungssteuerelektroden eine größere Abmessung aufweist als die Abmessung der Schlitze (9), und
die zwei Zeilen von Kristallausrichtungsrichtungssteuerelektroden in der Richtung der Abtastsignalverdrahtung (17) angeordnet sind.

3. Anzeige nach Anspruch 1, **dadurch gekennzeichnet, dass**
die transparente Pixelelektrode (8) zwei oder mehr kreisförmige oder polygonale Löcher (37) und zwei oder mehr lange schmale Schlitze (9) aufweist, die in ihr bereitgestellt sind,
die zwei Arten von Elektrodenstrukturen bereitgestellt sind, um die Flüssigkristallmoleküle in viele Richtungen kippen zu lassen, und
die erste Elektrodenstruktur durch die kreisförmigen oder polygonalen Löcher in den transparenten Elektroden gebildet ist.

4. Anzeige nach Anspruch 3, **dadurch gekennzeichnet, dass**
für die zweite Elektrodenstruktur zwei Zeilen von Kristallausrichtungsrichtungssteuerelektroden (19, 20), die voneinander getrennt und so angeordnet sind, dass sie auf voneinander verschiedene elektrische Potentiale gelegt werden, über die Isolierschicht (12) in einer Schicht unter der transparenten Pixelelektrode (8) existieren,

jede der Kristallausrichtungsrichtungssteuerelektroden eine größere Abmessung aufweist als die Abmessung der Schlitze (9), und
die zwei Zeilen von Kristallausrichtungsrichtungssteuerelektroden in der Richtung der Abtastsignalverdrahtung (17) angeordnet sind.

5. Anzeige nach einem der Ansprüche 1 bis 4, **dadurch gekennzeichnet, dass**
benachbarte transparente Pixelelektroden (8) in der Richtung der Abtastsignalverdrahtung (17) mit Dünnfilmtransistorkomponenten (16) verbunden sind, die jeweils von verschiedenen Abtastsignalverdrahtungen gesteuert werden.

6. Anzeige nach einem der vorigen Ansprüche, **dadurch gekennzeichnet, dass**
ein Schlitz (9), der in der transparenten Pixelelektrode (8) auf der Seite des Aktivmatrixsubstrats (13) bereitgestellt ist und sich lang und schmal erstreckt, und ein Schlitz, der zu der zweiten Elektrodenstruktur gehört, unter Beibehaltung einer Parallelbeziehung abwechselnd in einer Richtung angeordnet sind, die etwa ±45 Grad zu der Richtung der Abtastsignalverdrahtung (17) verläuft; oder
dadurch gekennzeichnet, dass
eine Struktur verwendet wird, bei der Schlitze (9), die in der transparenten Pixelelektrode (8) auf der Seite des Aktivmatrixsubstrats (13) bereitgestellt ist und sich lang und schmal erstrecken, in einer Richtung angeordnet sind, die etwa ±45 Grad zu der Richtung der Abtastsignalverdrahtung (17) verläuft; Schlitze, die zu der zweiten Elektrodenstruktur gehören, in einer parallelen Richtung und in einer senkrechten Richtung zu der Richtung der Abtastsignalverdrahtung angeordnet sind; und
die Flüssigkristallausrichtungsrichtungssteuerelektrode einen Rand der transparenten Pixelelektrode einschließt, während sie sich über die Isolierschicht (12) mit der transparenten Pixelelektrode überlappt; oder
dadurch gekennzeichnet, dass
eine Struktur verwendet wird, bei der ein Schlitz (9), der in der transparenten Pixelelektrode (8) auf der Seite des Aktivmatrixsubstrats (13) bereitgestellt ist und sich lang und schmal erstreckt, in einer parallelen Richtung und in einer senkrechten Richtung zu der Richtung der Abtastsignalverdrahtung (17) angeordnet ist;
ein Schlitz, der zu der zweiten Elektrodenstruktur gehört, parallel zu der Richtung der Abtastsignalverdrahtung angeordnet ist; und
die Flüssigkristallausrichtungsrichtungssteuerelektrode einen Rand der transparenten Pixelelektrode einschließt, während sie sich über die Isolierschicht (12) mit der transparenten Pixelelektrode überlappt; oder
dadurch gekennzeichnet, dass
eine Struktur verwendet wird, bei der Schlitze (9), die in der transparenten Pixelelektrode (8) auf der Seite des Aktivmatrixsubstrats (13) bereitgestellt sind und sich lang und schmal erstrecken, in einer parallelen Richtung und in einer senkrechten Richtung zu der Richtung der Abtastsignalverdrahtung (17) angeordnet sind; und
Schlitze, die zu der zweiten Elektrodenstruktur gehören, in einer Richtung angeordnet sind, die etwa ±45 Grad zu der Richtung der Abtastsignalverdrahtung verläuft.

7. Anzeige nach Anspruch 3, 4 oder 5, **dadurch gekennzeichnet,**
dass
eine Struktur verwendet wird, bei der Schlitze (9), die zu der zweiten Elektrodenstruktur gehören, in einer parallelen Richtung und in einer senkrechten Richtung zu der Richtung der Abtastsignalverdrahtung angeordnet sind, so dass sie zwei oder mehr kreisförmige oder polygonale Löcher (37) einschließen, die in der transparenten Pixelelektrode (8) auf der Seite des Aktivmatrixsubstrats (13) bereitgestellt sind; und
die Flüssigkristallausrichtungsrichtungssteuerelektrode einen Rand der transparenten Pixelelektrode (8) einschließt, während sie sich über die Isolierschicht (12) mit der transparenten Pixelelektrode überlappt.

8. Anzeige nach einem der vorigen Ansprüche, **dadurch gekennzeichnet, dass**
die Flüssigkristallausrichtungsrichtungssteuerelektrode (15) in derselben Schicht bereitgestellt ist wie die Abtastsignalverdrahtung (17); und/oder
dadurch gekennzeichnet, dass
eine zusätzliche Kapazität mit der Flüssigkristallausrichtungsrichtungssteuerelektrode und der transparenten Pixelelektrode bereitgestellt ist.

9. Anzeige nach Anspruch 2 oder 4, **dadurch gekennzeichnet,**
dass
die Kontaktknöpfe (30, 33, 36, 38, 39) sowohl der Abtastsignalverdrahtung (17) als auch der Flüssigkristallausrichtungsrichtungssteuerelektroden (15) entweder auf einer ersten Seite oder auf einer zweiten Seite des Anzeigeabschnitts angeordnet sind und die Kontaktknöpfe von zwei Reihen der Flüssigkristallausrichtungsrichtungssteuerelektroden zum Steuern einer Reihe von Pixeln so angeordnet sind, dass sie zwischen den Kontaktknöpfen der Abtastsignalverdrahtung eingebettet sein können; oder
dadurch gekennzeichnet, dass
die Kontaktknöpfe (30, 33, 36, 38, 39) sowohl der Abtastsignalverdrahtung (17) als auch der Flüssigkristallausrichtungsrichtungssteuerelektro-

den (15) sowohl auf einer ersten Seite als auch auf einer zweiten Seite des Anzeigeabschnitts angeordnet sind und die Kontaktknöpfe von zwei Reihen der Flüssigkristallausrichtungsrichtungssteuerelektroden zum Steuern einer Reihe von Pixeln so angeordnet sind, dass sie zwischen den Kontaktknöpfen der Abtastsignalverdrahtung eingebettet sein können.

10. Anzeige nach Anspruch 5, **dadurch gekennzeichnet, dass**
die Kontaktknöpfe (30, 33, 36, 38, 39) sowohl der Abtastsignalverdrahtung (17) als auch der Flüssigkristallausrichtungsrichtungssteuerelektroden (15) entweder auf einer ersten Seite oder auf einer zweiten Seite des Anzeigeabschnitts angeordnet sind und die Kontaktknöpfe einer Reihe der Flüssigkristallausrichtungsrichtungssteuerelektrode zum Steuern einer Reihe von Pixeln so angeordnet sind, dass sie zwischen den Kontaktknöpfen der Abtastsignalverdrahtung eingebettet sein können; oder
dadurch gekennzeichnet, dass
die Kontaktknöpfe (30, 33, 36, 38, 39) sowohl der Abtastsignalverdrahtung (17) als auch der Flüssigkristallausrichtungsrichtungssteuerelektroden (15) sowohl auf einer ersten Seite als auch auf einer zweiten Seite des Anzeigeabschnitts angeordnet sind und die Kontaktknöpfe einer Reihe der Flüssigkristallausrichtungsrichtungssteuerelektrode zum Steuern einer Reihe von Pixeln so angeordnet sind, dass sie zwischen den Kontaktknöpfen der Abtastsignalverdrahtung eingebettet sein können.

11. Anzeige nach einem der Ansprüche 1 bis 5, **dadurch gekennzeichnet, dass**
die Kontaktknöpfe (30, 33, 36,) der Abtastsignalverdrahtung entweder auf einer ersten Seite oder auf einer zweiten Seite des Anzeigeabschnitts angeordnet sind, und die Kontaktknöpfe (38, 39) der Flüssigkristallausrichtungsrichtungssteuerelektrode (15) auf einer anderen Seite angeordnet sind, die von der Seite der Kontaktknöpfe der Abtastsignalverdrahtung verschieden ist.

12. Verfahren zum Ansteuern der Anzeige nach Anspruch 11, **dadurch gekennzeichnet, dass**
beim Anzeigen von beweglichen Bildern eine zwischen der Flüssigkristallausrichtungsrichtungssteuerelektrode (15) und der transparenten Pixelelektrode angelegte Vorspannung höher eingestellt wird als eine Spannung beim Anzeigen von Standbildern, und **dadurch** eine Kippgeschwindigkeit der anisotropen Flüssigkristallmoleküle mit negativer Dielektrizitätskonstante höher eingestellt wird.

13. Verfahren zum Ansteuern der Anzeige nach einem der Ansprüche 1 bis 5, **dadurch gekennzeichnet, dass**
das elektrische Potential der Flüssigkristallausrichtungsrichtungssteuerelektrode (15) niedriger eingestellt wird als das elektrische Potential der transparenten Pixelelektrode, wenn das elektrische Potential der transparenten Pixelelektrode (8), die auf der Seite des Aktivmatrixsubstrats (13) für jedes Pixel getrennt ist, niedriger ist als das elektrische Potential der gegenüberliegenden transparenten flachen gemeinsamen Elektrode (4) auf der Seite des Farbfiltersubstrats (1);
das elektrische Potential der Flüssigkristallausrichtungsrichtungssteuerelektrode (15) höher eingestellt wird als das elektrische Potential der transparenten Pixelelektrode, wenn das elektrische Potential der transparenten Pixelelektrode (8) höher ist als das elektrische Potential der gegenüberliegenden transparenten flachen gemeinsamen Elektrode auf der Seite des Farbfiltersubstrats; und
die Polaritäten des elektrischen Potentials der transparenten Pixelelektrode und des elektrischen Potentials der Flüssigkristallausrichtungsrichtungssteuerelektrode jede Vertikalabtastperiode zu der Polarität des elektrischen Potentials der flachen gemeinsamen Elektrode auf der Seite des Farbfiltersubstrats umgepolt werden.

14. Verfahren nach Anspruch 13 zum Ansteuern der Anzeige nach Anspruch 2 oder 4, **dadurch gekennzeichnet, dass**
die elektrischen Potentiale der Flüssigkristallausrichtungsrichtungssteuerelektroden, die in der Nähe der beiden Seiten der Abtastsignalverdrahtung angeordnet sind, als elektrische Potentiale mit einer voneinander verschiedenen Polarität eingestellt werden; und
jedes der elektrischen Potentiale der zwei Reihen von Flüssigkristallausrichtungsrichtungssteuerelektroden, die einem Pixel voneinander getrennt sind, jede Vertikalabtastperiode zu der Polarität des elektrischen Potentials der flachen gemeinsamen Elektrode auf der Seite des Farbfiltersubstrats umgepolt werden.

15. Flüssigkristallanzeige der vertikal ausgerichteten Art vom aktiven Farbmatrixtyp mit einem Aktivmatrixsubstrat (13), auf dem gebildet ist:

eine Abtastsignalverdrahtung (17),
eine Videosignalverdrahtung (11),
ein Dünnfilmtransistor (16), der an einer Kreuzung der Abtastsignalverdrahtung und der Videosignalverdrahtung bereitgestellt ist,
eine transparente Pixelelektrode (8), die mit dem Dünnfilmtransistorelement verbunden ist und in der zwei oder mehr lange schmale Schlitze (9) bereitgestellt sind, und
eine Flüssigkristallausrichtungsrichtungssteu-

erelektrode (15), die über eine Isolierschicht (12) in einer Schicht unterhalb der transparenten Pixelelektrode bereitgestellt ist;
wobei die Flüssigkristallanzeige weiter enthält:

ein Farbfiltersubstrat (1), das dem Aktivmatrixsubstrat gegenüberliegt, und
eine anisotrope Flüssigkristallschicht mit einer negativen Dielektrizitätskonstante, die zwischen dem Aktivmatrixsubstrat und dem Farbfiltersubstrat eingebettet ist;
wobei eine transparente flache gemeinsame Elektrode (4) auf der Seite des Farbfiltersubstrats bereitgestellt ist und
wobei zum Anlegen einer Spannung an die Flüssigkristallmoleküle (14), die vertikal zwischen dem Aktivmatrixsubstrat und dem Farbfiltersubstrat ausgerichtet sind, und zum Kippenlassen der Flüssigkristallmoleküle in zwei oder vier verschiedene Richtungen zwei Arten der folgenden Elektrodenstrukturen in einem Pixel des Aktivmatrixsubstrats bereitgestellt sind:

eine erste Elektrodenstruktur, die der transparenten flachen gemeinsamen Elektrode gegenüberliegt und auf der Seite des Aktivmatrixsubstrats gebildet ist durch diejenigen der langen schmalen Schlitze in der transparenten Pixelelektrode, unter denen keine Flüssigkristallausrichtungsrichtungssteuerelektrode gebildet ist, und
eine zweite Elektrodenstruktur, die der transparenten flachen gemeinsamen Elektrode gegenüberliegt und auf der Seite des Aktivmatrixsubstrats gebildet ist durch diejenigen der langen schmalen Schlitze in der transparenten Pixelelektrode, unter denen eine Flüssigkristallausrichtungsrichtungssteuerelektrode gebildet ist, und durch die entsprechende Flüssigkristallausrichtungsrichtungssteuerelektrode (15), die eine größere Abmessung aufweist als die Abmessung der Schlitze;
dadurch gekennzeichnet, dass
in einem Pixel der Zeile n und der Spalte m ein erstes Dünnfilmtransistorelement (49) an einer Stelle gebildet ist, an der die Abtastsignalverdrahtung (17) der Zeile (n-1) und die Videosignalverdrahtung (11) der Spalte (m+1) einander kreuzen, und die Videosignalverdrahtung der Spalte (m+1) und die Flüssigkristallausrichtungsrichtungssteuerelektrode (15), die für das Pixel der Zeile n und der Spalte m verwendet werden, über das erste Dünnfilmtransistorelement verbunden sind; und
ein zweites Dünnfilmtransistorelement (16) an einer Stelle gebildet ist, an der die Abtastsignalverdrahtung der Zeile n und die Videosignalverdrahtung der Spalte m einander kreuzen, und die Videosignalverdrahtung der Spalte m und die transparente Pixelelektrode, die für das Pixel der Zeile n und der Spalte m verwendet werden, über das zweite Dünnfilmtransistorelement verbunden sind.

16. Flüssigkristallanzeige der vertikal ausgerichteten Art vom aktiven Farbmatrixtyp mit einem Aktivmatrixsubstrat (13), auf dem gebildet ist:

eine Abtastsignalverdrahtung (17),
eine Videosignalverdrahtung (11),
ein Dünnfilmtransistor (16), der an einer Kreuzung der Abtastsignalverdrahtung und der Videosignalverdrahtung bereitgestellt ist,
eine transparente Pixelelektrode (8), die mit dem Dünnfilmtransistorelement verbunden ist und in der zwei oder mehr lange schmale Schlitze (9) bereitgestellt sind, und
eine Flüssigkristallausrichtungsrichtungssteuerelektrode (15), die über eine Isolierschicht (12) in einer Schicht unterhalb der transparenten Pixelelektrode bereitgestellt ist;
wobei die Flüssigkristallanzeige weiter enthält:

ein Farbfiltersubstrat (1), das dem Aktivmatrixsubstrat gegenüberliegt, und
eine anisotrope Flüssigkristallschicht mit einer negativen Dielektrizitätskonstante, die zwischen dem Aktivmatrixsubstrat und dem Farbfiltersubstrat eingebettet ist;
wobei eine transparente flache gemeinsame Elektrode (4) auf der Seite des Farbfiltersubstrats bereitgestellt ist und
wobei zum Anlegen einer Spannung an die Flüssigkristallmoleküle (14), die vertikal zwischen dem Aktivmatrixsubstrat und dem Farbfiltersubstrat ausgerichtet sind, und zum Kippenlassen der Flüssigkristallmoleküle in zwei oder vier verschiedene Richtungen zwei Arten der folgenden Elektrodenstrukturen in einem Pixel des Aktivmatrixsubstrats bereitgestellt sind:

eine erste Elektrodenstruktur, die der transparenten flachen gemeinsamen Elektrode gegenüberliegt und auf der Seite des Aktivmatrixsubstrats gebildet ist durch diejenigen der langen schmalen Schlitze in der transparenten Pixel-

elektrode, unter denen keine Flüssigkristallausrichtungsrichtungssteuerelektrode gebildet ist, und
eine zweite Elektrodenstruktur, die der transparenten flachen gemeinsamen Elektrode gegenüberliegt und auf der Seite des Aktivmatrixsubstrats gebildet ist durch diejenigen der langen schmalen Schlitze in der transparenten Pixelelektrode, unter denen eine Flüssigkristallausrichtungsrichtungssteuerelektrode gebildet ist, und durch die entsprechende Flüssigkristallausrichtungsrichtungssteuerelektrode (15), die eine größere Abmessung aufweist als die Abmessung der Schlitze;
dadurch gekennzeichnet, dass
eine gemeinsame Elektrodenverdrahtung (48) auf der Seite des Aktivmatrixsubstrats bereitgestellt ist und sich in einer Richtung parallel zu der Abtastsignalverdrahtung (17) erstreckt,
in einem Pixel der Zeile n und der Spalte m ein erstes Dünnfilmtransistorelement (50) an der Abtastsignalverdrahtung (17) der Zeile (n-1) gebildet ist und die gemeinsame Elektrodenverdrahtung (48) der Zeile n und die Flüssigkristallausrichtungsrichtungssteuerelektrode (15), die für das Pixel der Zeile n und der Spalte m verwendet werden, über das erste Dünnfilmtransistorelement verbunden sind, und
ein zweites Dünnfilmtransistorelement (16) an einer Stelle gebildet ist, an der die Abtastsignalverdrahtung der Zeile n und die Videosignalverdrahtung (11) der Spalte m einander kreuzen, und die Videosignalverdrahtung der Spalte m und die transparente Pixelelektrode (8), die für das Pixel der Zeile n und der Spalte m verwendet werden, über das zweite Dünnfilmtransistorelement verbunden sind.

17. Anzeige nach Anspruch 15, **dadurch gekennzeichnet, dass**
die transparente Pixelelektrode (8) zwei oder mehr kreisförmige oder polygonale Löcher (37) und zwei oder mehr lange schmale Schlitze (9) aufweist, die in ihr bereitgestellt sind,
die zwei Arten von Elektrodenstrukturen bereitgestellt sind, um die Flüssigkristallmoleküle in viele Richtungen kippen zu lassen, und
die erste Elektrodenstruktur durch die kreisförmigen oder polygonalen Löcher in den transparenten Elektroden gebildet ist.

18. Anzeige nach Anspruch 16, **dadurch gekennzeichnet, dass**
die transparente Pixelelektrode (8) zwei oder mehr kreisförmige oder polygonale Löcher (37) und zwei oder mehr lange schmale Schlitze (9) aufweist, die in ihr bereitgestellt sind,
die zwei Arten von Elektrodenstrukturen bereitgestellt sind, um die Flüssigkristallmoleküle in viele Richtungen kippen zu lassen, und
die erste Elektrodenstruktur durch die kreisförmigen oder polygonalen Löcher in den transparenten Elektroden gebildet ist.

19. Verfahren zum Treiben einer Anzeige nach einem der Ansprüche 15 bis 18, **dadurch gekennzeichnet, dass**
die Zeitbreite des Abtastsignalverlaufs in der Abtastsignalverdrahtung (17) nicht kleiner ist als das Zweifache einer Horizontalperiode,
der Abtastsignalverlauf in der Abtastsignalverdrahtung der (n-1)-ten Zeile und der Abtastsignalverlauf in der Abtastsignalverdrahtung der (n)-ten Zeile einander um nicht weniger als die Zeit einer Horizontalperiode überlappen, und
die Polaritäten der Videosignalspannung der Videosignalverdrahtung (11) der Spalte m und der Videosignalspannung der Videosignalverdrahtung der Spalte (m+1) voneinander verschieden sind und die Polaritäten jede Horizontalperiode miteinander vertauscht werden und die Polaritäten jede Vertikalabtastperiode gegenseitig umgepolt werden.

20. Anzeige nach Anspruch 15 oder 17, **dadurch gekennzeichnet,**
dass
die Kanallänge (L_2) des ersten Dünnfilmtransistorelements (49), das an einer Stelle gebildet ist, an der die Abtastsignalverdrahtung (17) der Zeile (n-1) und die Videosignalverdrahtung (11) der Spalte (m+1) einander kreuzen und das mit der Flüssigkristallausrichtungsrichtungssteuerelektrode (15) verbunden ist, größer ist als die Kanallänge (L_1) des zweiten Dünnfilmtransistorelements (16), das an einer Stelle gebildet ist, an der die Abtastsignalverdrahtung der Zeile n und die Videosignalverdrahtung der Spalte m einander kreuzen und das mit der transparenten Pixelelektrode verbunden ist ($L_1 < L_2$).

21. Anzeige nach Anspruch 16 oder 18, **dadurch gekennzeichnet,**
dass
die Kanallänge (L_2) des ersten Dünnfilmtransistorelements (49), das an der Abtastsignalverdrahtung der Zeile (n-1) gebildet ist und das mit der Flüssigkristallausrichtungsrichtungssteuerelektrode (15) verbunden ist, größer ist als die Kanallänge (L_1) des zweiten Dünnfilmtransistorelements (16), das an einer Stelle gebildet ist, an der die Abtastsi-

gnalverdrahtung der Zeile n und die Videosignalverdrahtung der Spalte m einander kreuzen, und das mit der transparenten Pixelelektrode verbunden ist ($L_1 < L_2$).

22. Anzeige nach einem der Ansprüche 15 bis 21, **dadurch gekennzeichnet, dass**
eine Doppeltransistorelementstruktur oder eine Versatzkanalelementstruktur für das Dünnfilmtransistorelement (16) verwendet wird, das mit der Flüssigkristallausrichtungsrichtungssteuerelektrode (15) verbunden ist.

23. Anzeige nach Anspruch 15 oder 16, **dadurch gekennzeichnet,**
dass
ein Schlitz (9), der in der transparenten Pixelelektrode (8) auf der Seite des Aktivmatrixsubstrats (13) gebildet ist und sich lang und schmal erstreckt, und ein Schlitz, der zu der zweiten Elektrodenstruktur gehört, unter Beibehaltung einer Parallelbeziehung zueinander abwechselnd in einer Winkelrichtung von etwa ±45 Grad zu der Richtung der Abtastsignalverdrahtung (17) angeordnet sind; oder
dadurch gekennzeichnet, dass
ein Schlitz (9), der in der transparenten Pixelelektrode (8) auf der Seite des Aktivmatrixsubstrats (13) gebildet ist und sich lang und schmal erstreckt, im Wesentlichen in einer parallelen Richtung und in einer senkrechten Richtung zu der Richtung der Abtastsignalverdrahtung (17) angeordnet sind, und ein Schlitz, der zu der zweiten Elektrodenstruktur gehört, in einer Winkelrichtung von etwa ±45 Grad zu der Richtung der Abtastsignalverdrahtungen angeordnet ist; oder
dadurch gekennzeichnet, dass
ein Schlitz (9), der in der transparenten Pixelelektrode (8) auf der Seite des Aktivmatrixsubstrats (13) gebildet ist und sich lang und schmal erstreckt, in einer Winkelrichtung von etwa ±45 Grad zu der Ausdehnungsrichtung der Abtastsignalverdrahtungen angeordnet ist und ein Schlitz, der zu der zweiten Elektrodenstruktur gehört, in einer parallelen Richtung und in einer senkrechten Richtung zu der Ausdehnungsrichtung der Abtastsignalverdrahtung angeordnet ist und die Flüssigkristallausrichtungsrichtungssteuerelektrode einen Rand der transparenten Pixelelektrode einschließt, während sie sich über die Isolierschicht (12) mit der transparenten Pixelelektrode überlappt.

24. Anzeige nach Anspruch 17 oder 18, **dadurch gekennzeichnet,**
dass
ein Schlitz (9), der zu der zweiten Elektrodenstruktur gehört, in einer parallelen Richtung und in einer senkrechten Richtung zu der Ausdehnungsrichtung der Abtastsignalverdrahtung (17) angeordnet ist, so dass zwei oder mehr kreisförmige oder polygonale Löcher (37), die in der transparenten Pixelelektrode (8) auf der Seite des Aktivmatrixsubstrats bereitgestellt sind, umrundet sind, und die Flüssigkristallausrichtungsrichtungssteuerelektrode einen Rand der transparenten Pixelelektrode einschließt, während sie sich über die Isolierschicht (12) mit der transparenten Pixelelektrode überlappt.

25. Anzeige nach einem der Ansprüche 15 bis 24, **dadurch gekennzeichnet, dass**
die Flüssigkristallausrichtungsrichtungssteuerelektrode (15) in derselben Schicht gebildet ist wie die Abtastsignalverdrahtung (17); oder
dadurch gekennzeichnet, dass
die Flüssigkristallausrichtungsrichtungssteuerelektrode (15) in derselben Schicht gebildet ist wie die Videosignalverdrahtung (11).

26. Anzeige nach einem der Ansprüche 15 bis 18, **dadurch gekennzeichnet, dass**
zwei Dünnfilmtransistorelemente (16) in einem Pixel erforderlich sind, um das eine Pixel anzusteuern, und nur ein Kontaktloch (18) existiert zum elektrischen Verbinden der Drainelektrode des Dünnfilmtransistorelements, das an einer Stelle gebildet ist, an der die Abtastsignalverdrahtung (17) der Zeile n und die Videosignalverdrahtung (11) der Spalte m einander kreuzen, und der transparenten Pixelelektrode (8); oder
dadurch gekennzeichnet, dass
zwei Dünnfilmtransistorelemente (16) in einem Pixel erforderlich sind, um das eine Pixel anzusteuern, und zwei Kontaktlöcher (61, 62) existieren zum elektrischen Verbinden der Drainelektrode des Dünnfilmtransistorelements, das an einer Stelle gebildet ist, an der die Abtastsignalverdrahtung (17) der Zeile (n-1) und die Videosignalverdrahtung (11) der Spalte (m+1) einander kreuzen, und der Flüssigkristallausrichtungsrichtungssteuerelektrode (15); und nur ein Kontaktloch (18) existiert zum elektrischen Verbinden der Drainelektrode des Dünnfilmtransistorelements, das an einer Stelle gebildet ist, an der die Abtastsignalverdrahtung (17) der Zeile n und die Videosignalverdrahtung (11) der Spalte m einander kreuzen, und der transparenten Pixelelektrode (8); oder
dadurch gekennzeichnet, dass
zwei Dünnfilmtransistorelemente (16) in einem Pixel erforderlich sind, um das eine Pixel anzusteuern, ein Dünnfilmtransistorelement mit der transparenten Pixelelektrode (8) verbunden ist, das andere verbleibende Dünnfilmtransistorelement mit der Flüssigkristallausrichtungsrichtungssteuerelektrode (15) verbunden ist, und die transparente Pixelelektrode und die Flüssigkristallausrichtungsrichtungssteuerelektrode sich über die Isolierschicht (12) überlappen zum Bilden einer Kapazität.

27. Anzeige nach einem der Ansprüche 15 bis 26, **dadurch gekennzeichnet, dass**
eine Zwischenelektrode (67) des ersten Dünnfilmtransistorelements, das mit der Flüssigkristallausrichtungsrichtungssteuerelektrode (15) verbunden ist, und die transparente Pixelelektrode (8) sich über die Isolierschicht (12) überlappen zum Bilden einer Kapazität, und das erste Dünnfilmtransistorelement eine Doppeltransistorstruktur aufweist.

28. Anzeige nach Anspruch 15 oder 17, **dadurch gekennzeichnet,**
dass
die transparente Pixelelektrode (8) der Zeile n und der spalte m und die Abtastsignalverdrahtung (17) der(n-1)-ten Zeile sich über die Isolierschicht (12) überlappen zum Bilden einer Speicherkapazität.

29. Anzeige nach Anspruch 16 oder 18, **dadurch gekennzeichnet,**
dass
die transparente Pixelelektrode (8) der Zeile n und der spalte m und die gemeinsame Elektrode (48) der Zeile n sich über die Isolierschicht (12) überlappen zum Bilden einer Speicherkapazität.

30. Anzeige nach einem der Ansprüche 15 bis 29, **dadurch gekennzeichnet, dass**
das Dünnfilmtransistorelement, die Videosignalverdrahtung und die Flüssigkristallausrichtungsrichtungssteuerelektrode in derselben Schicht bereitgestellt sind.

31. Verfahren zum Herstellen einer Anzeige nach Anspruch 30,
dadurch gekennzeichnet, dass
das Dünnfilmtransistorelement, die Videosignalverdrahtung und die Flüssigkristallausrichtungsrichtungssteuerelektrode gleichzeitig unter Verwendung einer Halbtonbelichtungstechnik hergestellt sind.

Revendications

1. Ecran à cristaux liquides couleur avec un mode aligné verticalement du type à matrice active comprenant un substrat de matrice active (13) ayant formé sur celui-là :

un câblage de signal de balayage (17);
un câblage de signal vidéo (11) ;
un transistor à couche peu épaisse (16) qui est prévu à une intersection du câblage de signal de balayage et du câblage de signal vidéo ;
une électrode de pixel transparente (8) qui est raccordée à l'élément de transistor à couche peu épaisse et dans laquelle deux ou davantage de longues et fines fentes (9) sont prévues ; et
une électrode de commande de la direction d'alignement des cristaux liquides (15) disposée sur une couche en dessous de l'électrode de pixel transparente prévue via un film isolant (12) ;
l'écran à cristaux liquides comprenant en outre :

un substrat de filtre de couleur (1) faisant face au substrat de matrice active, et
une couche de cristaux liquides anisotrope ayant une constante diélectrique négative prise en sandwich par le substrat de matrice active et le substrat de filtre de couleur,
dans lequel une électrode commune plate, transparente (4) est prévue du côté du substrat de filtre de couleur ; et dans lequel,
afin d'appliquer une tension aux molécules de cristaux liquides (14) alignées verticalement entre le substrat de matrice active et le substrat de filtre de couleur et de faire que les molécules de cristaux liquides penchent dans deux ou quatre directions différentes, deux types de structures d'électrode qui suivent sont prévus dans un pixel du substrat de matrice active :

une première structure d'électrode faisant face à l'électrode commune, plate, transparente et formée du côté du substrat de matrice active par celles des longues et fines fentes dans l'électrode de pixel transparente dans l'électrode de pixel transparente sous laquelle aucune électrode de commande de la direction d'alignement des cristaux liquides n'est formée ;
une seconde structure d'électrode faisant face à l'électrode commune, plate, transparente et formée du côté du substrat de matrice active par celles des longues et fines fentes dans l'électrode de pixel transparente dans l'électrode de pixel transparente sous laquelle une électrode de commande de la direction d'alignement des cristaux liquides est formée et par l'électrode de commande de la direction d'alignement des cristaux liquides correspondante (15) qui a une dimension plus importante que la dimension des fentes ;
caractérisé en ce que
pour chaque rangée de pixels, une ou davantage de rangées d'électrodes de commande de la direction d'alignement des cristaux sont prévues,
les différentes rangées des électrodes de commande de la direction d'alignement des cristaux liquides sont raccor-

dées aux bornes de sortie des différents CI's (circuits imprimés) de commande, respectivement ; et
une commande distincte pour chaque rangée d'électrodes de commande de la direction d'alignement des cristaux liquides est prévue.

2. Ecran selon la revendication 1, **caractérisé en ce que**
pour la seconde structure d'électrode, deux rangées d'électrodes de commande de la direction d'alignement des cristaux liquides (19, 20) qui sont mutuellement séparées et qui sont arrangées pour être mises à des potentiels électriques différents les uns des autres, existent sur une couche en dessous de l'électrode de pixel transparente (8) via le film isolant (12),
l'une ou l'autre des électrodes de commande de la direction d'alignement des cristaux liquides a une dimension plus importante que la dimension des fentes (9), et
les deux rangées d'électrodes de commande de la direction d'alignement des cristaux liquides sont disposées dans la direction du câblage de signal de balayage (17).

3. Ecran selon la revendication 1, **caractérisé en ce que**
l'électrode de pixel transparente (8) a deux ou davantage de trous circulaires ou polygonaux (37) et deux ou davantage de fentes longues et fines (9) prévues en elle,
les deux types de structures d'électrode sont prévus afin de faire que les molécules de cristaux liquides se penchent dans de nombreuses directions, et
la première structure d'électrode est formée par les trous circulaires ou polygonaux dans les électrodes transparentes.

4. Ecran selon la revendication 3, **caractérisé en ce que**
pour la seconde structure d'électrode, deux rangées d'électrodes de commande de la direction d'alignement des cristaux liquides (19, 20) qui sont mutuellement séparées et qui sont arrangées pour être mises à des potentiels électriques différents les uns des autres, existent sur une couche en dessous de l'électrode de pixel transparente (8) via le film isolant (12),
l'une ou l'autre des électrodes de commande de la direction d'alignement des cristaux liquides a une dimension plus importante que la dimension de la fente (9) ; et
les deux rangées d'électrodes de commande de la direction d'alignement des cristaux liquides sont disposées dans la direction du câblage de signal de balayage (17).

5. Ecran selon l'une quelconque des revendications 1 à 4,
caractérisé en ce que
des électrodes de pixel transparentes adjacentes (8) dans la direction du câblage de signal de balayage (17) sont raccordées aux éléments du transistor à couche peu épaisse (16) commandés par les différents câblages de signal de balayage, respectivement.

6. Ecran selon l'une quelconque des revendications précédentes, **caractérisé en ce que**
une fente (9) prévue dans l'électrode de pixel transparente (8) du côté du substrat de matrice active (13) et s'étendant longue et fine, et une fente appartenant à la seconde structure d'électrode sont disposées alternativement, maintenant une relation parallèle dans une direction qui fait environ 45 degrés par rapport à la direction du câblage de signal de balayage (17) ; ou
caractérisé en ce que
il est adopté une structure où des fentes (9) prévues dans l'électrode de pixel transparente (8) du côté du substrat de matrice active (13) et s'étendant longues et fines sont disposées dans une direction faisant $\pm$45 degrés par rapport à la direction du câblage de signal de balayage (17) ;
des fentes appartenant à la seconde structure d'électrode sont disposées dans une direction parallèle et dans une direction perpendiculaire par rapport à la direction du câblage de signal de balayage ; et
l'électrode de commande de la direction d'alignement des cristaux liquides entoure une périphérie de l'électrode de pixel transparente tout en recouvrant partiellement l'électrode de pixel transparente via le film isolant (12) ; ou
caractérisé en ce que
il est adopté une structure où une fente (9) prévue dans une électrode de pixel transparente (8) du côté du substrat de matrice active (13) et s'étendant longue et fine, est disposée dans une direction parallèle et dans une direction perpendiculaire par rapport à la direction du câblage de signal de balayage (17) ;
une fente appartenant à la seconde structure d'électrode est arrangée parallèle à la direction du câblage de signal de balayage ; et
l'électrode de commande de la direction d'alignement des cristaux liquides entoure une périphérie de l'électrode de pixel transparente tout en recouvrant partiellement l'électrode de pixel transparente via le film isolant (12) ; ou
caractérisé en ce que
il est adopté une structure où des fentes (9) prévues dans l'électrode de pixel transparente (8) du côté du substrat de matrice active (13) et s'étendant longues et fines sont arrangées dans une direction parallèle et dans une direction perpendiculaire par rapport à

la direction du câblage de signal de balayage (17) ; et des fentes appartenant à la seconde structure d'électrode sont arrangées dans une direction qui fait ±45 degrés par rapport à la direction d'un câblage de signal de balayage.

7. Ecran selon la revendication 3, 4 ou 5, **caractérisé en ce que**
il est adopté une structure où des fentes (9) appartenant à la seconde structure d'électrode sont disposées dans une direction parallèle et dans une direction perpendiculaire par rapport à la direction du câblage de signal de balayage de sorte à entourer deux ou davantage de trous circulaires ou polygonaux (37) prévus dans l'électrode de pixel transparente du côté du substrat de matrice active (13) ; et l'électrode de commande de la direction d'alignement des cristaux liquides entoure une périphérie de l'électrode de pixel transparente (8) tout en recouvrant partiellement l'électrode de pixel transparente via le film isolant (12).

8. Ecran selon l'une quelconque des revendications précédentes, **caractérisé en ce que**
l'électrode de commande de la direction d'alignement des cristaux liquides (15) est prévue sur la même couche que le câblage de signal de balayage (17) ; et/ou
caractérisé en ce que
une capacité supplémentaire est prévue avec l'électrode de commande de la direction d'alignement des cristaux liquides et avec l'électrode de pixel transparente.

9. Ecran selon la revendication 2 ou 4, **caractérisé en ce que**
l'un et l'autre des boutons de contact (30, 33, 36, 38, 39) du câblage de signal de balayage (17) et des électrodes de commande de la direction d'alignement des cristaux liquides (15) sont disposés sur l'un ou l'autre d'un premier côté ou d'un second côté de la partie d'écran d'affichage, et les boutons de contact des deux rangées de l'électrode de commande de la direction d'alignement des cristaux liquides pour commander une rangée de pixels sont disposés de telle sorte qu'ils peuvent être pris en sandwich entre les boutons de contact du câblage de signal de balayage ; ou
caractérisé en ce que
les boutons de contact (30, 33, 36, 38, 39) pour l'un et l'autre du câblage de signal de balayage (17) et des électrodes de commande de la direction d'alignement des cristaux liquides (15) sont disposés sur l'un et l'autre des second et premier côtés de la partie d'écran d'affichage, et les boutons de contact des deux rangées de l'électrode de commande de la direction d'alignement des cristaux liquides pour commander une rangée de pixels sont disposés de telle sorte qu'ils peuvent être pris en sandwich entre les boutons de contact du câblage de signal de balayage.

10. Ecran selon la revendication 5, **caractérisé en ce que**
l'un et l'autre des boutons de contact (30, 33, 36, 38, 39) du câblage de signal de balayage (17) et des électrodes de commande de la direction d'alignement des cristaux liquides (15) sont disposés sur l'un ou l'autre d'un premier côté ou d'un second côté de la partie d'écran d'affichage, et les boutons de contact d'une rangée de l'électrode de commande de la direction d'alignement des cristaux liquides pour commander une rangée de pixels sont disposés de telle sorte qu'ils peuvent être pris en sandwich entre les boutons de contact du câblage de signal de balayage ; ou
caractérisé en ce que
les boutons de contact (30, 33, 36, 38, 39) pour l'un et l'autre du câblage de signal de balayage (17) et des électrodes de commande de la direction d'alignement des cristaux liquides (15) sont disposés sur l'un et l'autre des second et premier côtés de la partie d'écran d'affichage, et les boutons de contact d'une rangée de l'électrode de commande de la direction d'alignement des cristaux liquides pour commander une rangée de pixels sont disposés de telle sorte qu'ils peuvent être pris en sandwich entre les boutons de contact du câblage de signal de balayage.

11. Ecran selon l'une quelconque des revendications 1 à 5,
caractérisé en ce que
les boutons de contact (30, 33, 36) du câblage de signal de balayage sont disposés sur l'un ou l'autre d'un premier côté ou d'un second côté de la partie d'écran d'affichage, et les boutons de contact (38, 39) de l'électrode de commande de la direction d'alignement des cristaux liquides (15) sont disposés sur un autre côté différent du côté des boutons de contact du câblage de signal de balayage.

12. Procédé de commande de l'écran selon la revendication 11, **caractérisé en ce que**
au moment de l'affichage d'une image animée, une tension de polarisation appliquée entre l'électrode de commande de la direction d'alignement des cristaux liquides (15) et l'électrode de pixel transparente est mise plus haute qu'une tension au moment de l'affichage d'une image immobile et, de ce fait, une vitesse d'inclinaison des molécules de cristaux liquides anisotropes ayant une constante diélectrique négative est mise plus élevée.

13. Procédé de commande de l'écran selon l'une quelconque des revendications 1 à 5, **caractérisé en ce que**

lorsque le potentiel électrique de l'électrode de pixel transparente (8) séparée pour chaque pixel du côté du substrat de matrice active (13) est plus bas que le potentiel électrique de l'électrode commune plate qui fait face (4) du côté du substrat de filtre de couleur (1), le potentiel électrique de l'électrode de commande de la direction d'alignement des cristaux liquides (15) est mis plus bas que le potentiel électrique de l'électrode de pixel transparente ;
lorsque le potentiel électrique de l'électrode de pixel transparente est plus élevé que le potentiel électrique de l'électrode commune plate qui fait face du côté du substrat de filtre de couleur, le potentiel électrique de l'électrode de commande de la direction d'alignement des cristaux liquides (15) est mis plus haut que le potentiel électrique de l'électrode de pixel transparente ; et
les polarités du potentiel électrique de l'électrode de pixel transparente et du potentiel de l'électrode de commande de la direction d'alignement des cristaux liquides sont inversés par rapport à la polarité du potentiel électrique de l'électrode commune plate du côté du substrat de filtre de couleur à chaque période de balayage verticale.

14. Procédé selon la revendication 13 pour commander l'écran selon la revendication 2 ou 4, **caractérisé en ce que**
les potentiels électriques des électrodes de commande de la direction d'alignement des cristaux liquides disposées à proximité des deux côtés du câblage de signal de balayage sont mis à des potentiels électriques avec une polarité différente l'une de l'autre ; et
chacun des potentiels électriques des deux rangées d'électrodes de commande de la direction d'alignement des cristaux liquides mutuellement séparées dans un pixel sont inversés par rapport à la polarité du potentiel électrique de l'électrode commune plate du côté du substrat de filtre de couleur à chaque période de balayage verticale.

15. Ecran à cristaux liquides couleur avec un mode aligné verticalement du type à matrice active comprenant un substrat de matrice active (13) ayant formé sur celui-là :

un câblage de signal de balayage (17) ;
un câblage de signal vidéo (11) ;
un transistor à couche peu épaisse (16) qui est prévu à une intersection du câblage de signal de balayage et du câblage de signal vidéo ;
une électrode de pixel transparente (8) qui est raccordée à l'élément de transistor à couche peu épaisse et dans laquelle deux ou davantage de longues et fines fentes (9) sont prévues ; et
une électrode de commande de la direction d'alignement des cristaux liquides (15) disposée sur une couche en dessous de l'électrode de pixel transparente prévue via un film isolant (12) ;
l'écran à cristaux liquides comprenant en outre :

un substrat de filtre de couleur (1) faisant face au substrat de matrice active, et
une couche de cristaux liquides anisotrope ayant une constante diélectrique négative prise en sandwich par le substrat de matrice active et le substrat de filtre de couleur,
dans lequel une électrode commune plate, transparente (4) est prévue du côté du substrat de filtre de couleur ; et dans lequel,
afin d'appliquer une tension aux molécules de cristaux liquides (14) alignées verticalement entre le substrat de matrice active et le substrat de filtre de couleur et de faire que les molécules de cristaux liquides penchent dans deux ou quatre directions différentes, deux types de structures d'électrode qui suivent sont prévus dans un pixel du substrat de matrice active :

une première structure d'électrode faisant face à l'électrode commune, plate, transparente et formée du côté du substrat de matrice active par celles des longues et fines fentes dans l'électrode de pixel transparente dans l'électrode de pixel transparente sous laquelle aucune électrode de commande de la direction d'alignement des cristaux liquides n'est formée ;
une seconde structure d'électrode faisant face à l'électrode commune, plate, transparente et formée du côté du substrat de matrice active par celles des longues et fines fentes dans l'électrode de pixel transparente dans l'électrode de pixel transparente sous laquelle une électrode de commande de la direction d'alignement des cristaux liquides est formée et par l'électrode de commande de la direction d'alignement des cristaux liquides correspondante (15) qui a une dimension plus importante que la dimension des fentes ;
caractérisé en ce que
dans un pixel de la rangée n et de la colonne m, un premier élément de transistor à couche peu épaisse (49) est formé dans une position où le câblage de signal de balayage (17) de la rangée (n - 1) et le câblage de signal vidéo (11) de la colonne (m + 1) se croisent, et le câblage de vidéo de la colonne (m + 1) et l'électrode de commande de la direction d'alignement des cristaux liquides

(15) utilisée pour le pixel de la rangée n et de la colonne m sont raccordés via le premier élément de transistor à couche peu épaisse ; et
un second élément de transistor à couche peu épaisse (16) est formé dans une position où le câblage de signal de balayage de la rangée n et le câblage de signal vidéo de la colonne m se croisent, et le câblage de signal vidéo de la colonne m et l'électrode de pixel transparente utilisée pour le pixel de la rangée n et de la colonne m sont raccordés via le second élément de transistor à couche peu épaisse.

16. Ecran à cristaux liquides couleur avec un mode aligné verticalement du type à matrice active comprenant un substrat de matrice active (13) ayant formé sur celui-là :

un câblage de signal de balayage (17) ;
un câblage de signal vidéo (11) ;
un transistor à couche peu épaisse (16) qui est prévu à une intersection du câblage de signal de balayage et du câblage de signal vidéo ;
une électrode de pixel transparente (8) qui est raccordée à l'élément de transistor à couche peu épaisse et dans lequel deux ou davantage de longues et fines fentes (9) sont prévues ; et
une électrode de commande de la direction d'alignement des cristaux liquides (15) disposée sur une couche en dessous de l'électrode de pixel transparente prévue via un film isolant (12) ;
l'écran à cristaux liquides comprenant en outre :

un substrat de filtre de couleur (1) faisant face au substrat de matrice active, et
une couche de cristaux liquides anisotrope ayant une constante diélectrique négative prise en sandwich par le substrat de matrice active et le substrat de filtre de couleur,
dans lequel une électrode commune plate, transparente (4) est prévue du côté du substrat de filtre de couleur ; et dans lequel,
afin d'appliquer une tension aux molécules de cristaux liquides (14) alignées verticalement entre le substrat de matrice active et le substrat de filtre de couleur et de faire que les molécules de cristaux liquides penchent dans deux ou quatre directions différentes, deux types de structures d'électrode qui suivent sont prévus dans un pixel du substrat de matrice active :

une première structure d'électrode faisant face à l'électrode commune, plate, transparente et formée du côté du substrat de matrice active par celles des longues et fines fentes dans l'électrode de pixel transparente dans l'électrode de pixel transparente sous laquelle aucune électrode de commande de la direction d'alignement des cristaux liquides n'est formée ;
une seconde structure d'électrode faisant face à l'électrode commune, plate, transparente et formée du côté du substrat de matrice active par celles des longues et fines fentes dans l'électrode de pixel transparente dans l'électrode de pixel transparente sous laquelle une électrode de commande de la direction d'alignement des cristaux liquides est formée et par l'électrode de commande de la direction d'alignement des cristaux liquides correspondante (15) qui a une dimension plus importante que la dimension des fentes ;
caractérisé en ce que
un câblage d'électrode commune (48) est prévu du côté du substrat de matrice active s'étendant dans une direction parallèle au câblage de signal de balayage (17),
dans le pixel de la rangée n et de la colonne m, un premier élément de transistor à couche peu épaisse (50) est formé sur le câblage de signal de balayage (17) de la rangée (n - 1), et le câblage de l'électrode commune (48) de la rangée n et l'électrode de commande de la direction d'alignement des cristaux liquides (15) utilisée pour le pixel de la rangée n et de la colonne m sont raccordés via le premier élément de transistor à couche peu épaisse, et
un second élément de transistor à couche peu épaisse (16) est formé dans une position où le câblage de signal de balayage de la rangée n et le câblage de signal vidéo (11) de la colonne m se croisent, et le câblage de signal vidéo de la colonne m et l'électrode de pixel transparente (8) utilisée pour le pixel de la rangée n et de la colonne m sont raccordés via le second élément de transistor à couche peu épaisse.

17. Ecran selon la revendication 15, **caractérisé en ce que**
l'électrode de pixel transparente (8) a deux ou davantage de trous circulaires ou polygonaux (37) et deux ou davantage de fentes longues et fines (9) prévues en elle,
les deux types de structures d'électrode sont prévus

afin de faire que les molécules de cristaux liquides se penchent dans de nombreuses directions, et
la première structure d'électrode est formée par les trous circulaires ou polygonaux dans les électrodes transparentes.

18. Ecran selon la revendication 16, **caractérisé en ce que**
l'électrode de pixel transparente (8) a deux ou davantage de trous circulaires ou polygonaux (37) et deux ou davantage de fentes longues et fines (9) prévues en elle,
les deux types de structures d'électrode sont prévus afin de faire que les molécules de cristaux liquides se penchent dans de nombreuses directions, et
la première structure d'électrode est formée par les trous circulaires ou polygonaux dans les électrodes transparentes.

19. Procédé de commande de l'écran selon l'une quelconque des revendications 15 à 18, **caractérisé en ce que**
la largeur en temps de la forme d'onde du signal de balayage dans le câblage de signal de balayage (17) ne fait pas moins du double de la période horizontale,
la forme d'onde du signal de balayage dans le câblage de signal de balayage de la $(n - 1)^{ème}$ rangée et la forme d'onde du signal de balayage dans le câblage de signal de balayage de la $n^{ème}$ rangée se recoupent l'une l'autre par au moins un moment de la période horizontale, et
les polarités de la tension du signal vidéo du câblage de signal vidéo (11) de la colonne m et de la tension du signal vidéo du câblage de signal vidéo de la colonne (m + 1) sont différentes l'une de l'autre et les polarités étant mutuellement échangées à chaque période horizontale, et les polarités étant mutuellement inversées à chaque période verticale.

20. Ecran selon la revendication 15 ou 17, **caractérisé en ce que**
la longueur de canal (L_2) du premier élément de transistor à couche peu épaisse (49) qui est formé dans une position où le câblage de signal de balayage (17) de la rangée (n - 1) et le câblage de signal vidéo (11) de la colonne (m + 1) se croisent, et qui est raccordé à l'électrode de commande de la direction d'alignement des cristaux liquides (15), est plus importante qu'une longueur de canal (L_1) du second élément de transistor à couche peu épaisse (16) qui est formé dans une position où le câblage de signal de balayage de la rangée n et le câblage de signal vidéo de la colonne m se croisent, et qui est raccordé à l'électrode de pixel transparente ($L_1 < L_2$).

21. Ecran selon la revendication 16 ou 18, **caractérisé en ce que**
la longueur de canal (L_2) du premier élément de transistor à couche peu épaisse (50) qui est formé sur le câblage de signal de balayage de la rangée (n - 1) et qui est raccordé à l'électrode de commande de la direction d'alignement des cristaux liquides (15), est plus importante que la longueur de canal (L_1) du second élément de transistor à couche peu épaisse (16) qui est formé dans une position où le câblage de signal de balayage de la rangée n et le câblage de signal vidéo de la colonne m se croisent, et qui est raccordé à l'électrode de pixel transparente ($L_1 < L_2$).

22. Ecran selon l'une quelconque des revendications 15 à
21, **caractérisé en ce que**
une structure à deux éléments de transistor ou une structure à élément de canal décalé est utilisée pour l'élément de transistor à couche peu épaisse (16) raccordé à l'électrode de commande de la direction d'alignement des cristaux liquides (15).

23. Ecran selon la revendication 15 ou 16, **caractérisé en ce que**
une fente (9) formée dans l'électrode de pixel transparente (8) du côté du substrat de matrice active (13) et s'étendant longue et fine, et une fente appartenant à la seconde structure d'électrode sont disposées alternativement, maintenant une relation parallèle l'une par rapport à l'autre dans une direction selon un angle d'environ $\pm$45 degrés par rapport à la direction de prolongement du câblage de signal de balayage (17) ; ou
caractérisé en ce que
une fente (9) formée dans l'électrode de pixel transparente (8) du côté du substrat de matrice active (13) et s'étendant longue et fine, est disposée sensiblement dans une direction parallèle et dans une direction perpendiculaire par rapport à la direction de prolongement du câblage de signal de balayage (17) ; et une fente appartenant à la seconde structure d'électrode est disposée dans une direction selon un angle d'environ $\pm$45 degrés par rapport à la direction des câblages de signal de balayage ; ou
caractérisé en ce que
une fente (9) formée dans l'électrode de pixel transparente (8) du côté du substrat de matrice active (13) et s'étendant longue et fine, est disposée dans une direction selon un angle d'environ $\pm$45 degrés par rapport à la direction de prolongement du câblage de signal de balayage (17) ; et une fente appartenant à la seconde structure d'électrode est disposée dans une direction parallèle et dans une direction perpendiculaire par rapport à la direction de prolongement du câblage de signal de balayage (17) ; et l'électrode de commande de la direction d'alignement des cristaux liquides entoure une périphérie de l'électrode de pixel transparente tout en recouvrant partiellement l'électrode de pixel transparente via le film iso-

lant (12).

24. Ecran selon la revendication 17 ou 18, **caractérisé en ce que**
une fente (9) appartenant à la seconde structure d'électrode est disposée dans une direction parallèle et dans une direction perpendiculaire par rapport à la direction de prolongement du câblage de signal de balayage (17) de telle sorte que deux ou davantage de trous circulaires ou polygonaux (37) formés dans l'électrode de pixel transparente (8) du côté du substrat de matrice active sont entourés ; et l'électrode de commande de la direction d'alignement des cristaux liquides entoure une périphérie de l'électrode de pixel transparente tout en recouvrant partiellement l'électrode de pixel transparente via le film isolant (12).

25. Ecran selon l'une quelconque des revendications 15 à
24, **caractérisé en ce que**
l'électrode de commande de la direction d'alignement des cristaux liquides (15) est formée sur la même couche que le câblage de signal de balayage (17) ; ou
caractérisé en ce que
l'électrode de commande de la direction d'alignement des cristaux liquides (15) est formée sur la même couche que le câblage de signal vidéo (11) .

26. Ecran selon l'une quelconque des revendications 15 à
18, **caractérisé en ce que**
deux éléments de transistor à couche peu épaisse (16) sont requis dans un pixel afin de commander le seul pixel et seulement un trou de contact (18) existe pour raccorder électriquement l'électrode de drain d'un élément de transistor à couche peu épaisse formé dans une position où le câblage de signal de balayage (17) de la rangée n et le câblage de signal vidéo (11) de la colonne m se croisent, et l'électrode de pixel transparente (8) ; ou
caractérisé en ce que
deux éléments de transistor à couche peu épaisse (16) sont requis dans un pixel afin de commander le seul pixel ; deux trous de contact (61, 62) existent pour raccorder électriquement l'électrode de drain d'un élément de transistor à couche peu épaisse formé dans une position où le câblage de signal de balayage (17) de la rangée (n - 1) et le câblage de signal vidéo (11) de la colonne (m + 1) se croisent, et l'électrode de commande de la direction d'alignement des cristaux liquides (15) ; et seulement un trou de contact (18) existe pour raccorder électriquement l'électrode de drain d'un élément de transistor à couche peu épaisse formé dans une position où le câblage de signal de balayage de la rangée n et le câblage de signal vidéo de la colonne m se croisent, et l'électrode de pixel transparente (8) ; ou
caractérisé en ce que
deux éléments de transistor à couche peu épaisse (16) sont requis dans un pixel afin de commander le seul pixel ; et un élément de transistor à couche peu épaisse est raccordé à l'électrode de pixel transparente (8), l'autre élément de transistor à couche peu épaisse restant est raccordé à l'électrode de commande de la direction d'alignement des cristaux liquides (15), et l'électrode de pixel transparente et l'électrode de commande de la direction d'alignement des cristaux liquide sont recouverts via le film isolant (12) pour former une capacité.

27. Ecran selon l'une quelconque des revendications 15 à
26, **caractérisé en ce que**
une électrode intermédiaire (67) du premier élément de transistor à couche peu épaisse raccordé à l'électrode de commande de la direction d'alignement des cristaux liquide (15) et l'électrode de pixel transparente (8) se recouvrent partiellement via le film isolant (12) pour former une capacité, et le premier transistor à couche peu épaisse a une structure à deux transistors.

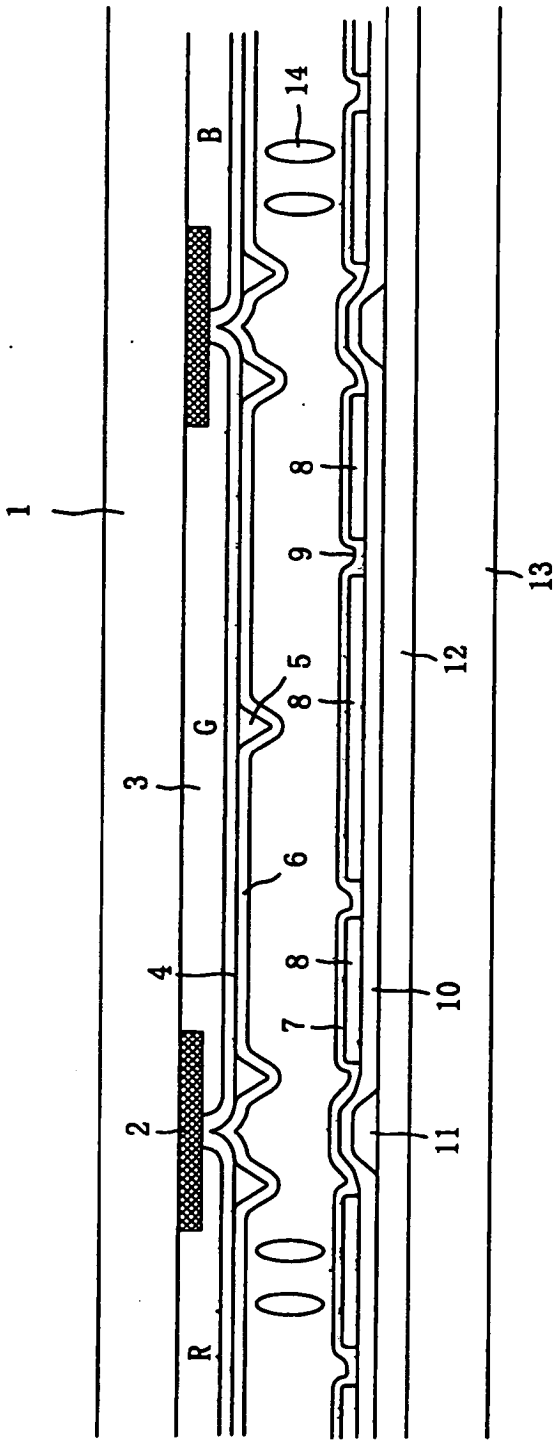
28. Ecran selon la revendication 15 ou 17, **caractérisé en ce que**
l'électrode de pixel transparente (8) de la rangée n et de la colonne m et le câblage de signal de balayage (17) de la $(n - 1)^{ème}$ rangée se chevauchent via le film isolant (12) pour former un condensateur de stockage.

29. Ecran selon la revendication 16 ou 18, **caractérisé en ce que**
l'électrode de pixel transparente (8) de la rangée n et de la colonne m et le câblage de l'électrode commune (48) de la rangée n se chevauchent via le film isolant (12) pour former un condensateur de stockage.

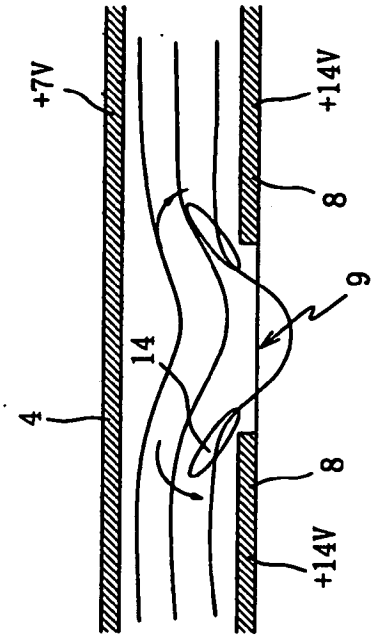
30. Ecran selon l'une quelconque des revendications 15 à
29, **caractérisé en ce que**
l'élément de transistor à couche peu épaisse, le câblage de signal vidéo et l'électrode de commande de la direction d'alignement des cristaux liquide sont prévus sur la même couche.

31. Procédé de fabrication d'un écran selon la revendication 30, **caractérisé en ce que**
l'élément de transistor à couche peu épaisse, le câblage de signal vidéo et l'électrode de commande de la direction d'alignement des cristaux liquide sont préparés en même temps, en utilisant une technique d'exposition en demi-teinte.

Fig. 1



PRIOR ART



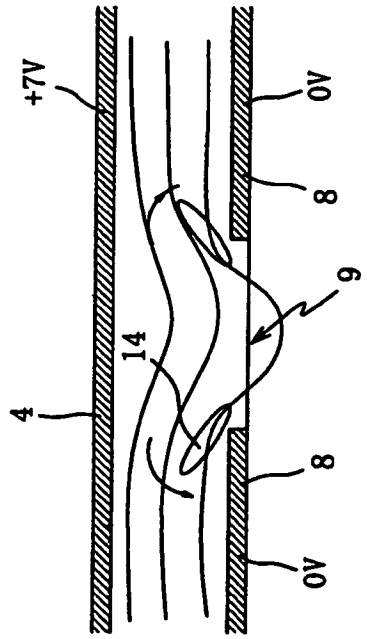
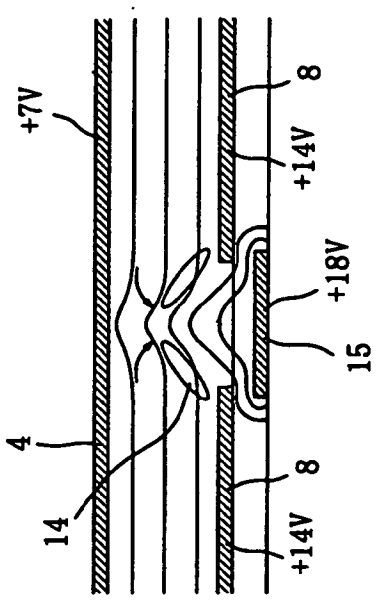


Fig. 2



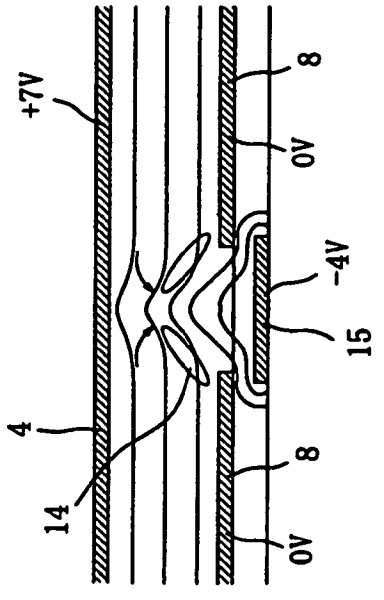


Fig. 3

Fig. 4

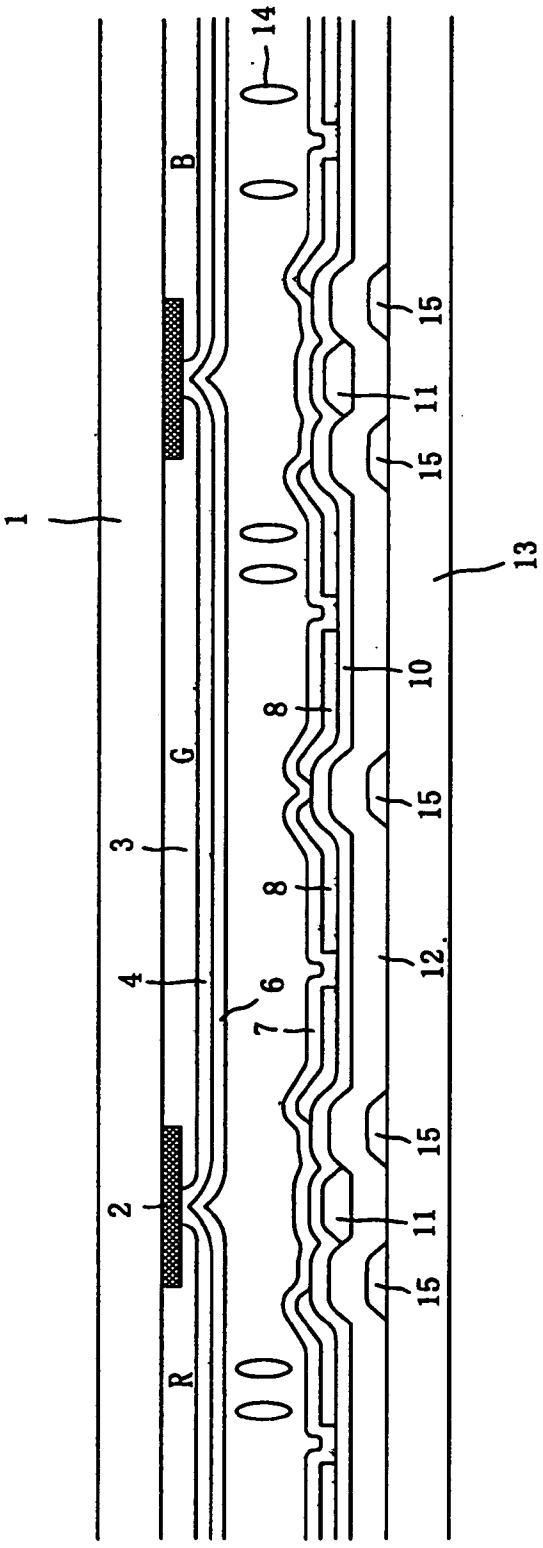


Fig. 5

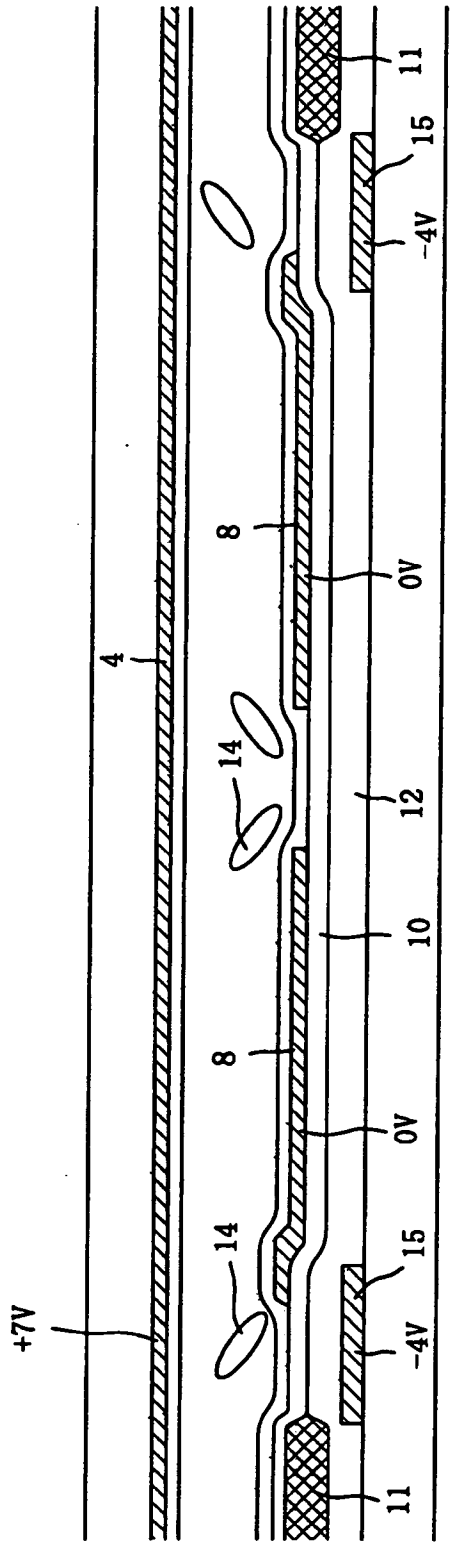


Fig. 6

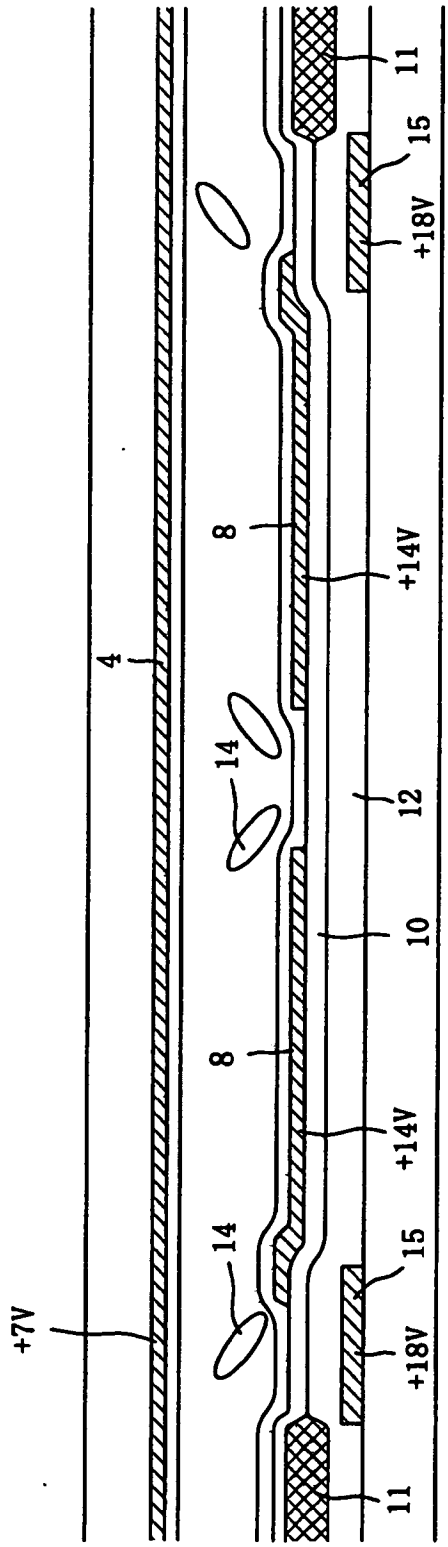


Fig. 7

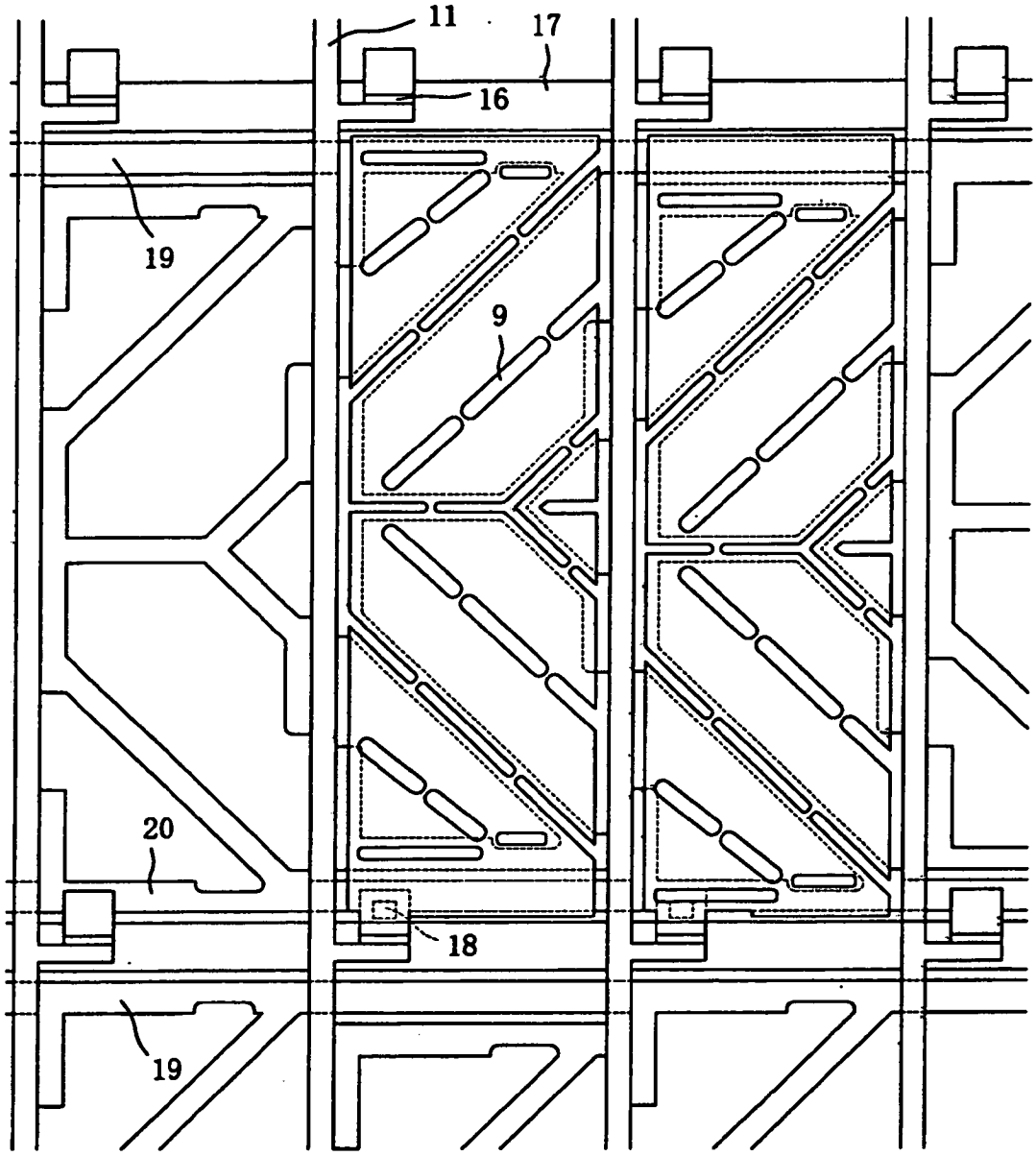


Fig. 8

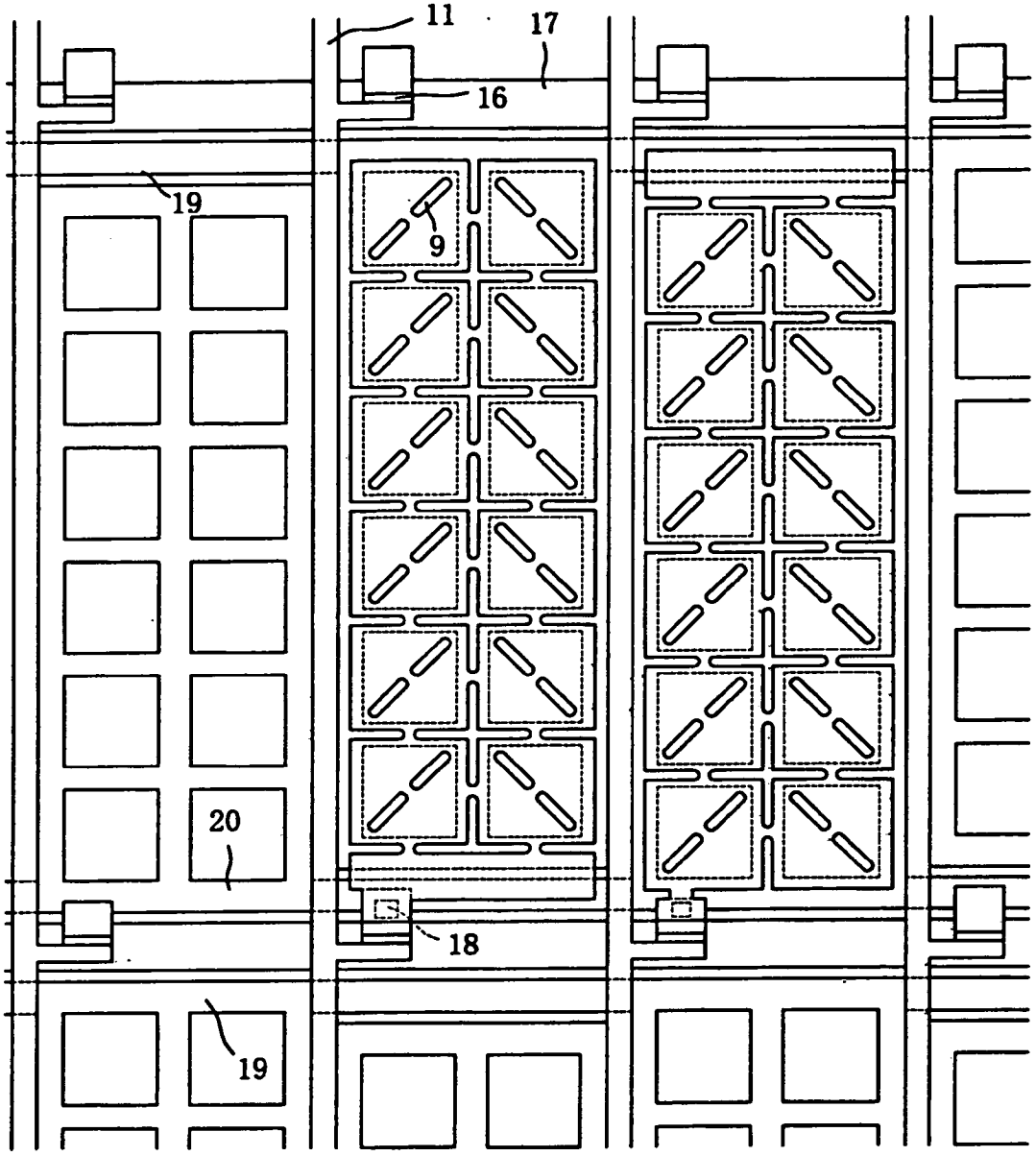


Fig. 9

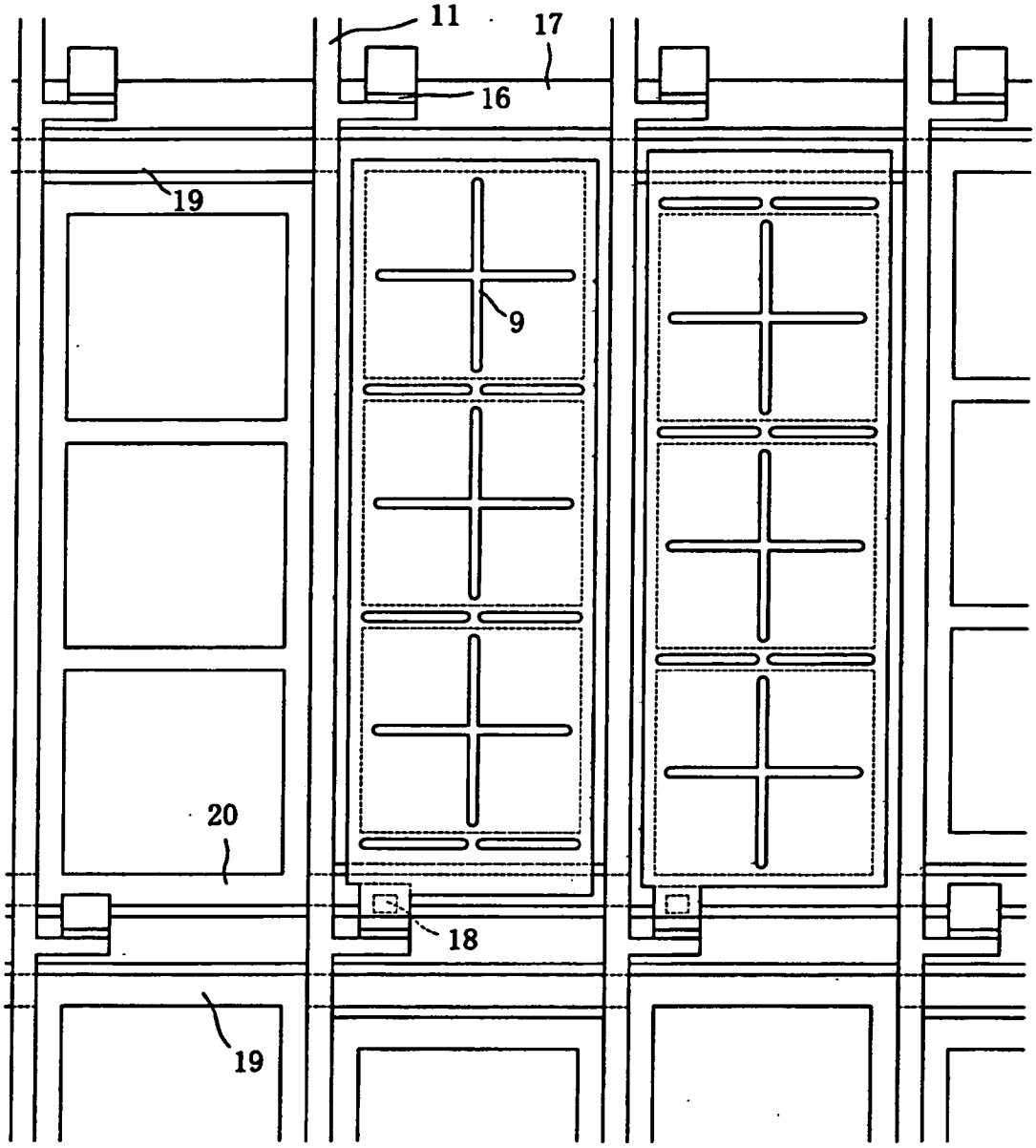


Fig. 10

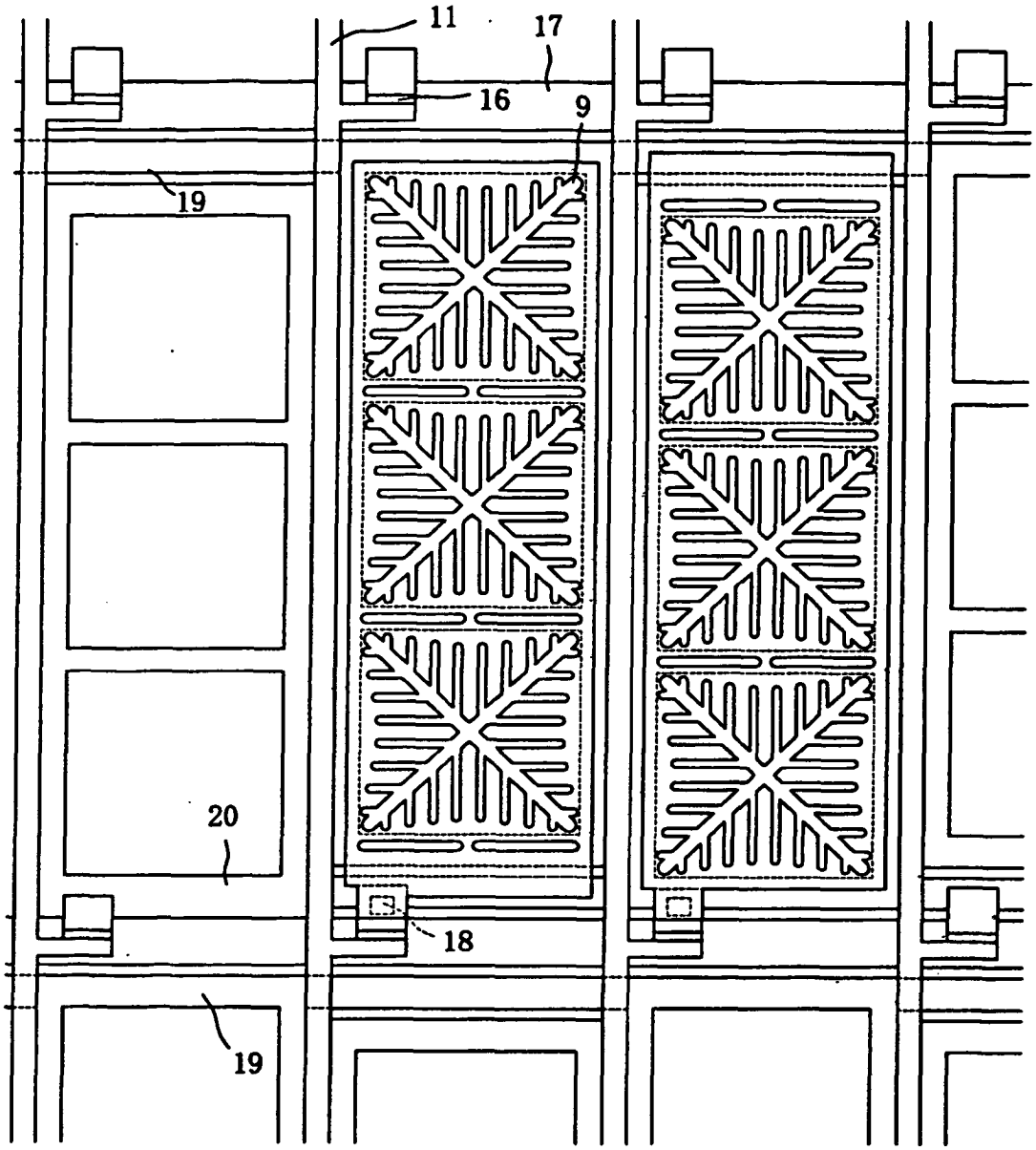


Fig. 11

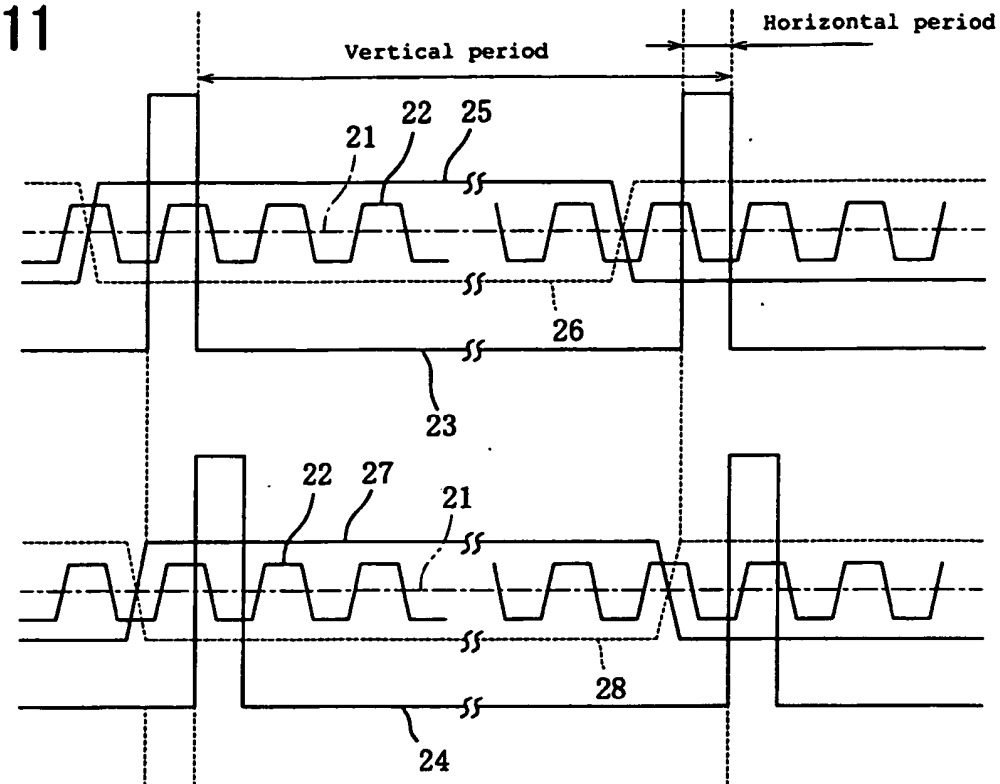

Horizontal period
Vertical period
21
22
25
26
23
22
27
21
28
24

Fig. 12

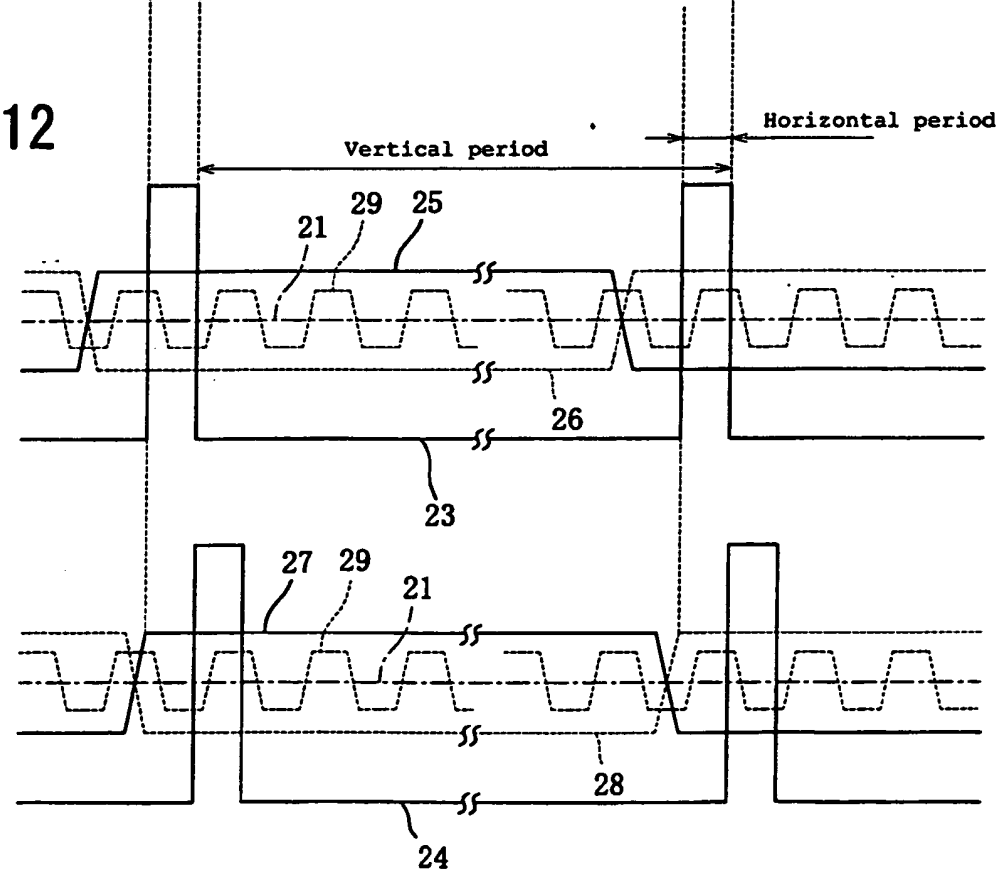

Horizontal period
Vertical period
21
29
25
26
23
27
29
21
28
24

Fig. 13

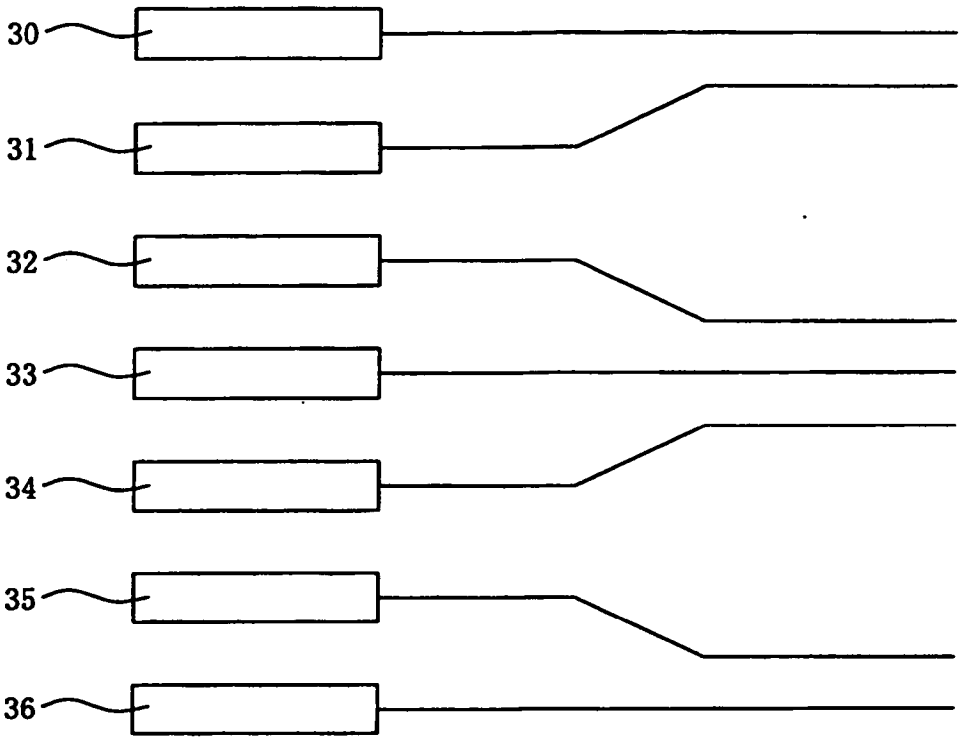


Fig. 14

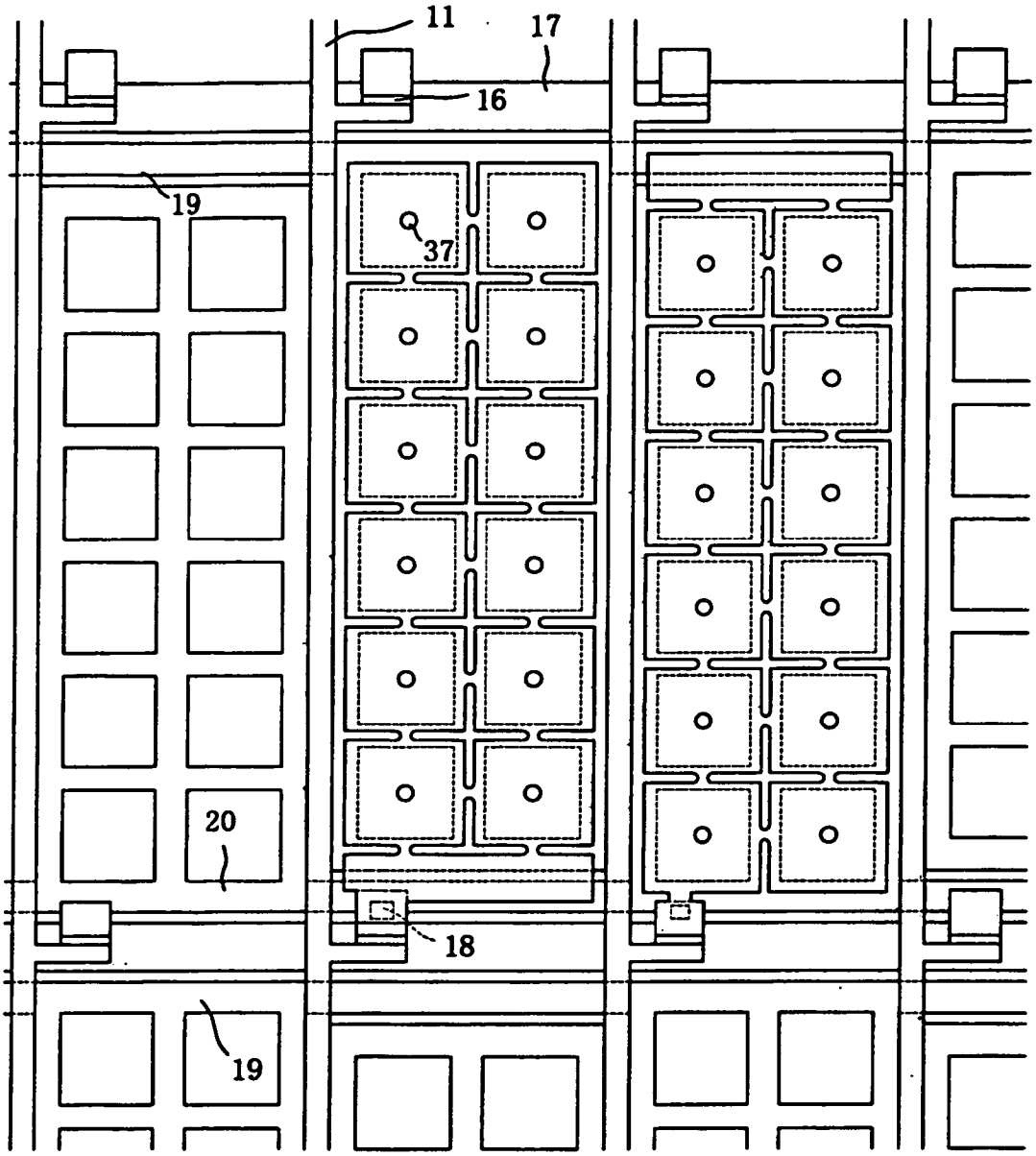


Fig. 15

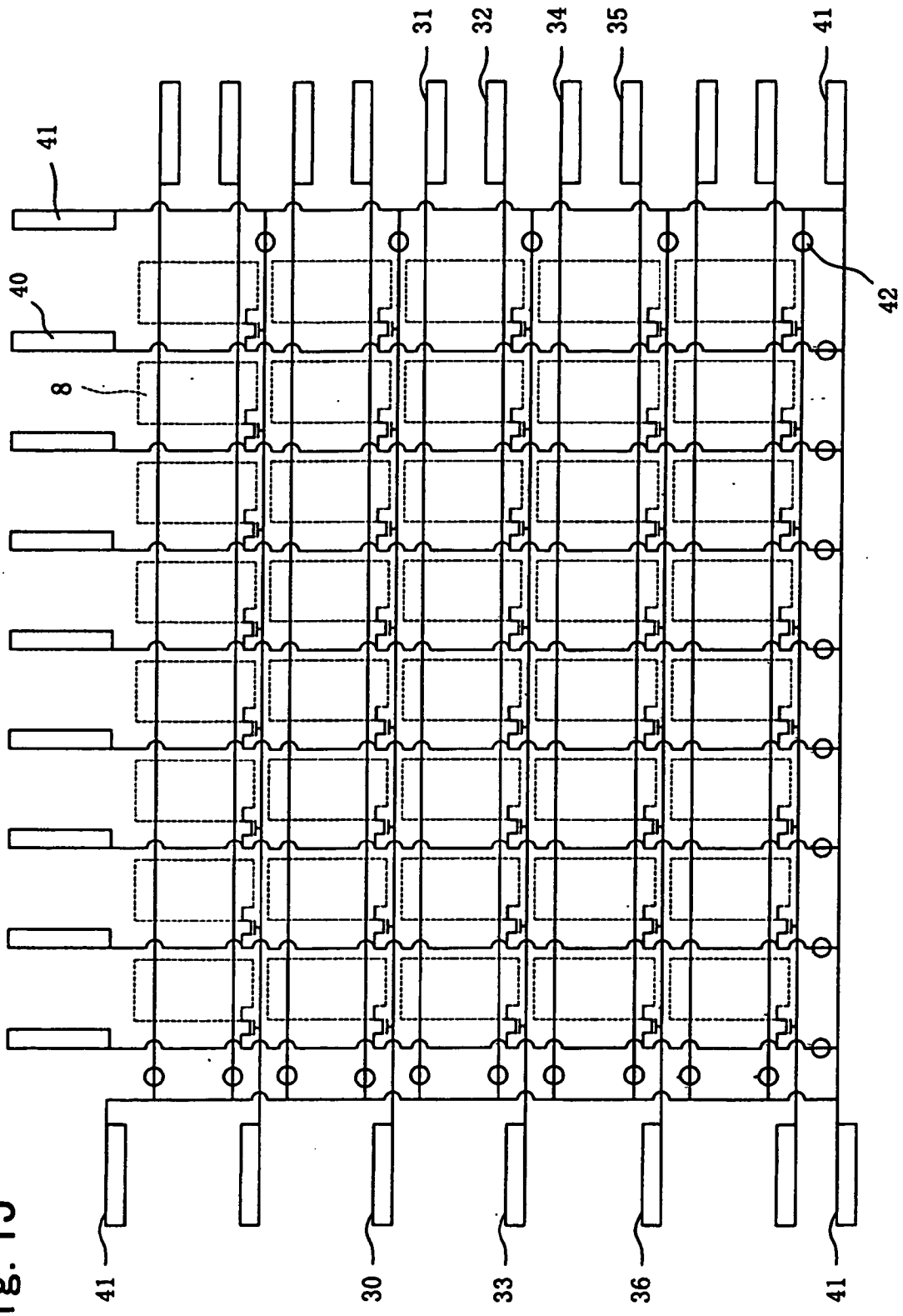


Fig. 16

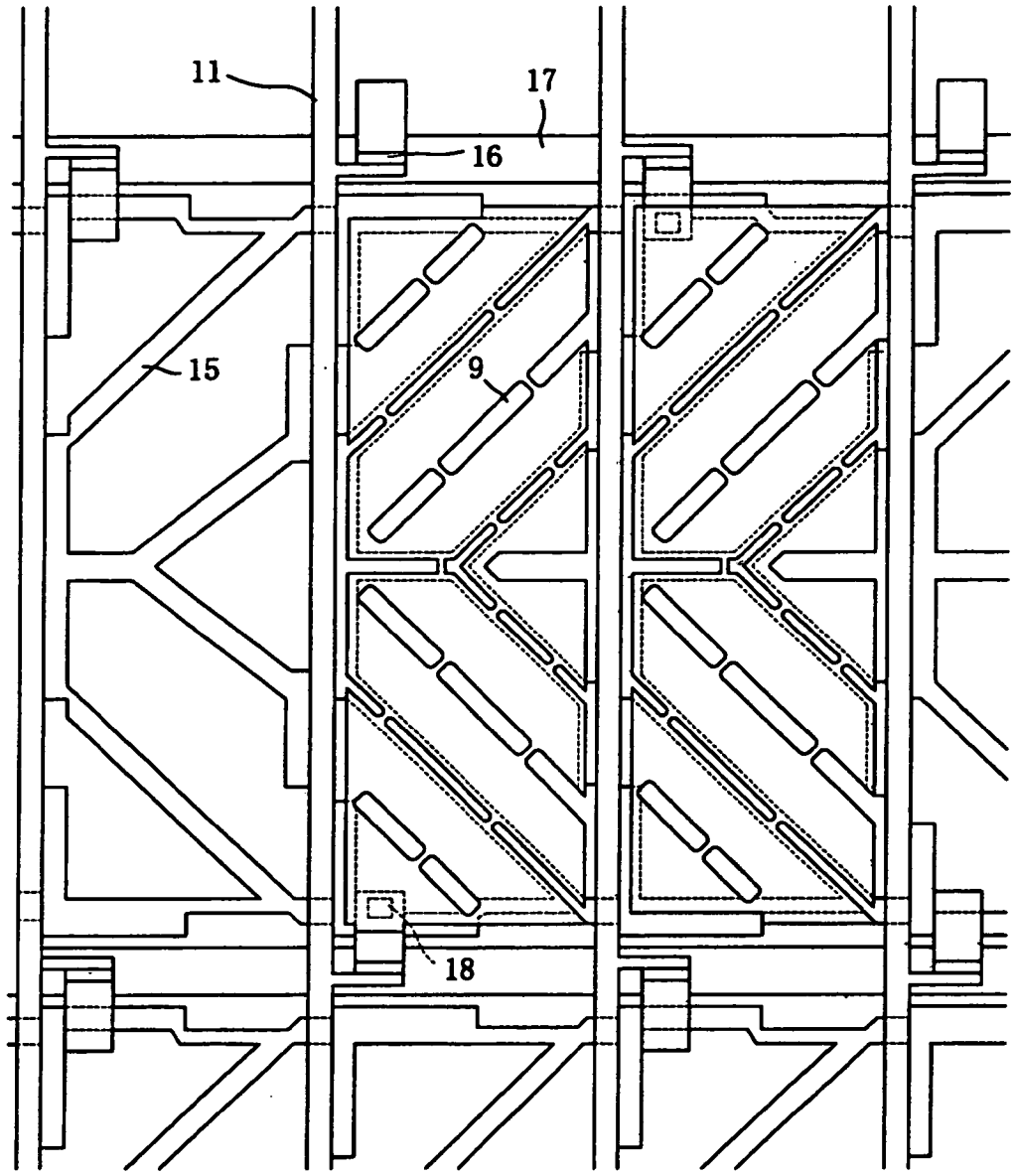


Fig. 17

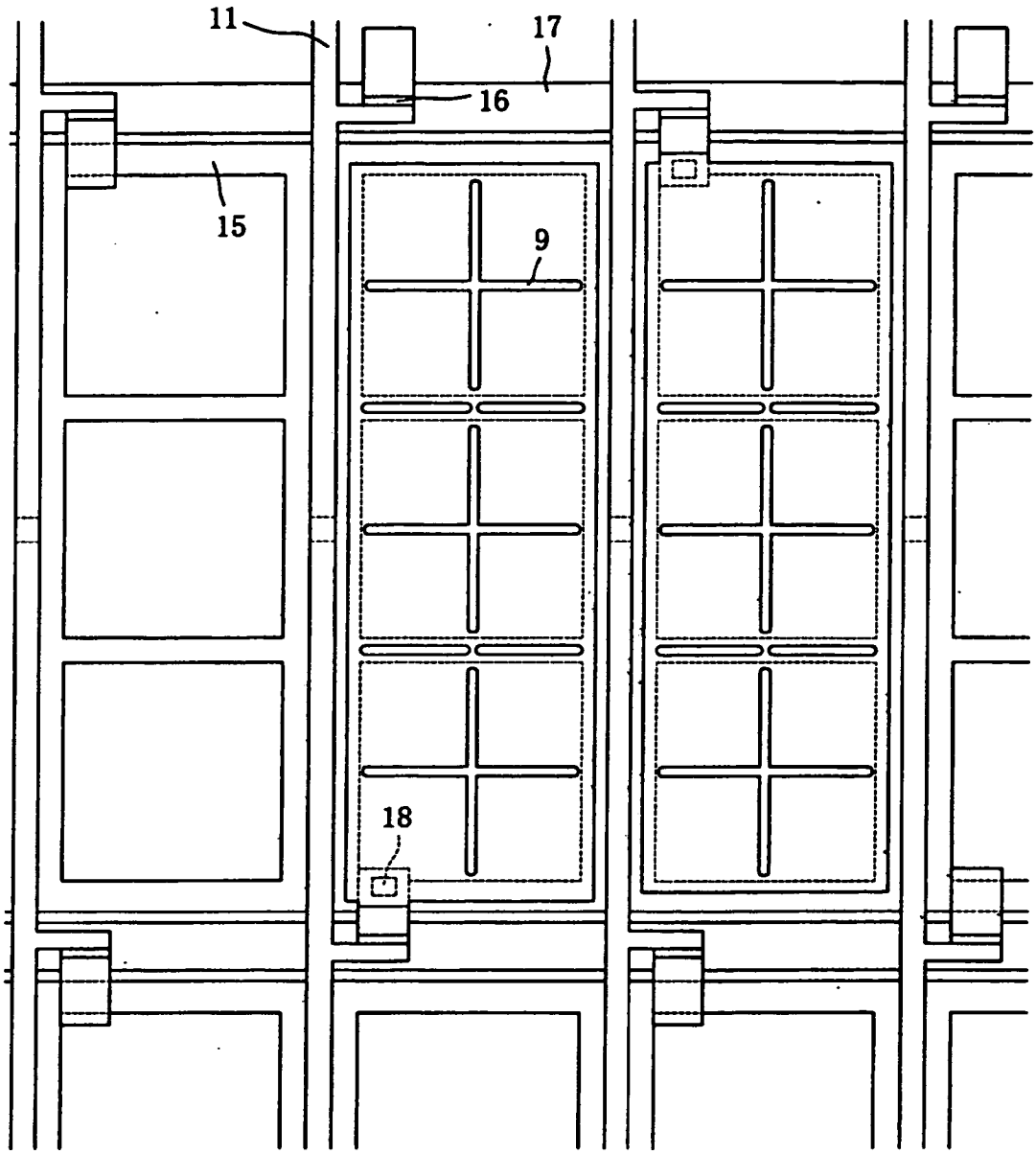


Fig. 18

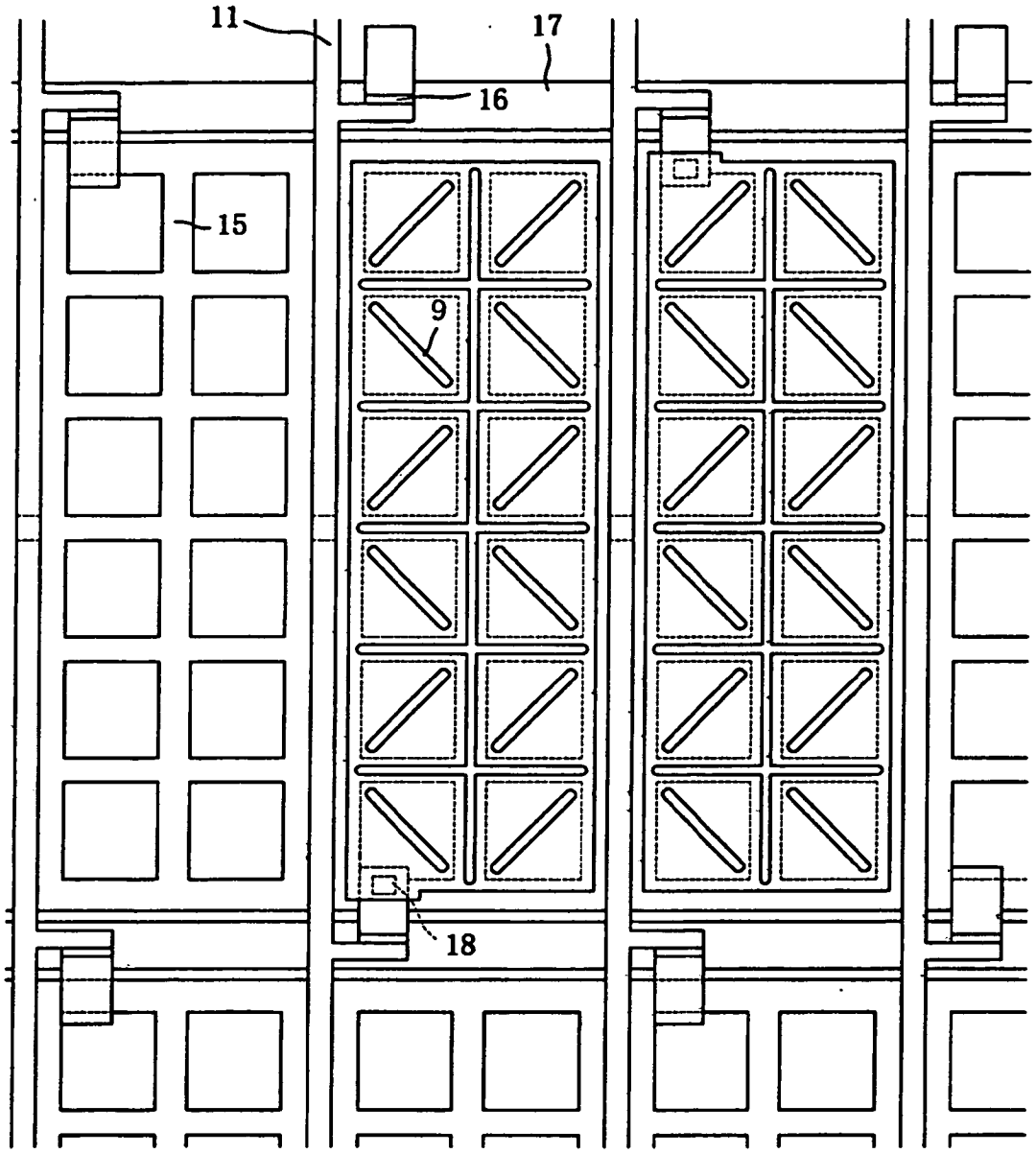
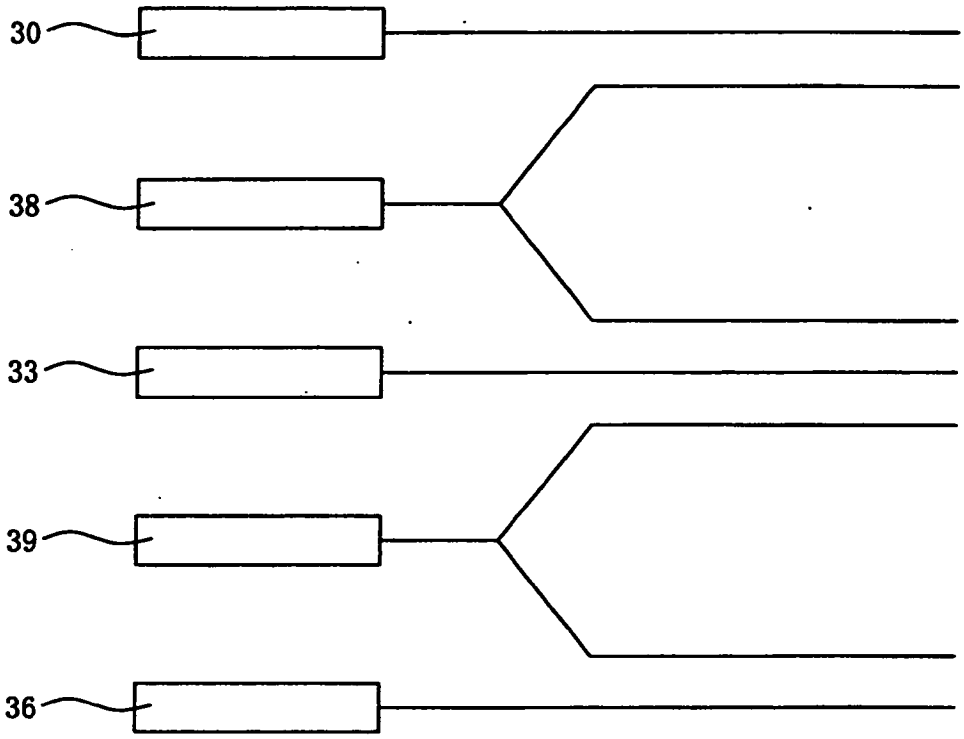


Fig. 19



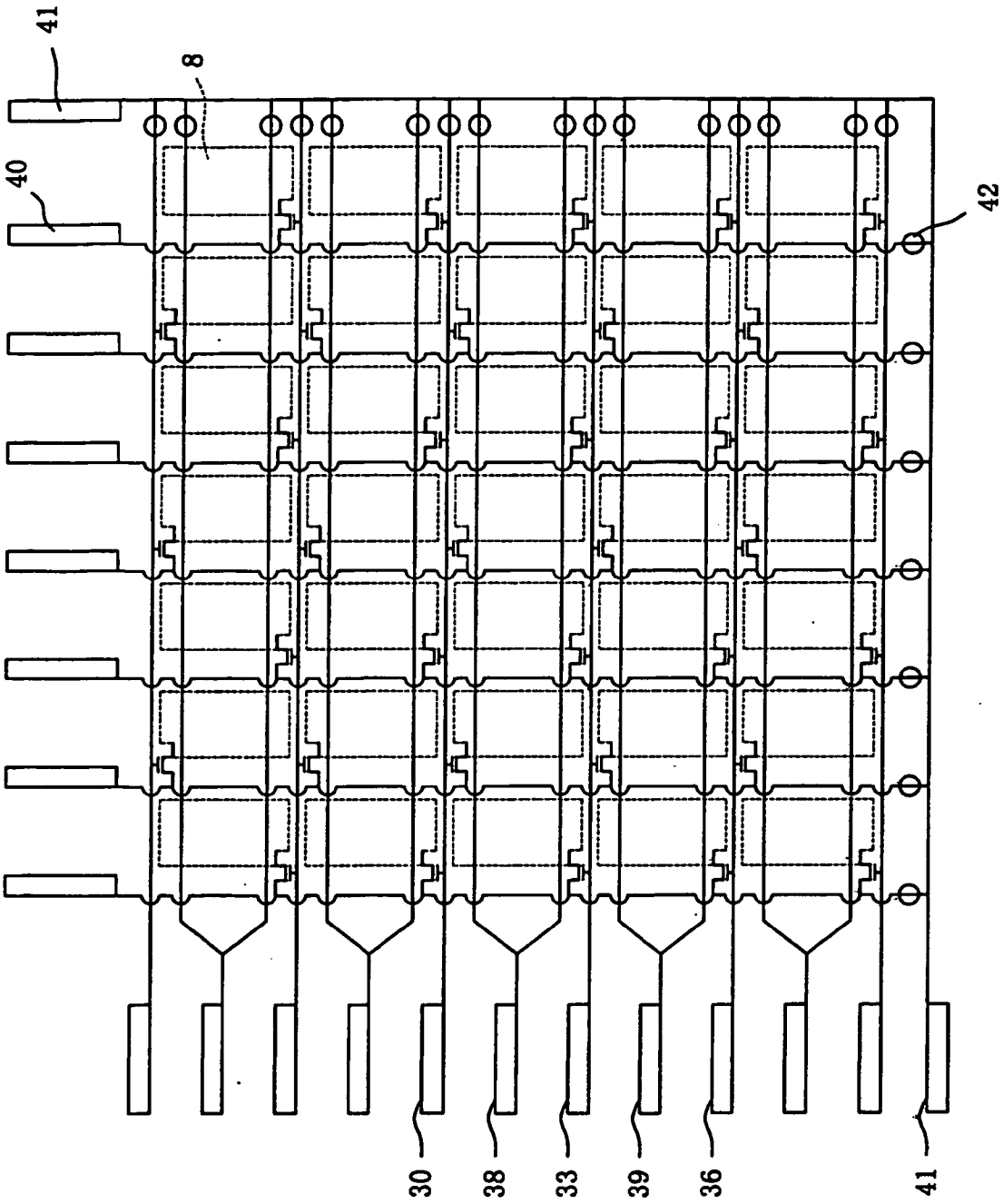


Fig. 20

Fig. 21

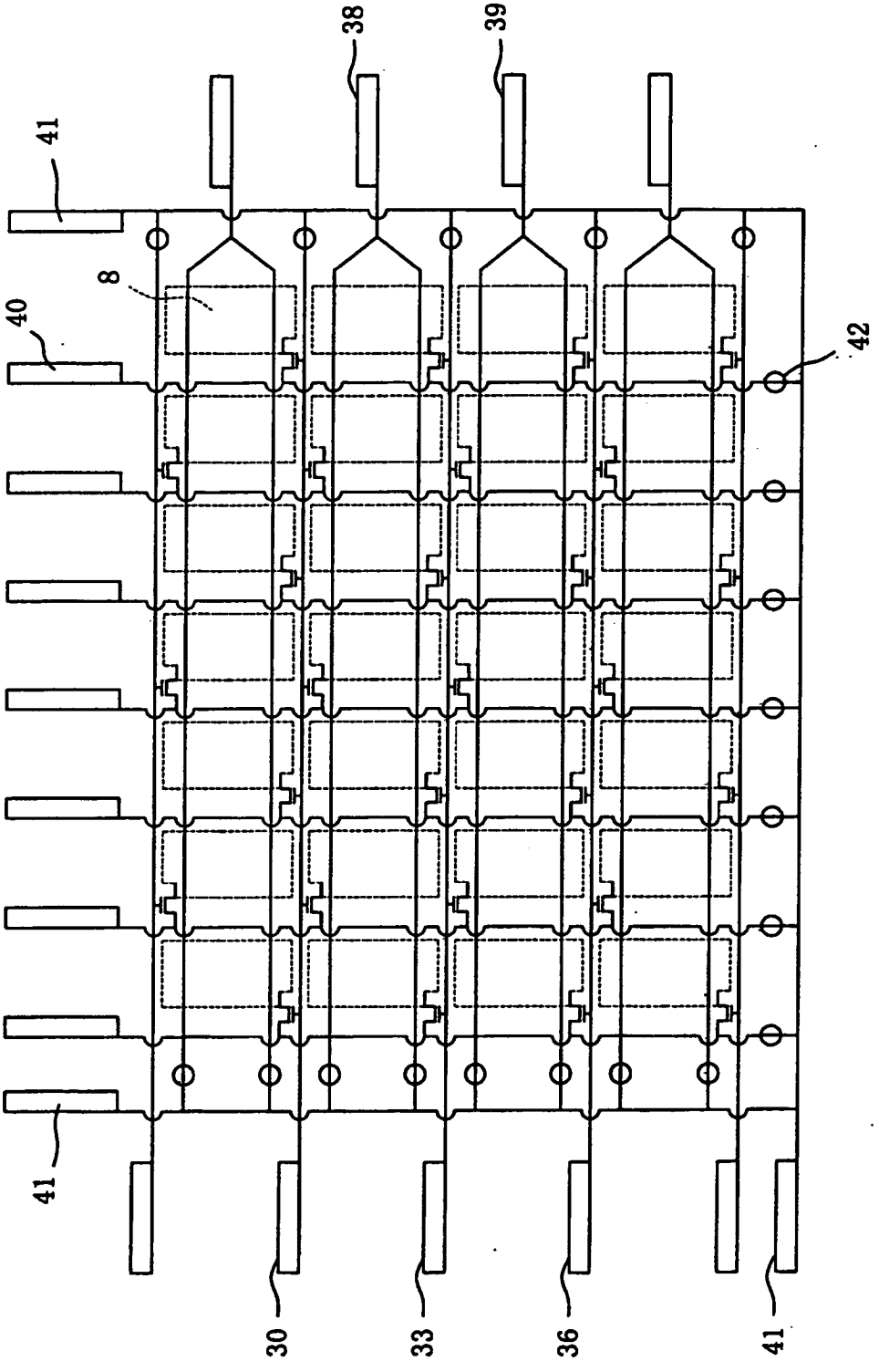


Fig. 22

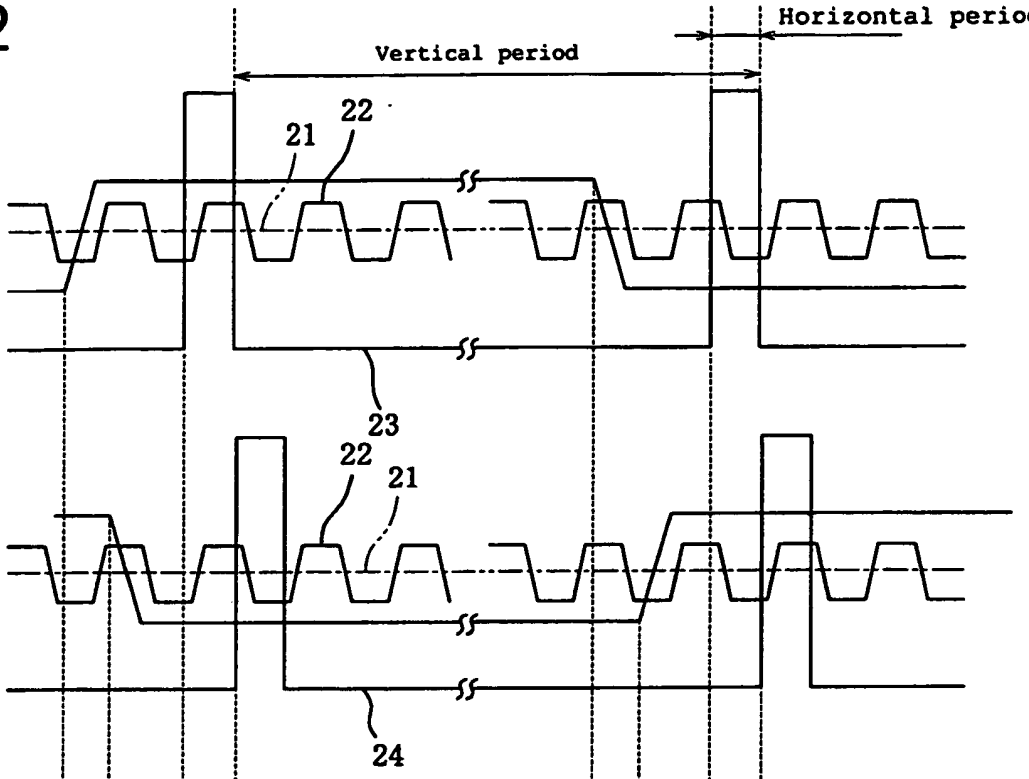

Horizontal period
Vertical period
21
22
23
22
21
24

Fig. 23

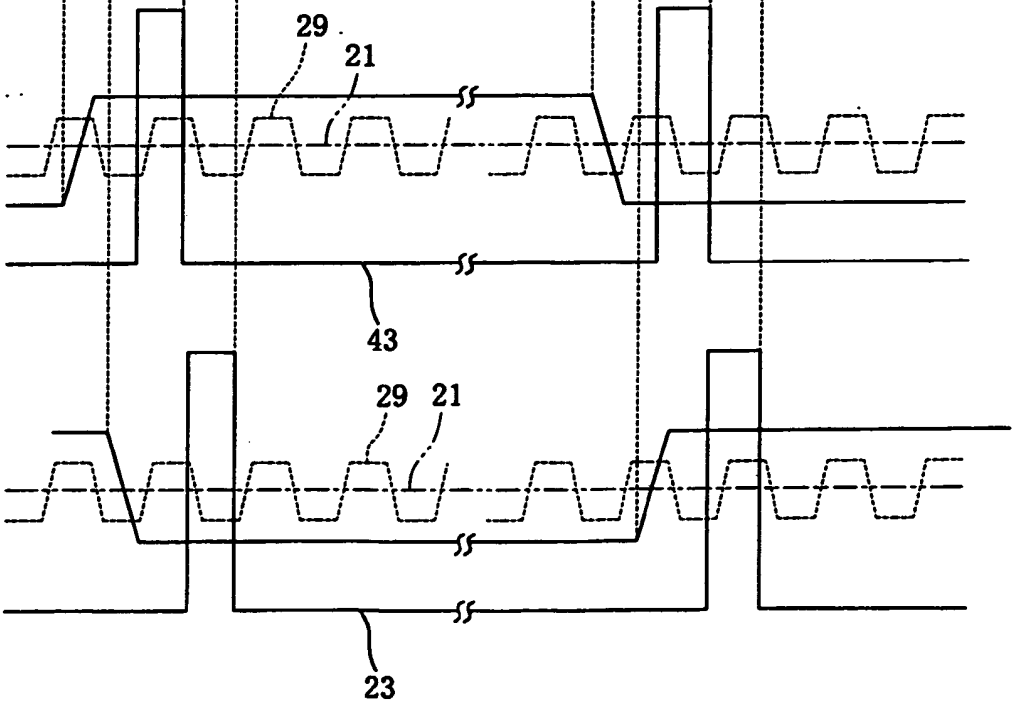

29
21
43
29
21
23

Fig. 24

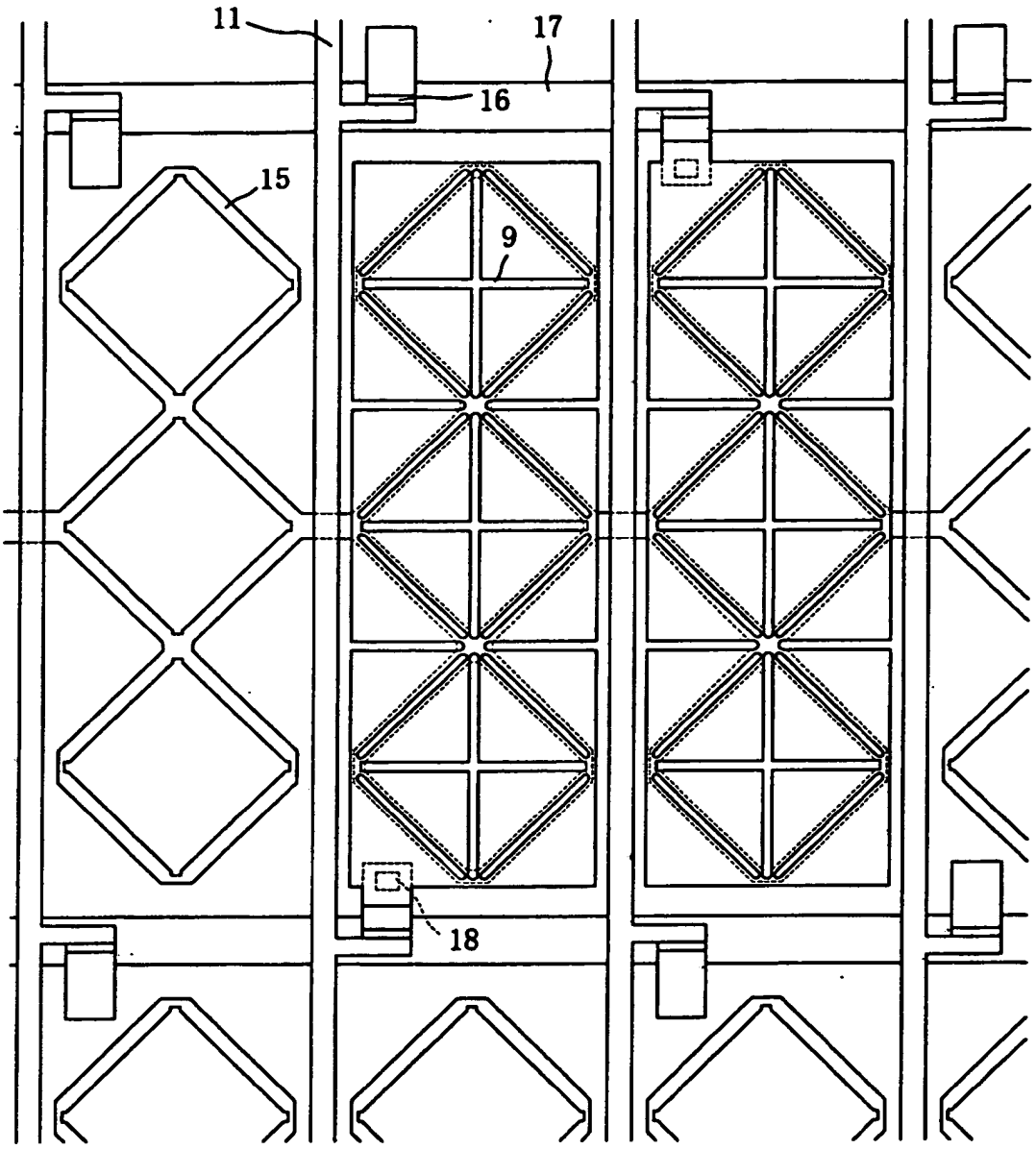
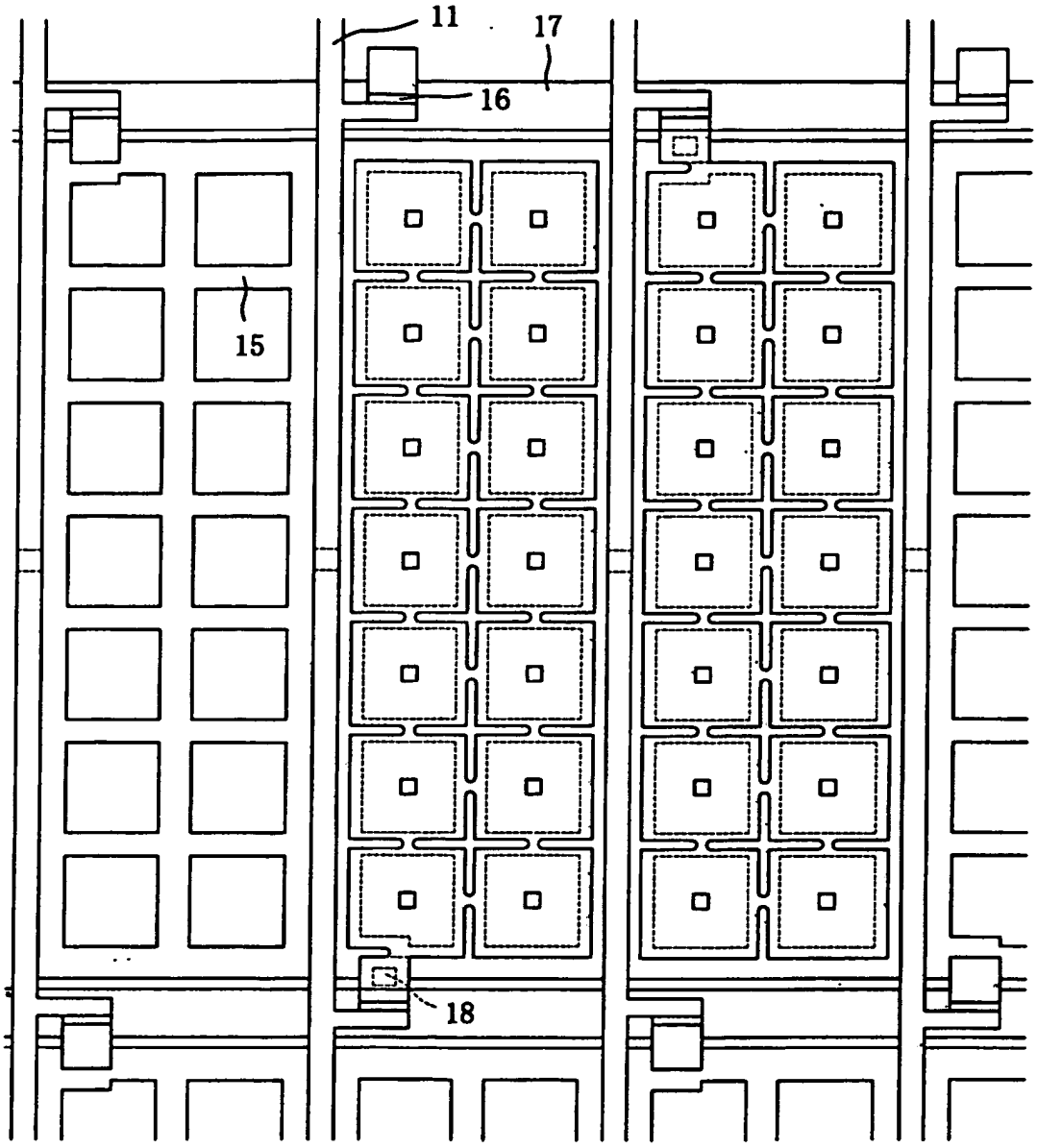


Fig. 25



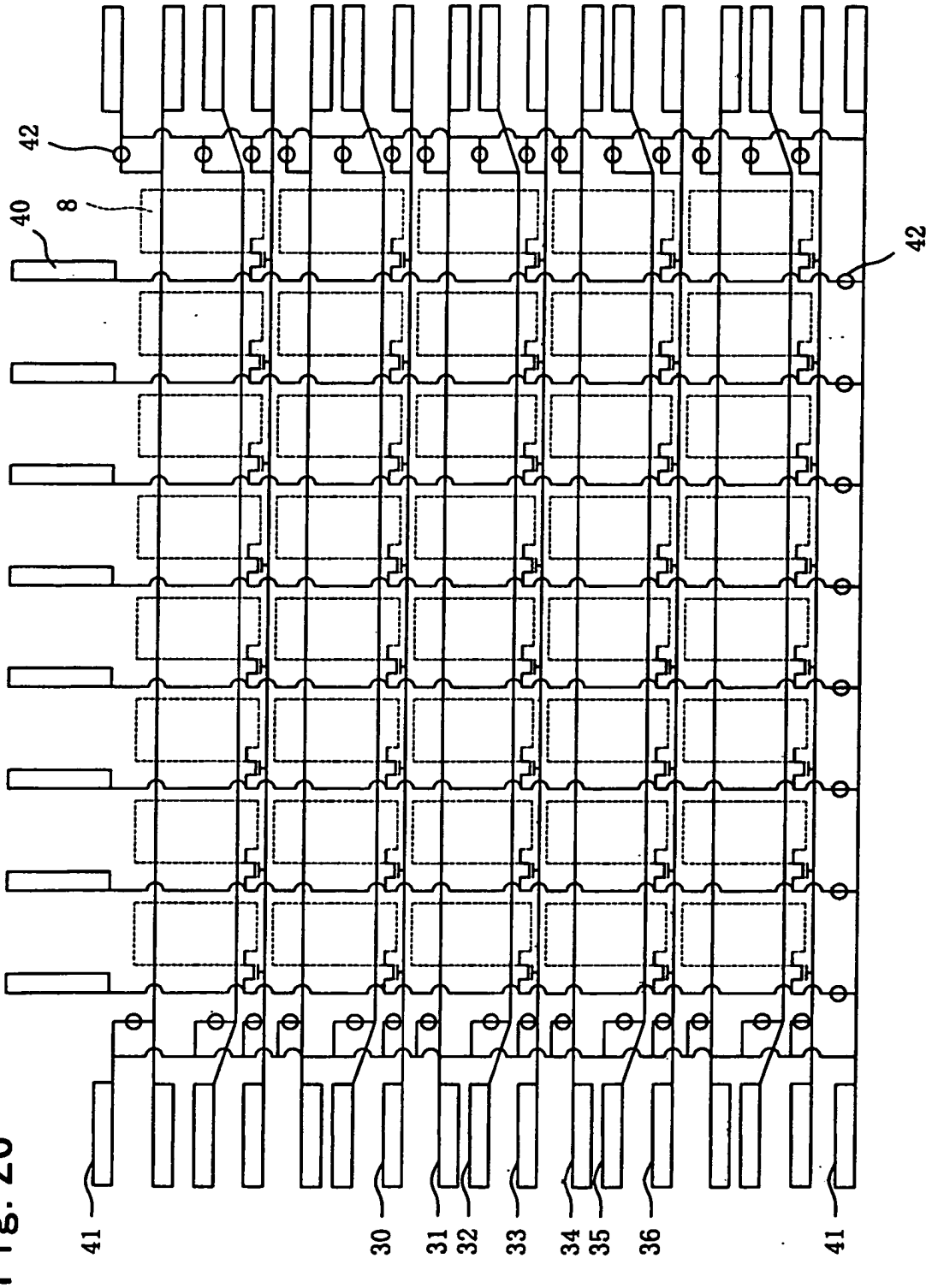


Fig. 26

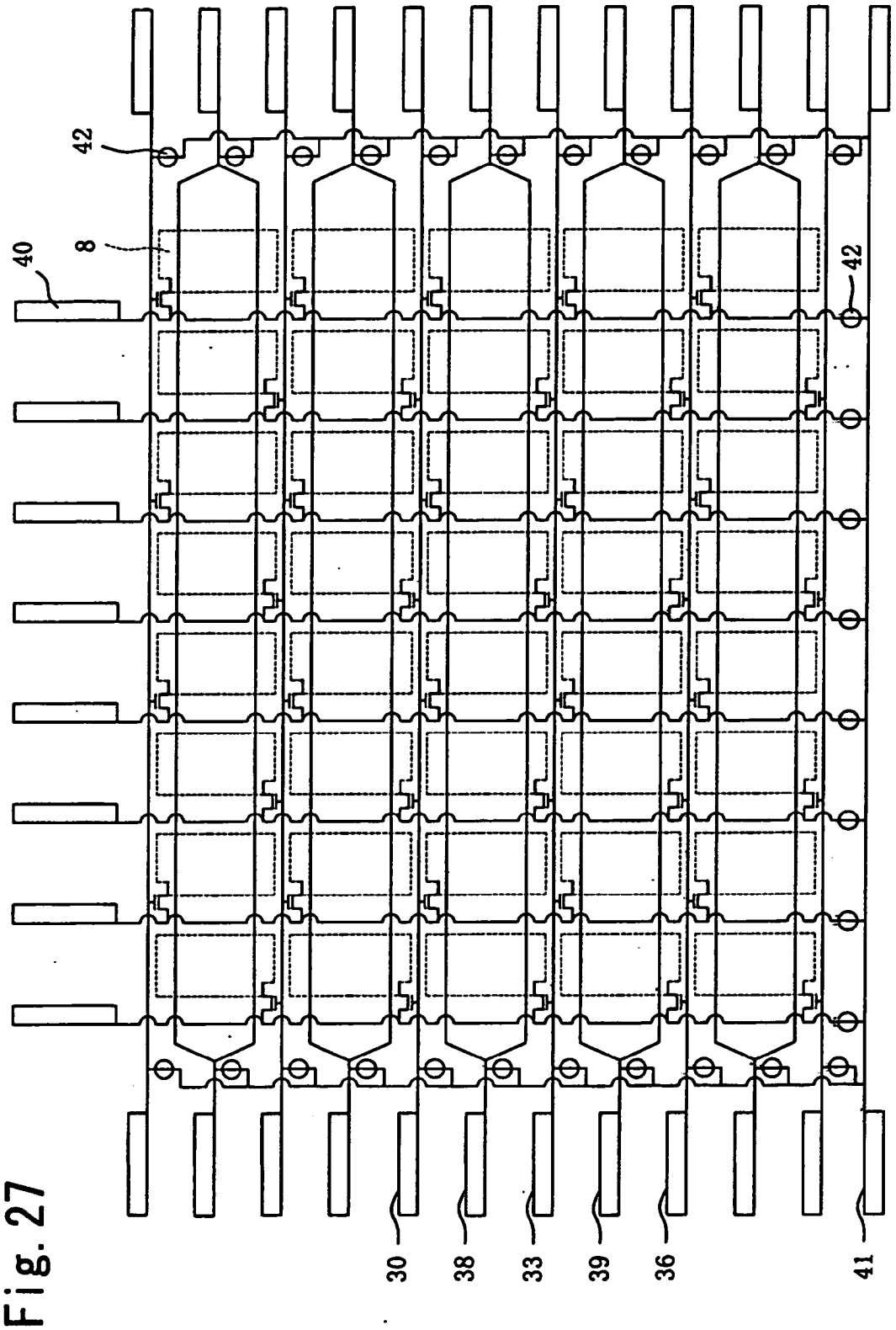


Fig. 27

Fig. 28

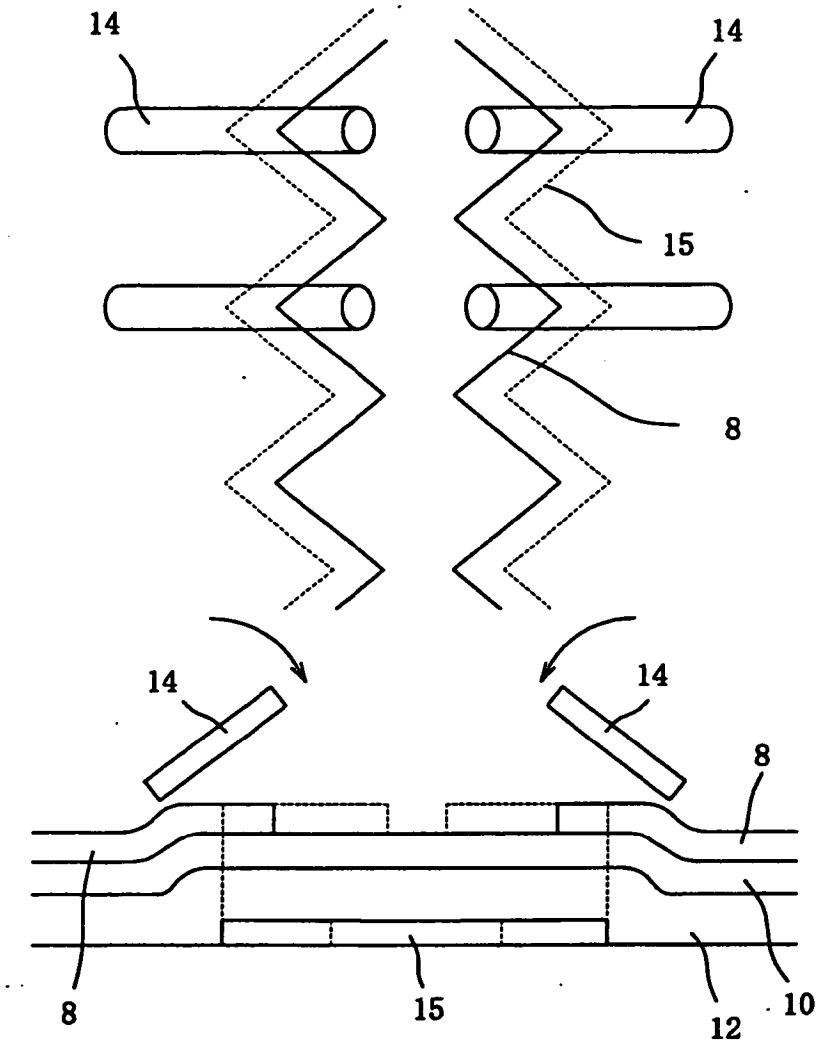


Fig. 29

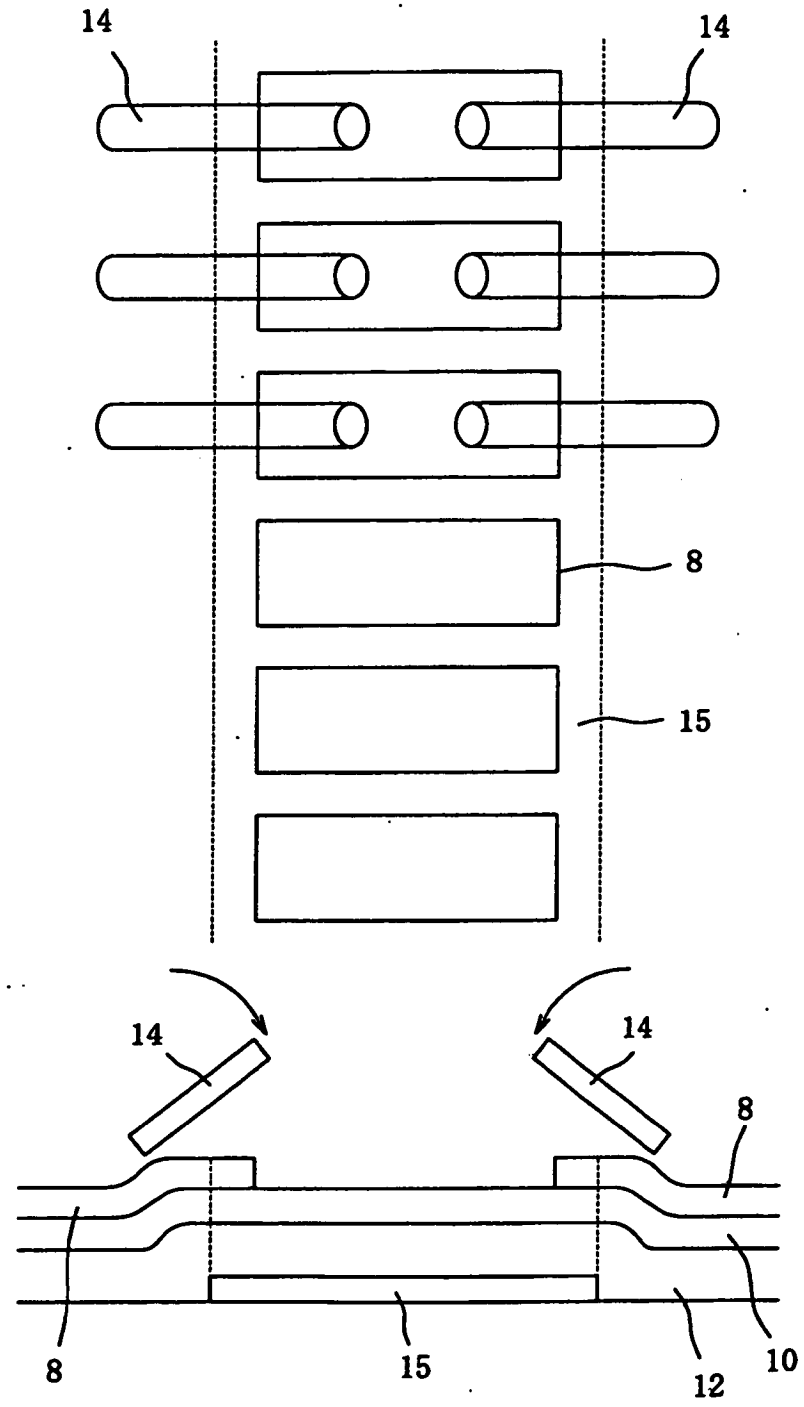


Fig. 30

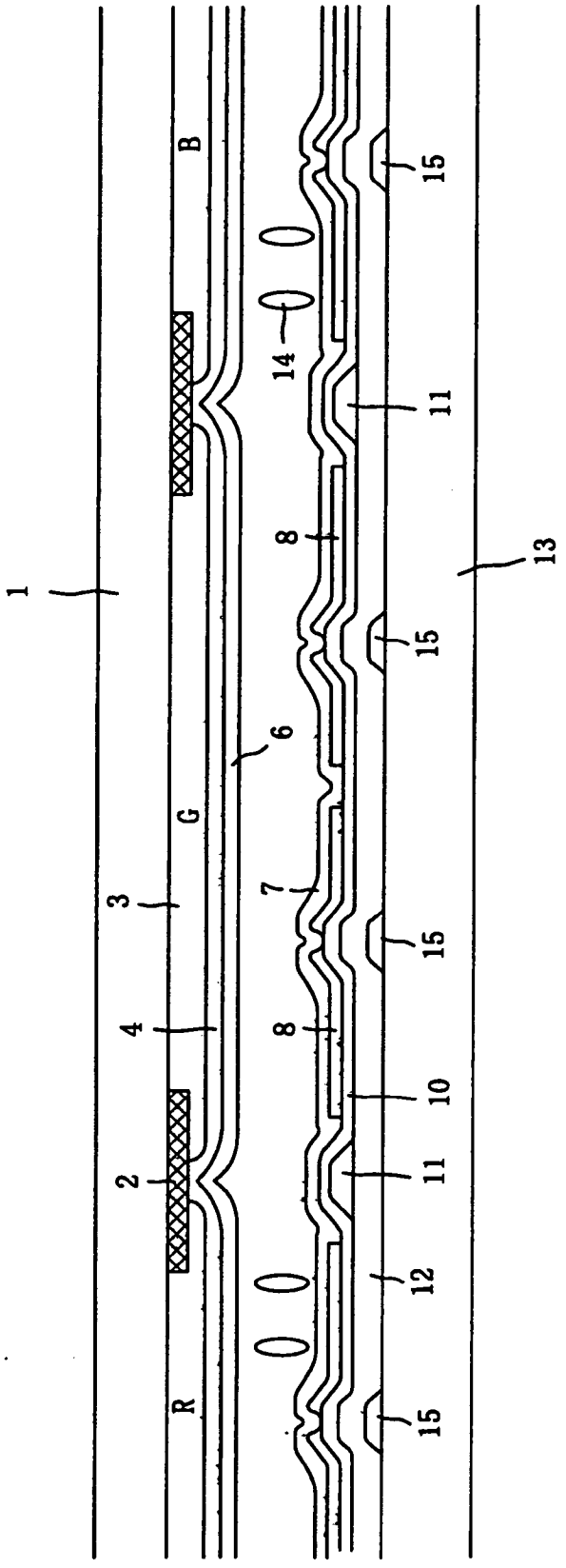


Fig. 31

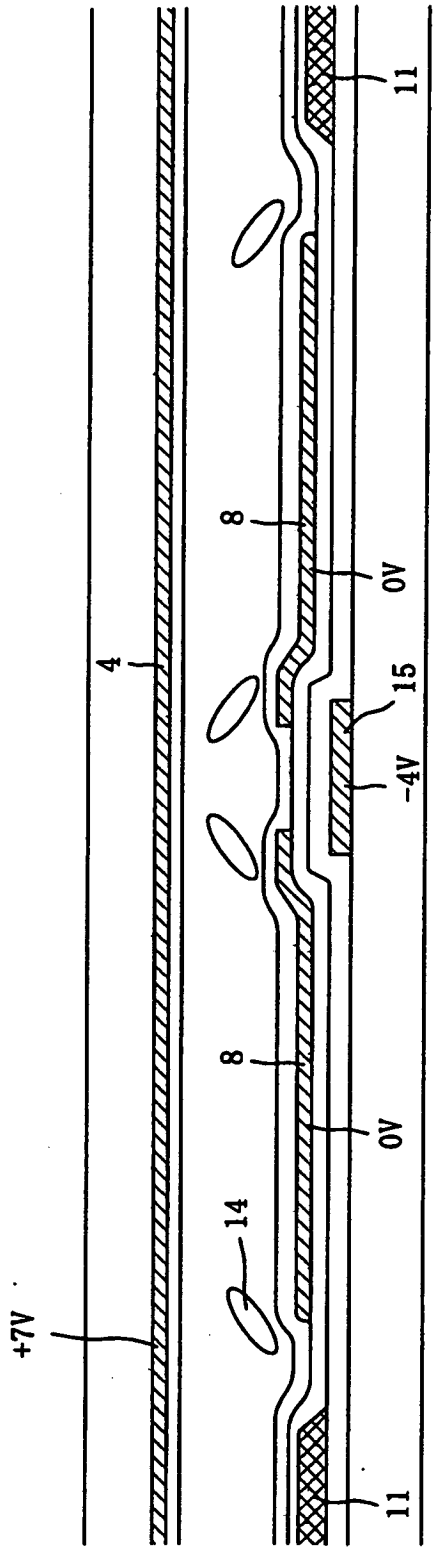


Fig. 32

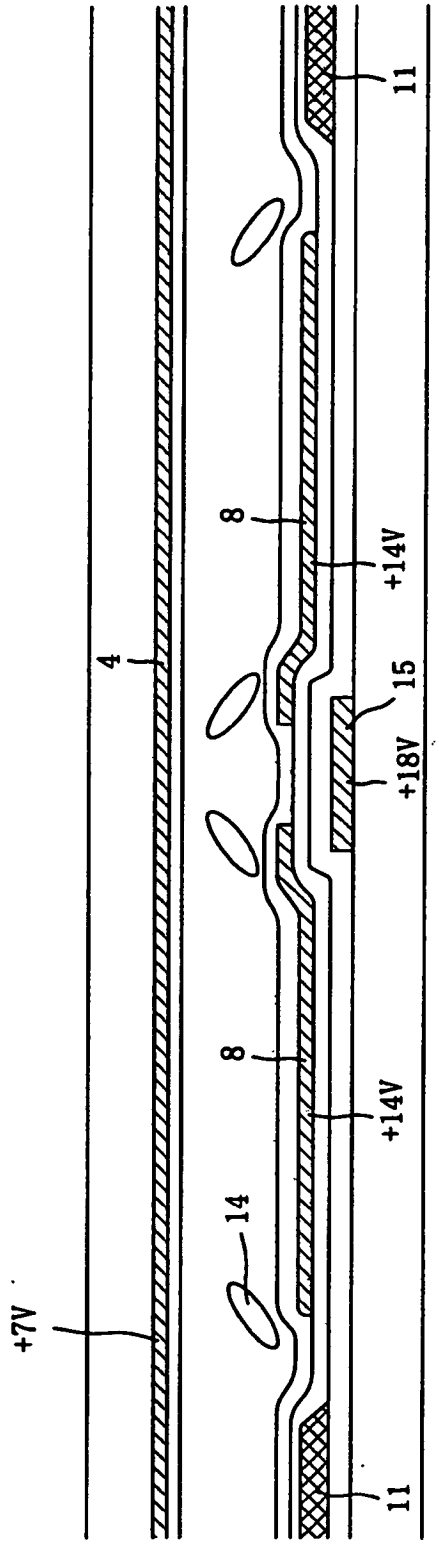


Fig. 33

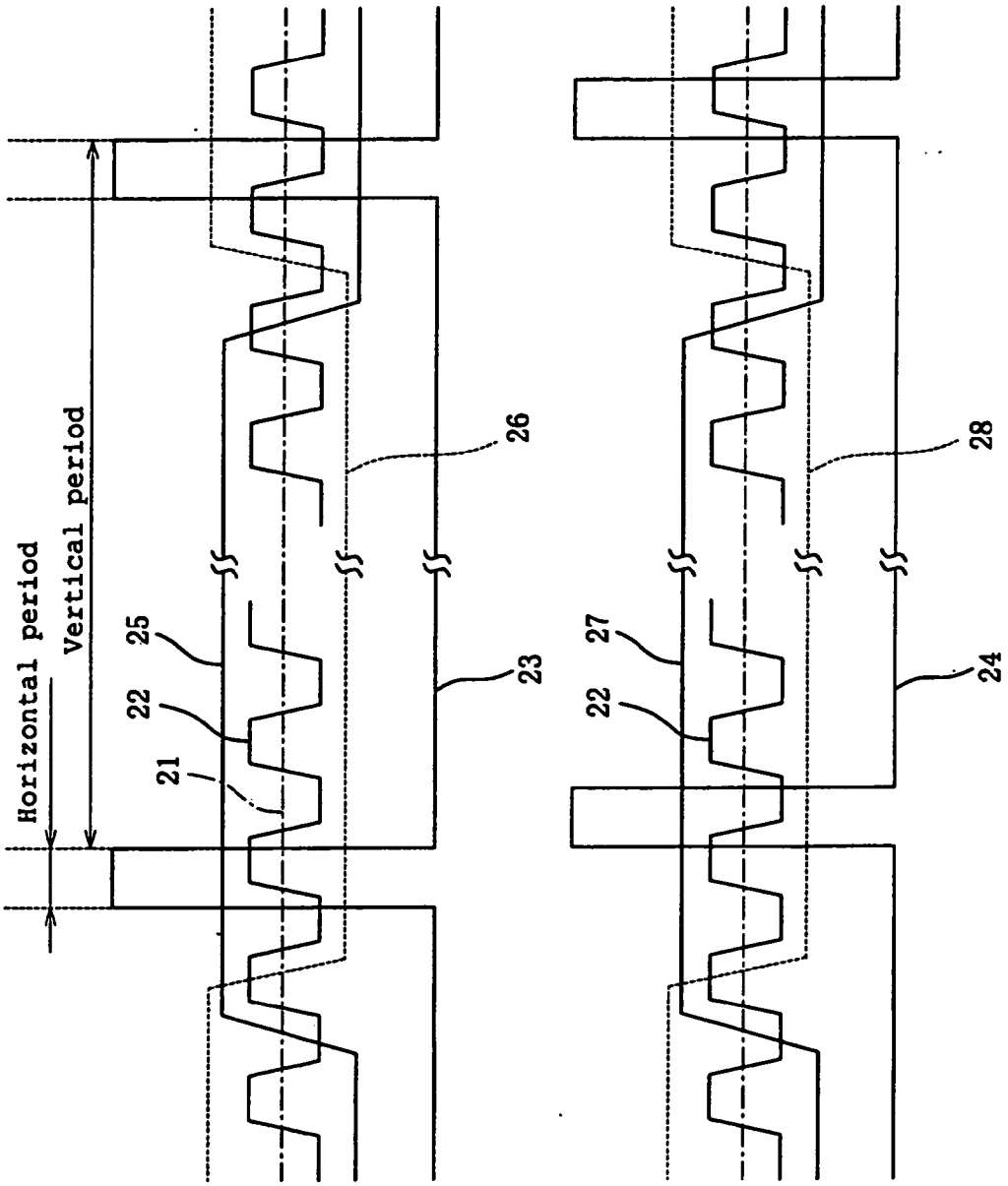
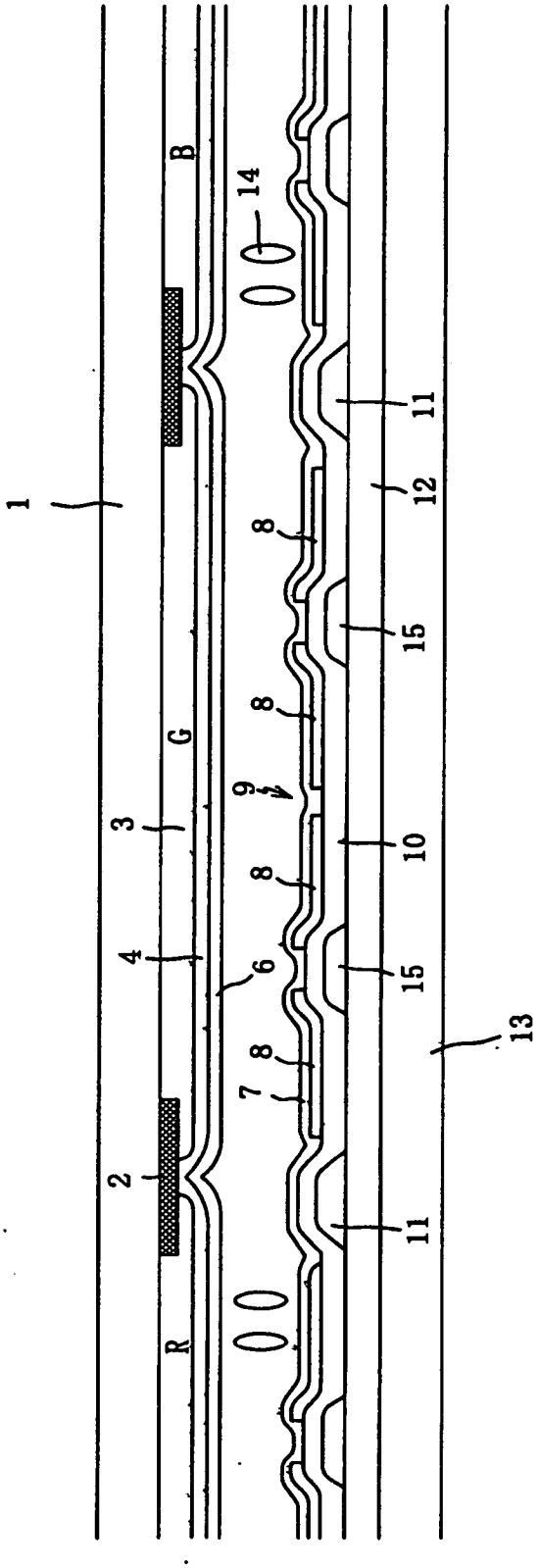


Fig. 34



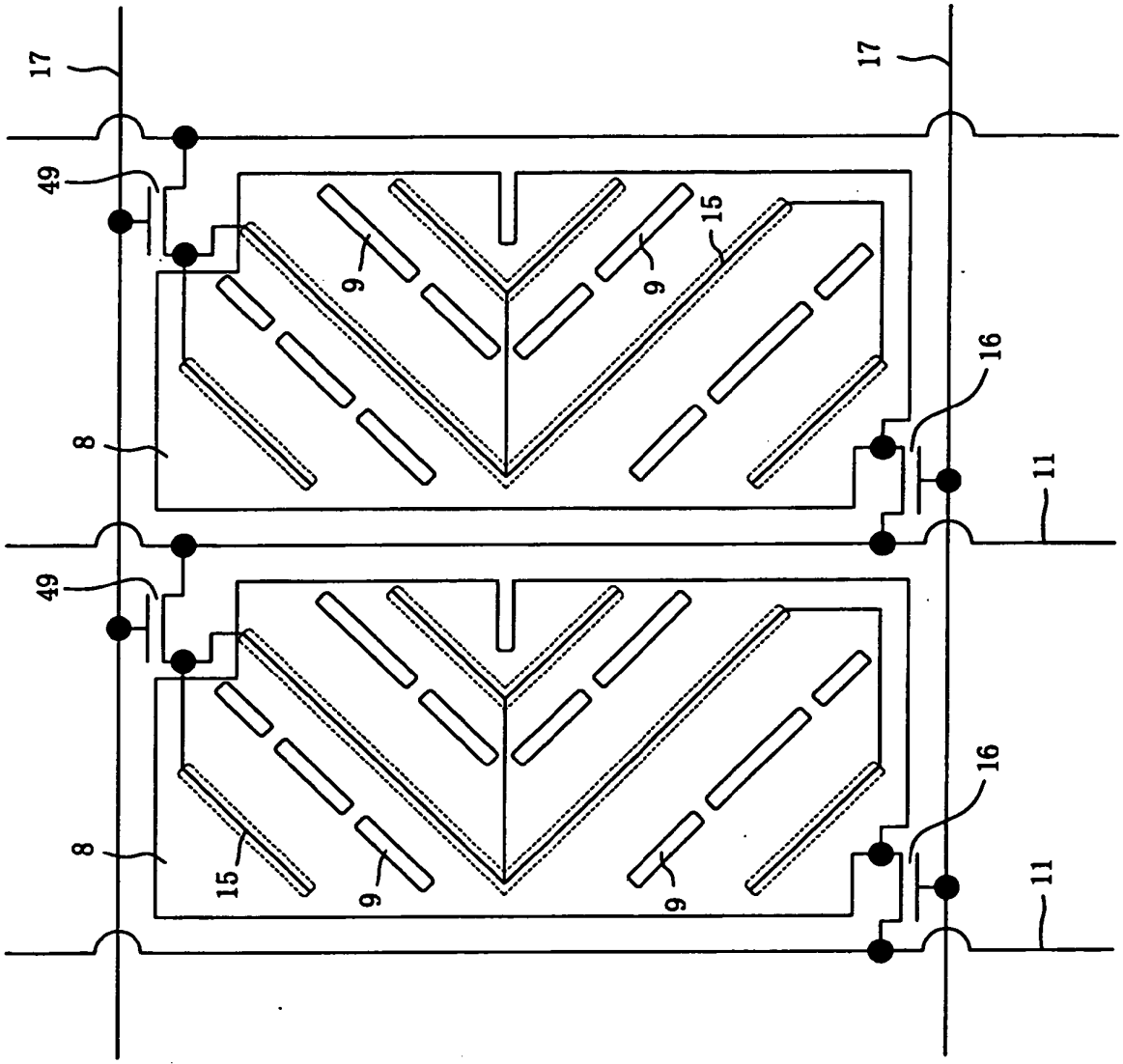


Fig. 35

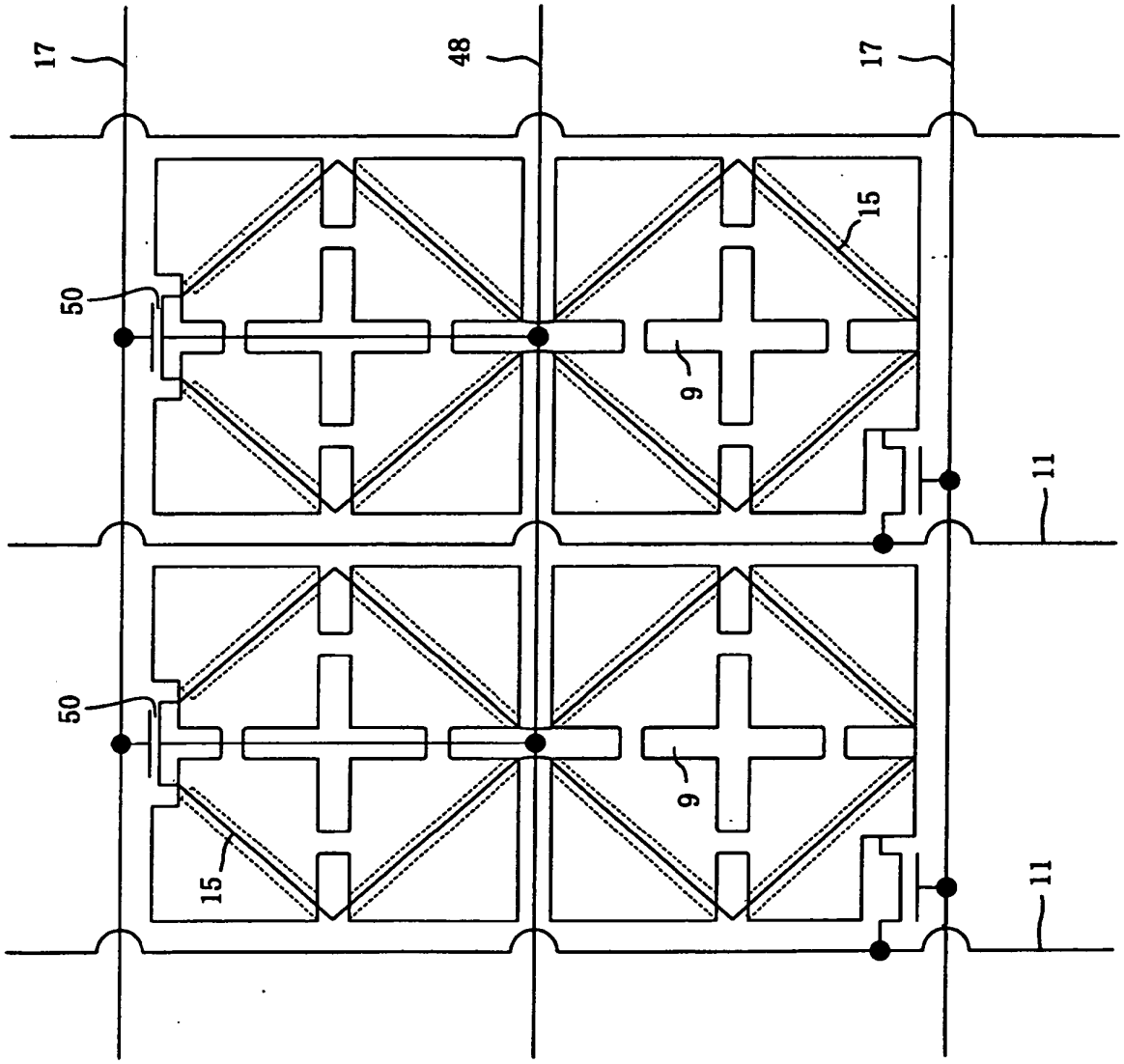


Fig. 36

Fig. 37

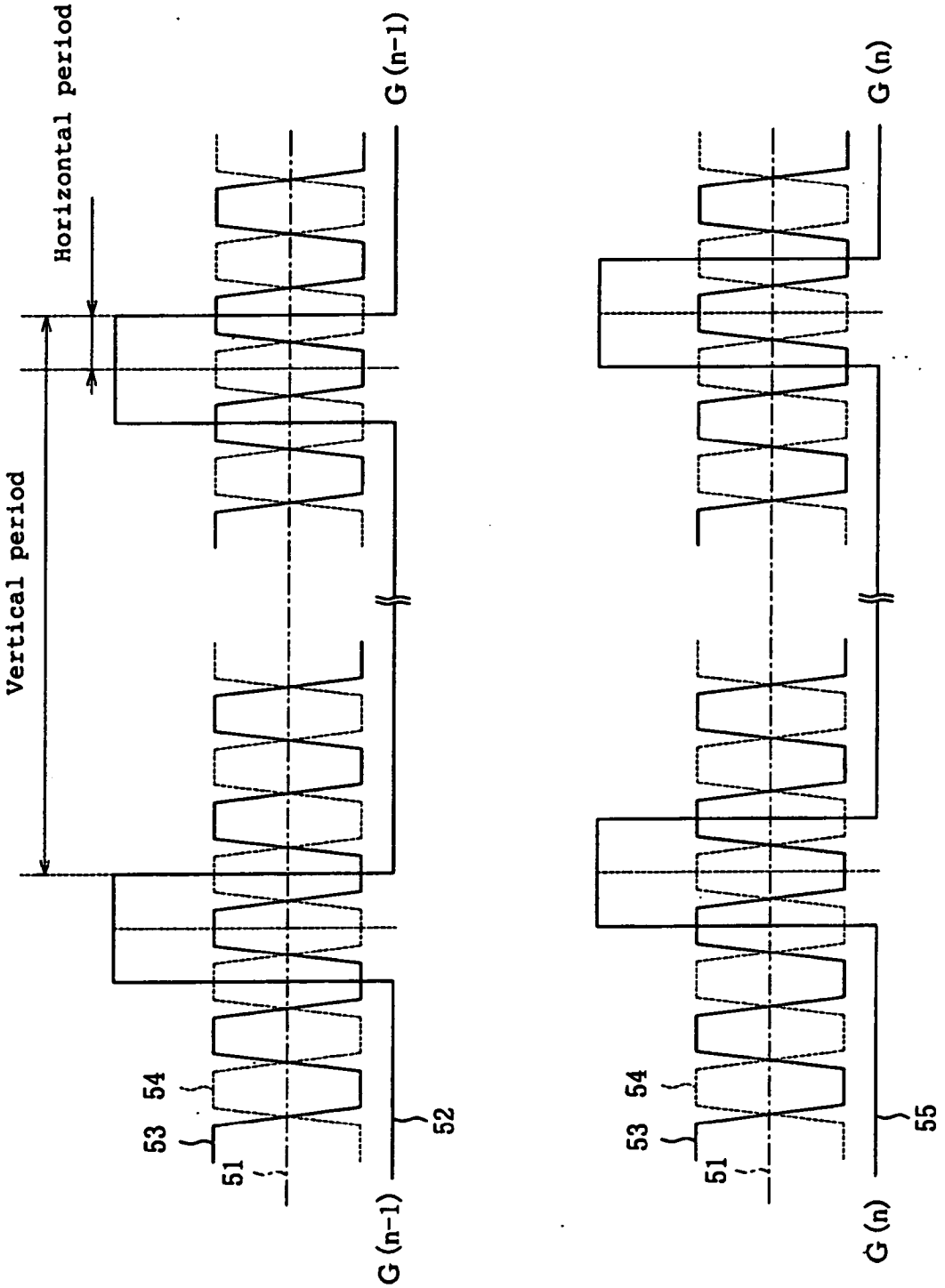


Fig. 38

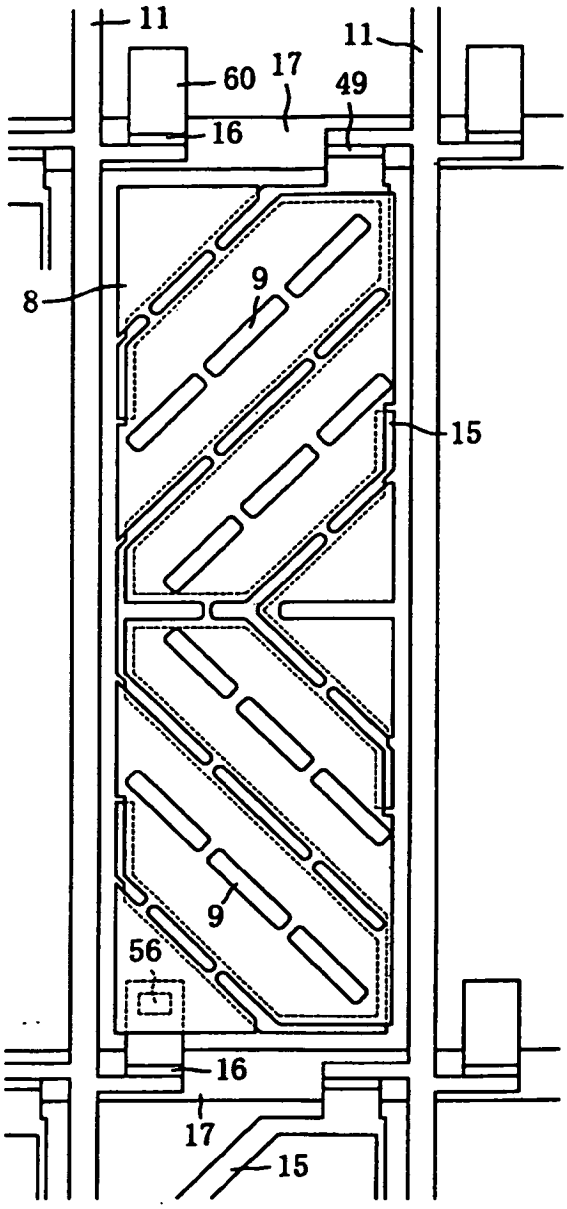
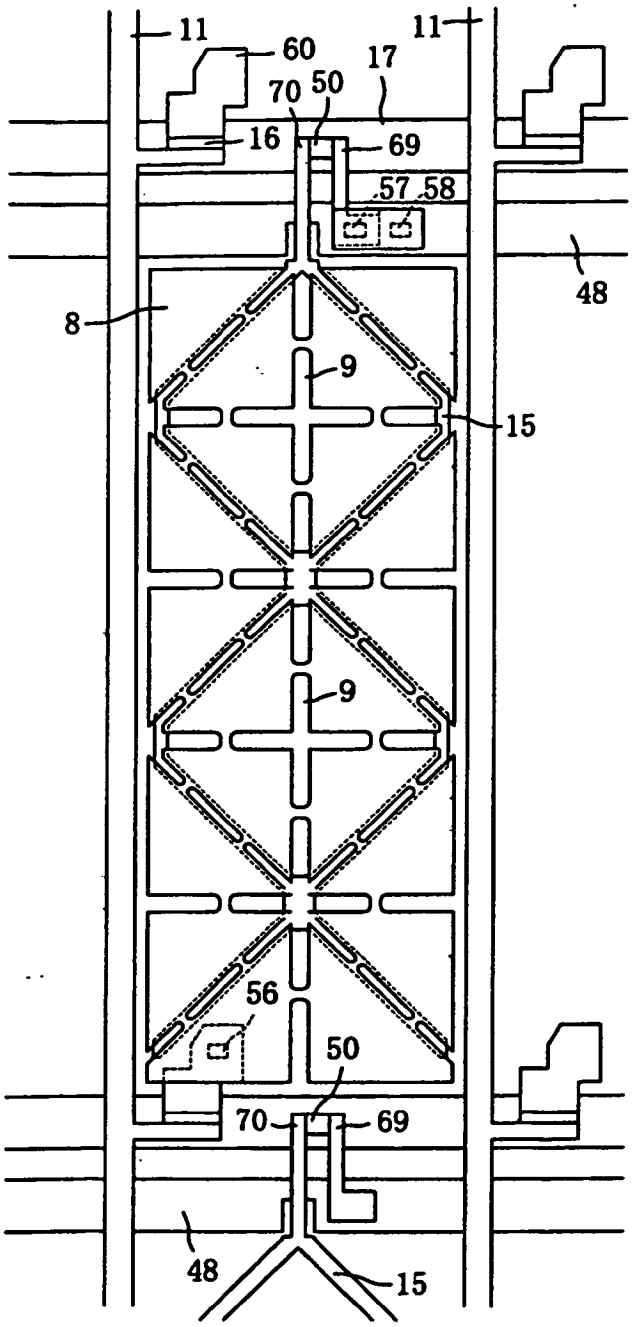


Fig. 39



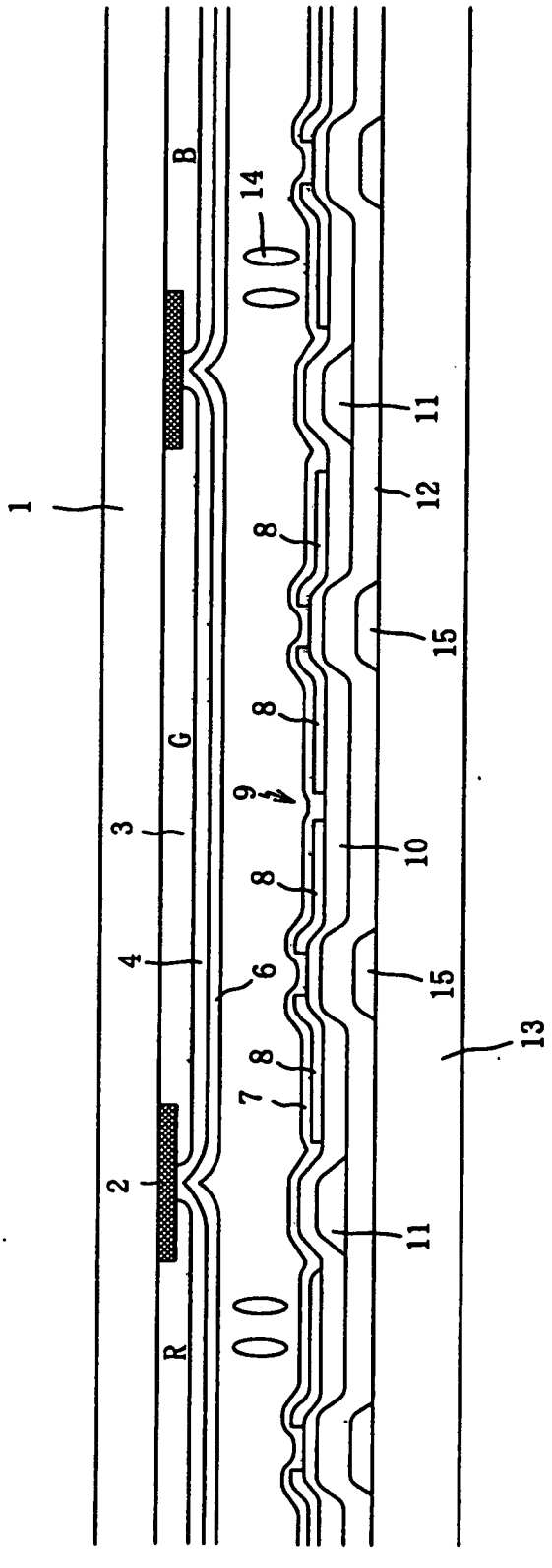


Fig. 40

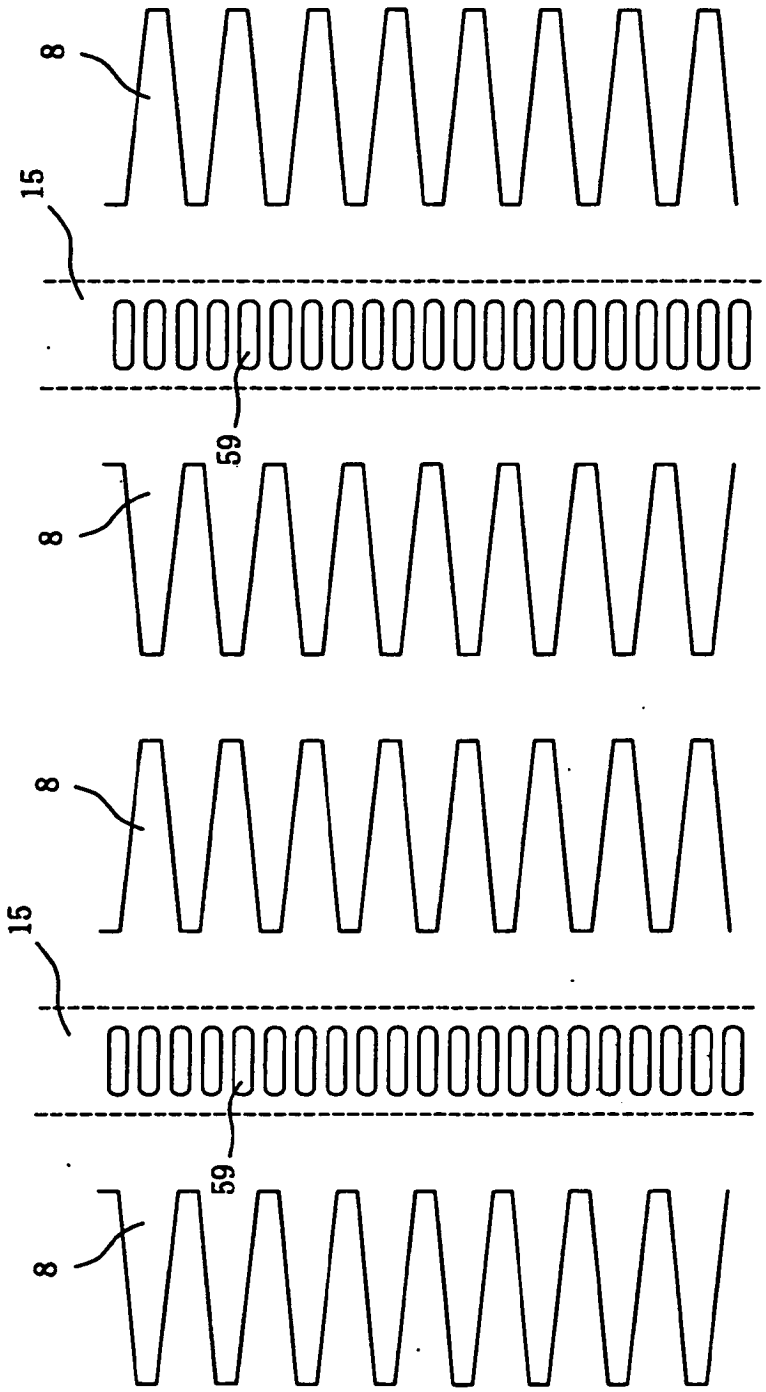


Fig. 41

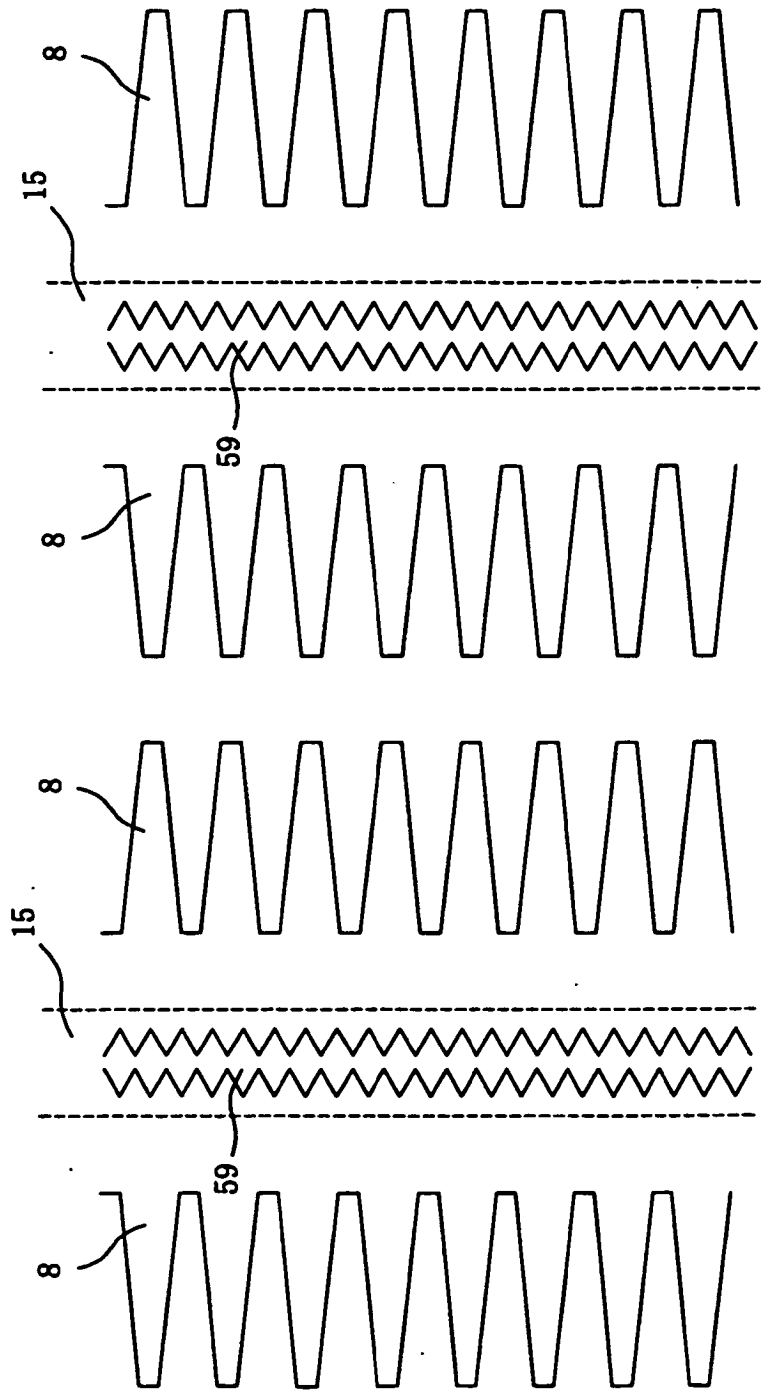


Fig. 42

Fig. 43

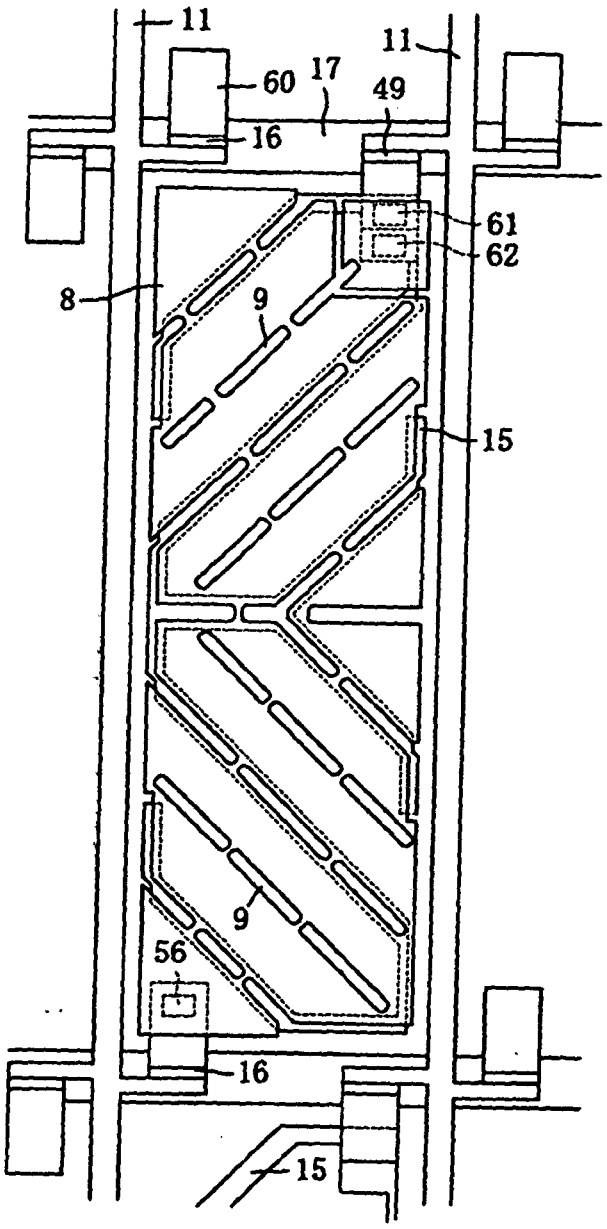


Fig. 44

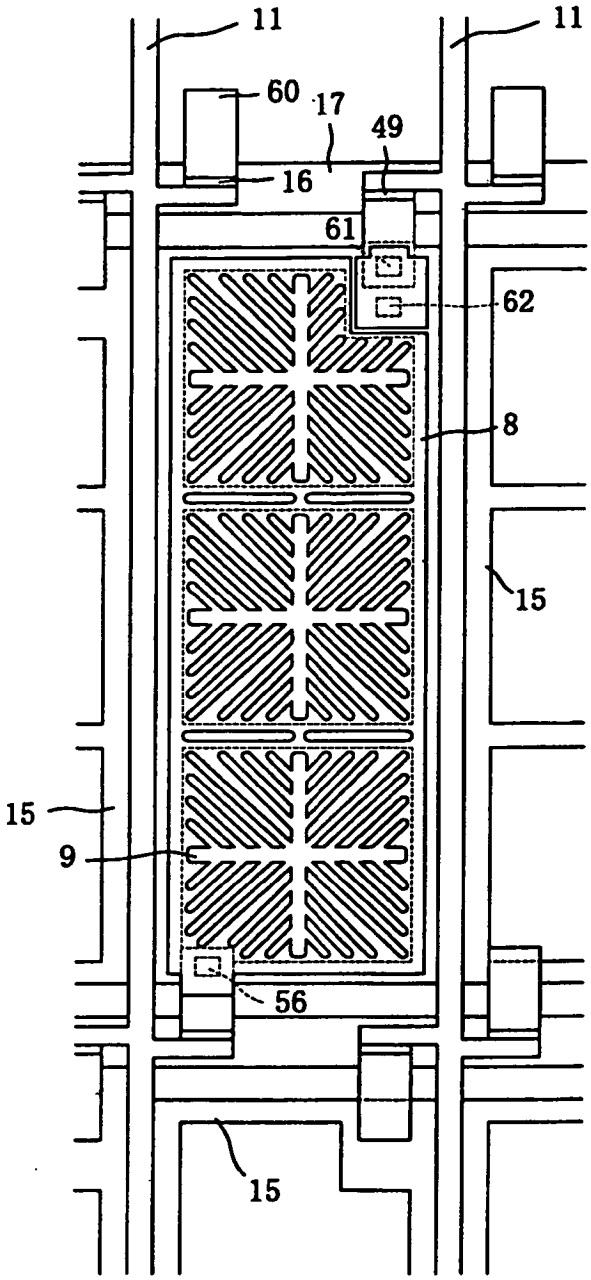


Fig. 45

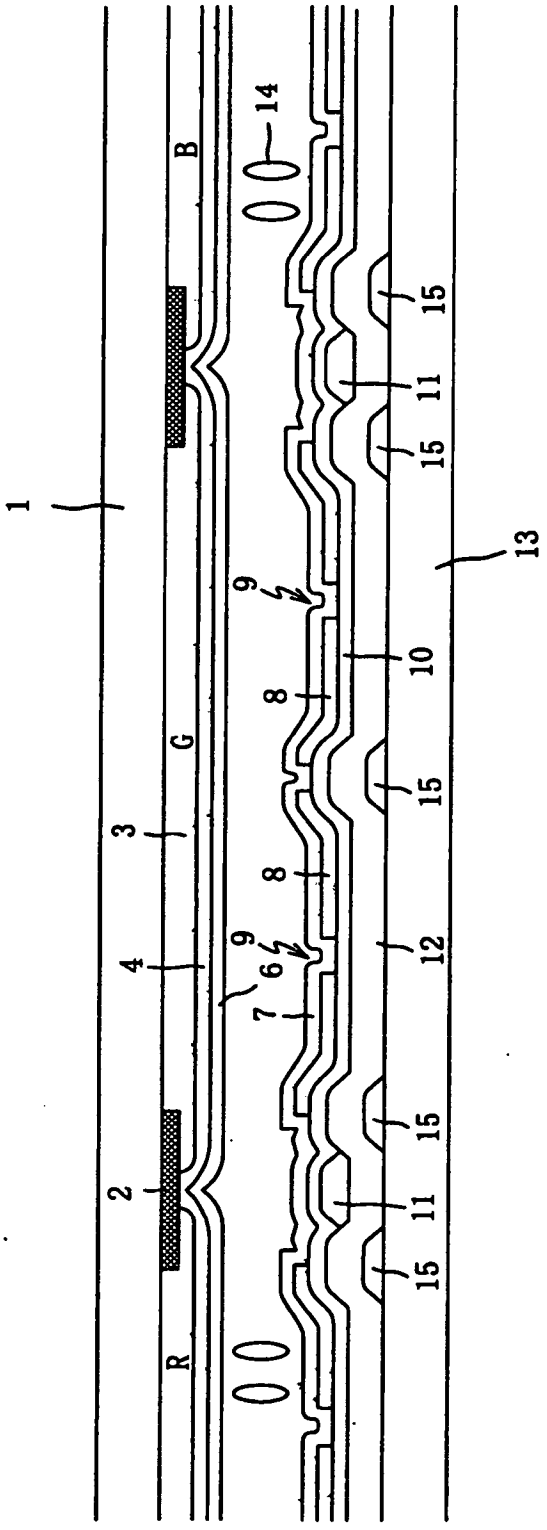


Fig. 46

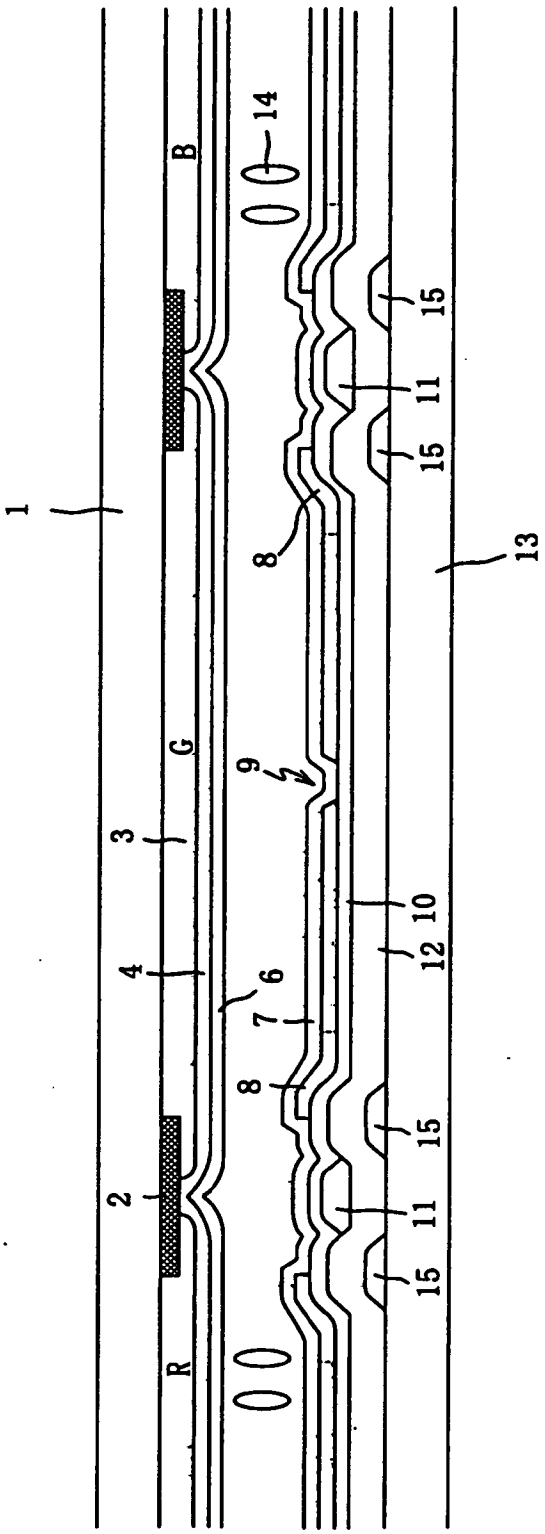


Fig. 47

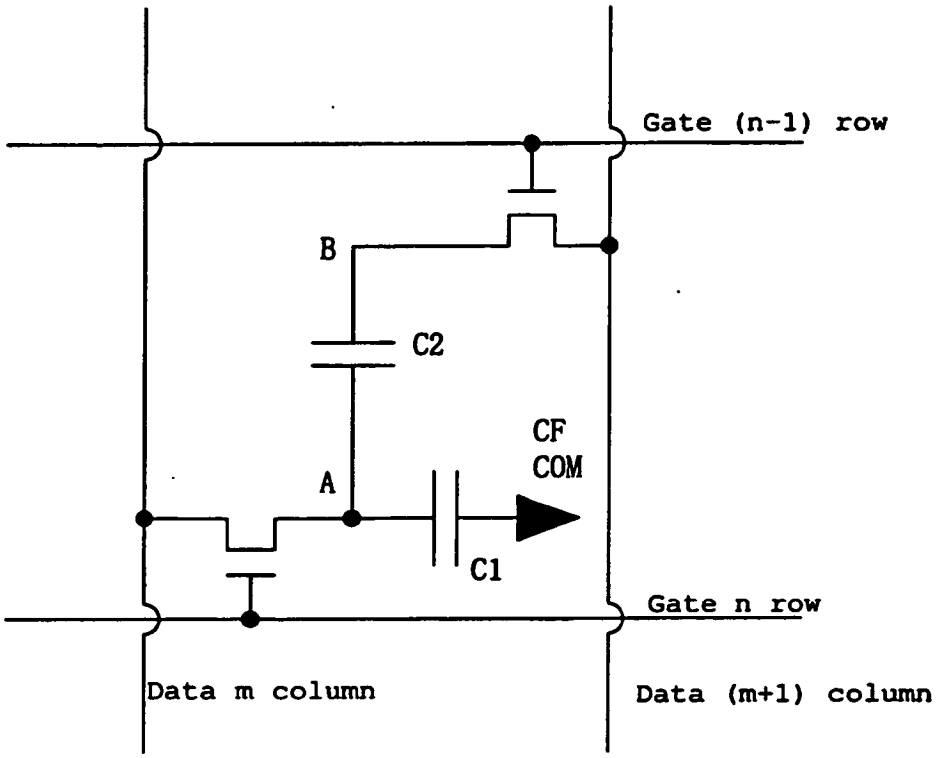


Fig. 48

A	B
+7V → -7V	-7V → -21V
-7V → +7V	+7V → +21V

Fig. 49

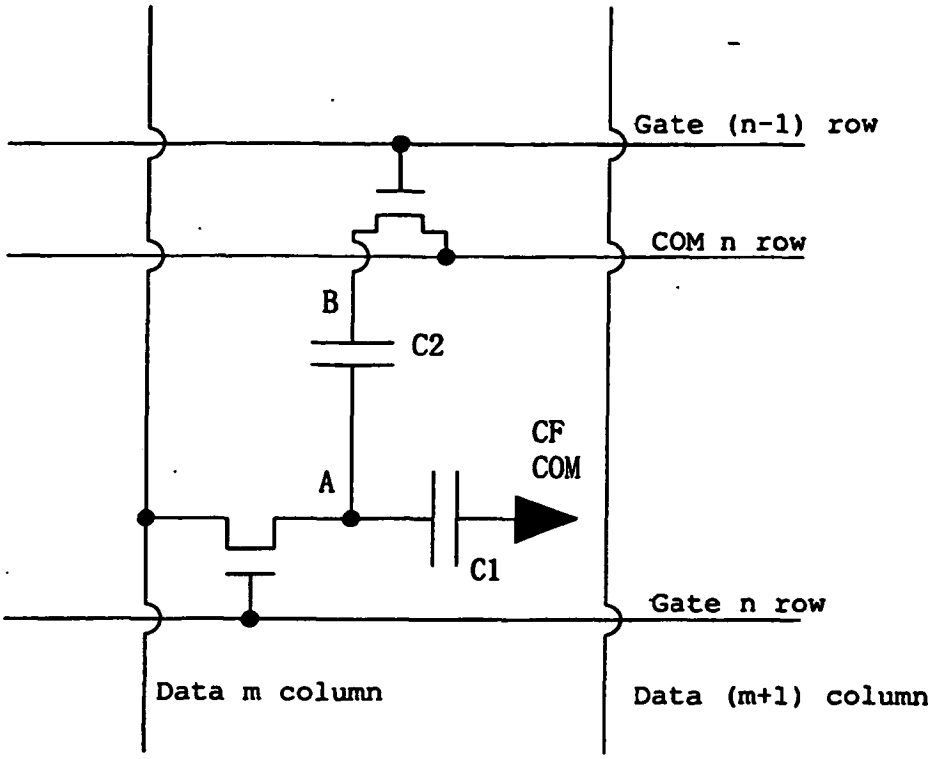


Fig. 50

A	B
+7V ↓ -7V	0V ↓ -14V
-7V ↓ +7V	0V ↓ +14V

Fig. 51

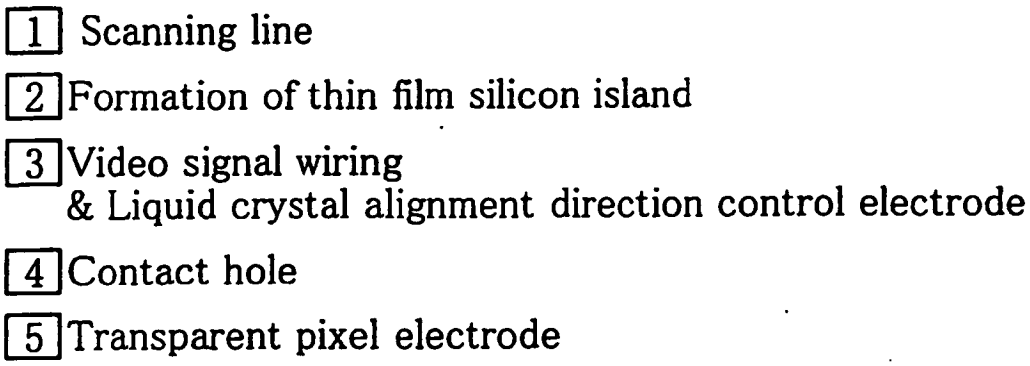

1 Scanning line
2 Formation of thin film silicon island
3 Video signal wiring
& Liquid crystal alignment direction control electrode
4 Contact hole
5 Transparent pixel electrode

Fig. 52

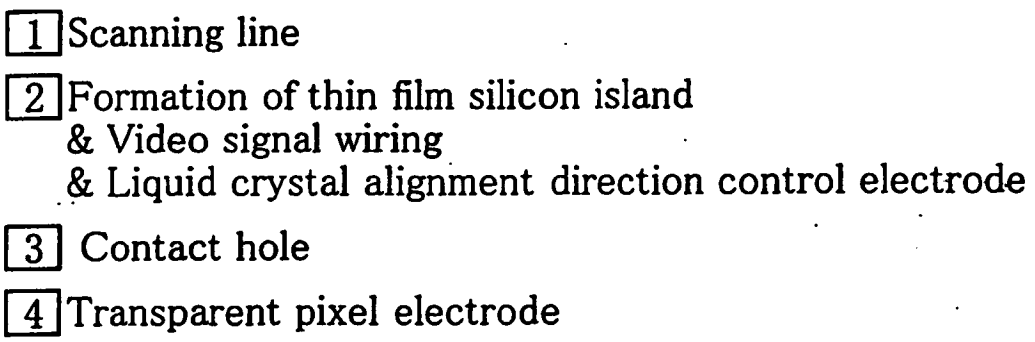

1 Scanning line
2 Formation of thin film silicon island
& Video signal wiring
& Liquid crystal alignment direction control electrode
3 Contact hole
4 Transparent pixel electrode

Fig. 53

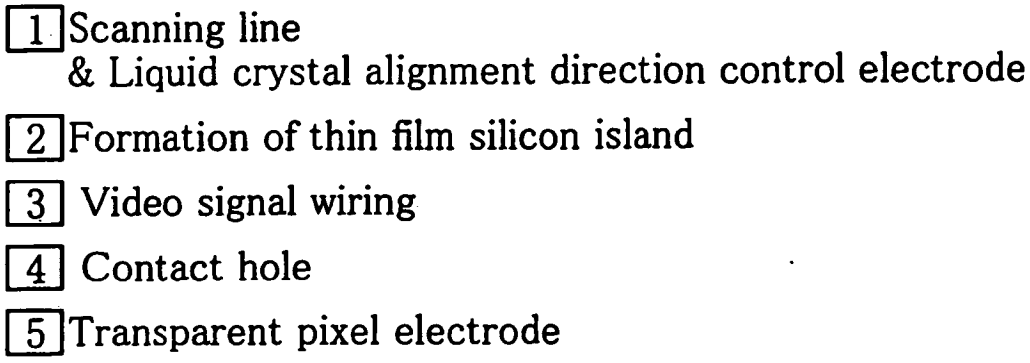

1 Scanning line
& Liquid crystal alignment direction control electrode
2 Formation of thin film silicon island
3 Video signal wiring
4 Contact hole
5 Transparent pixel electrode

Fig. 54

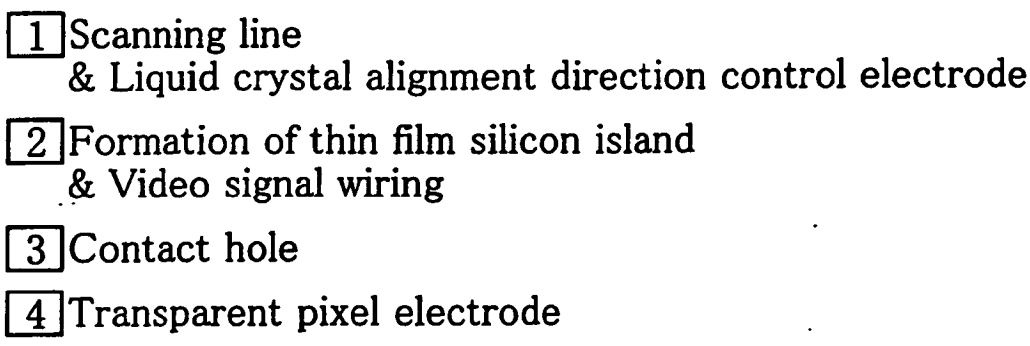

1 Scanning line
& Liquid crystal alignment direction control electrode
2 Formation of thin film silicon island
& Video signal wiring
3 Contact hole
4 Transparent pixel electrode

Fig. 55

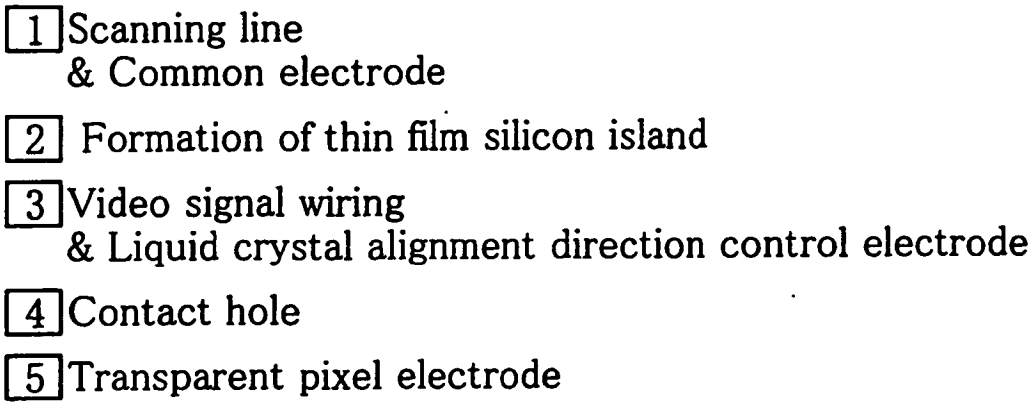

1 Scanning line
& Common electrode
2 Formation of thin film silicon island
3 Video signal wiring
& Liquid crystal alignment direction control electrode
4 Contact hole
5 Transparent pixel electrode

Fig. 56

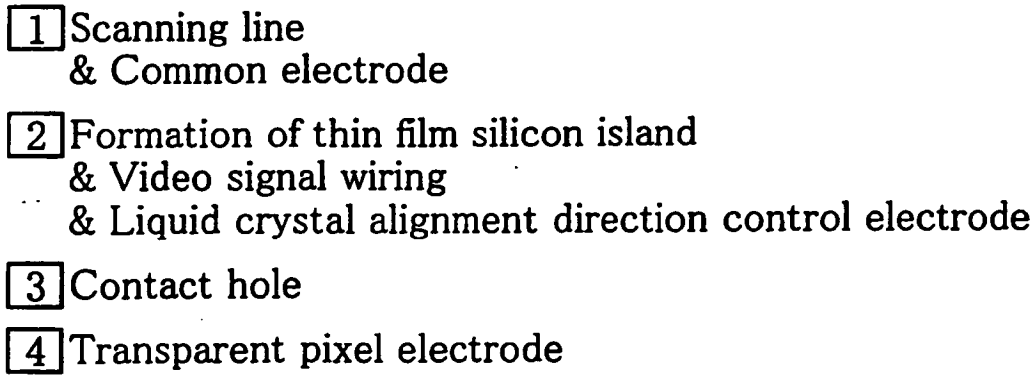

1 Scanning line
& Common electrode
2 Formation of thin film silicon island
& Video signal wiring
& Liquid crystal alignment direction control electrode
3 Contact hole
4 Transparent pixel electrode

Fig. 57

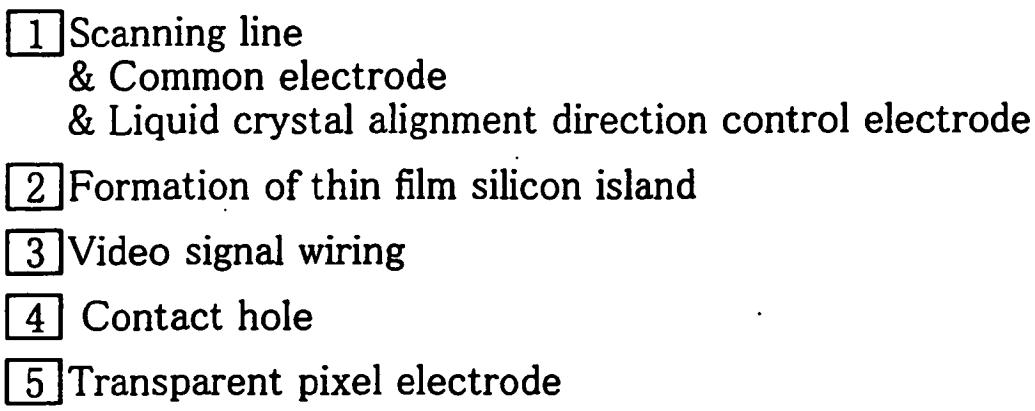

1 Scanning line
& Common electrode
& Liquid crystal alignment direction control electrode
2 Formation of thin film silicon island
3 Video signal wiring
4 Contact hole
5 Transparent pixel electrode

Fig. 58

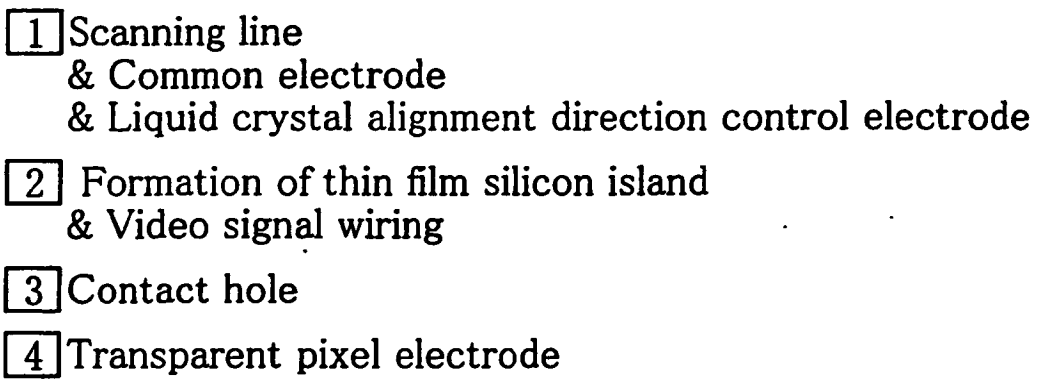

1 Scanning line
& Common electrode
& Liquid crystal alignment direction control electrode
2 Formation of thin film silicon island
& Video signal wiring
3 Contact hole
4 Transparent pixel electrode

Fig. 59

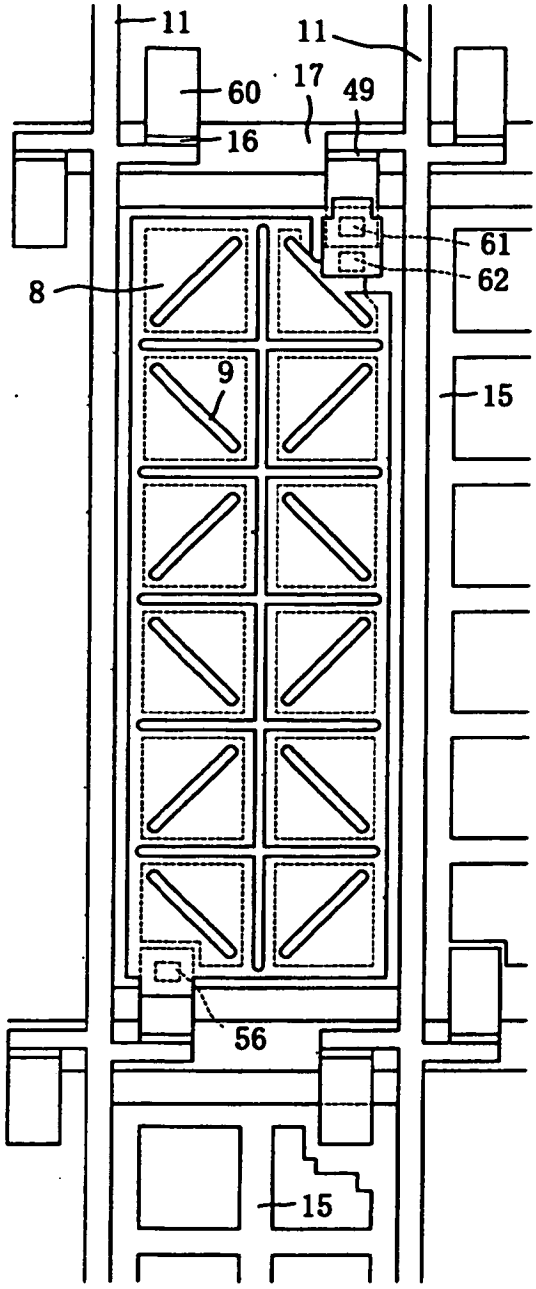


Fig. 60

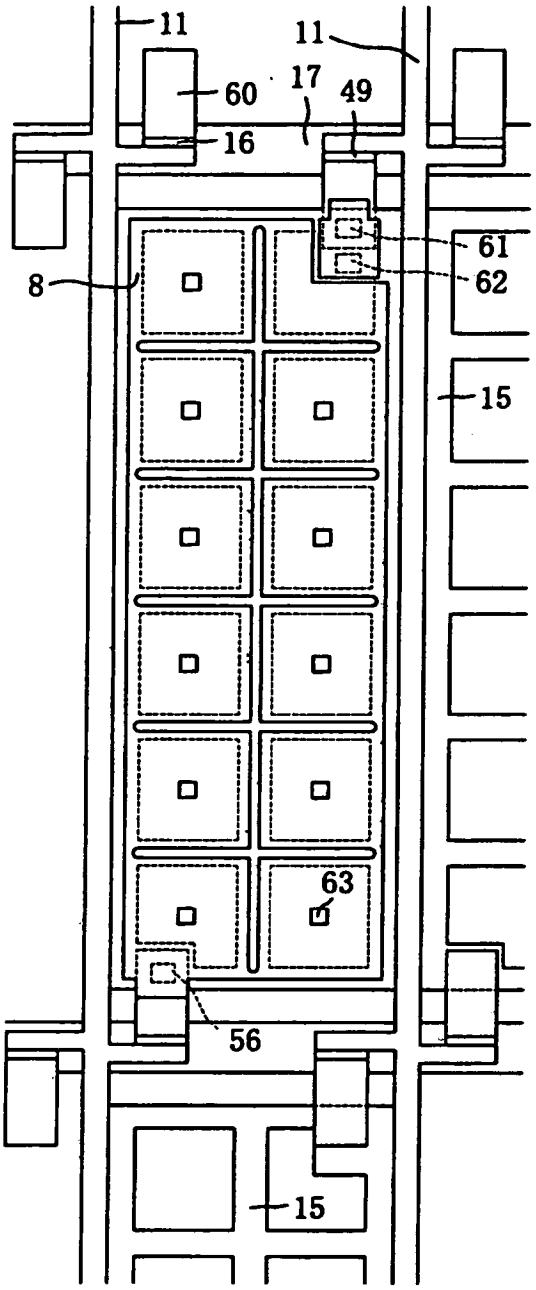
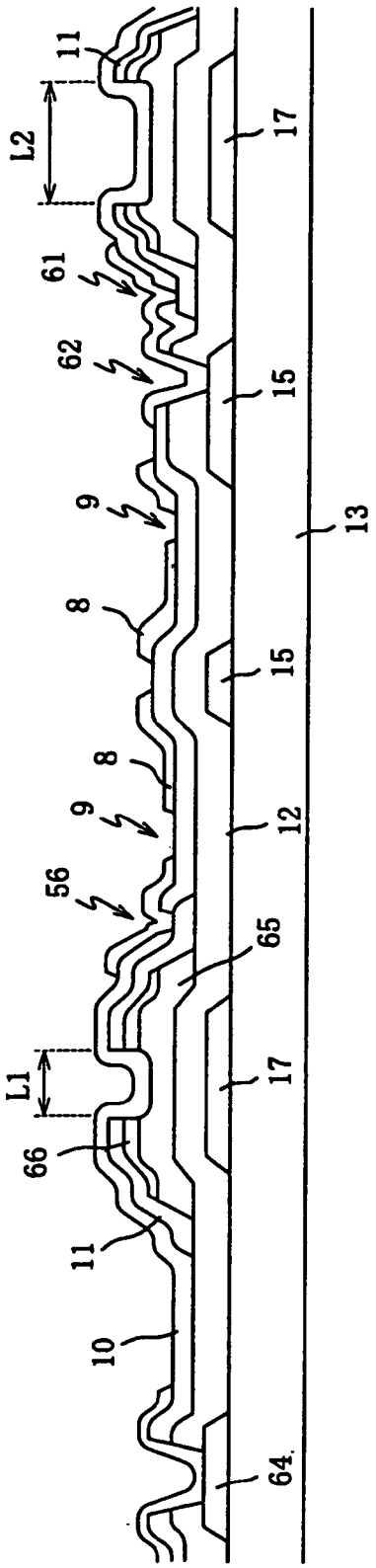


Fig. 61



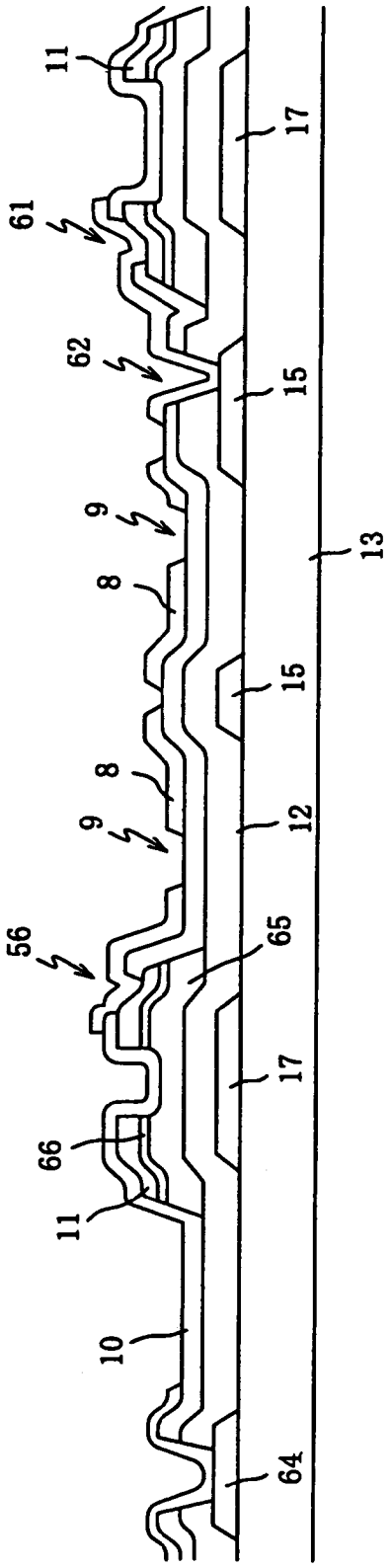


Fig. 62

Fig. 63

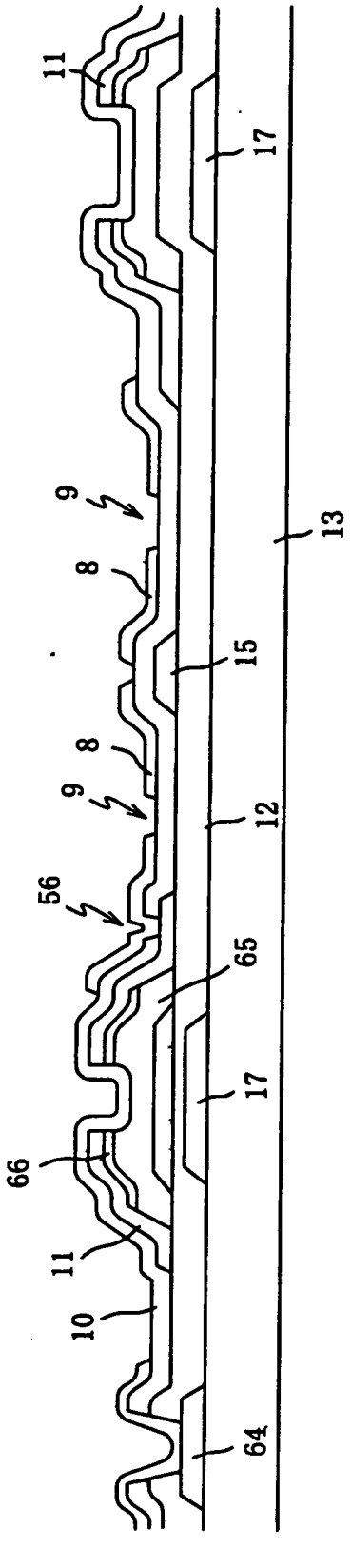


Fig. 64

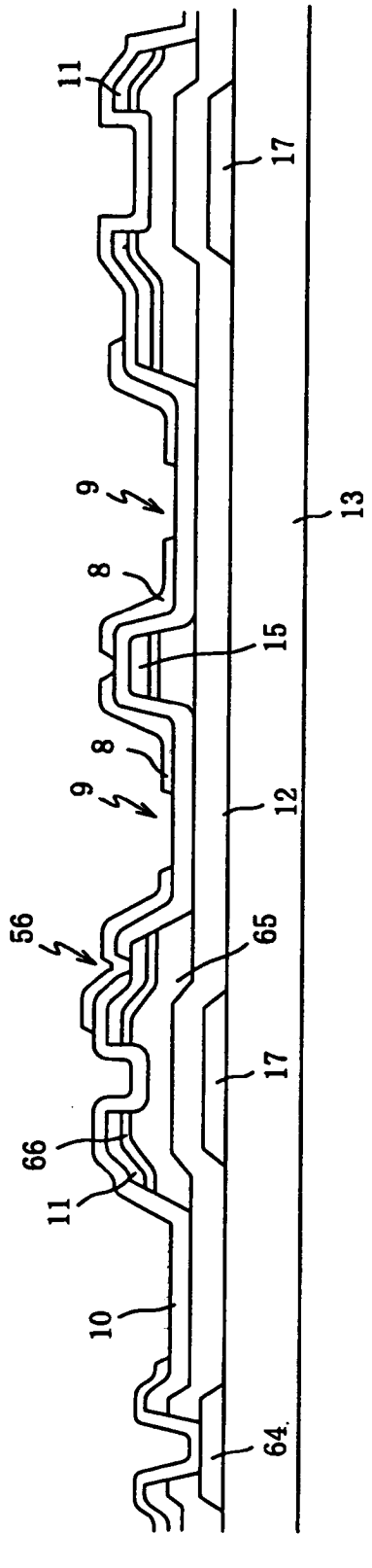


Fig. 65

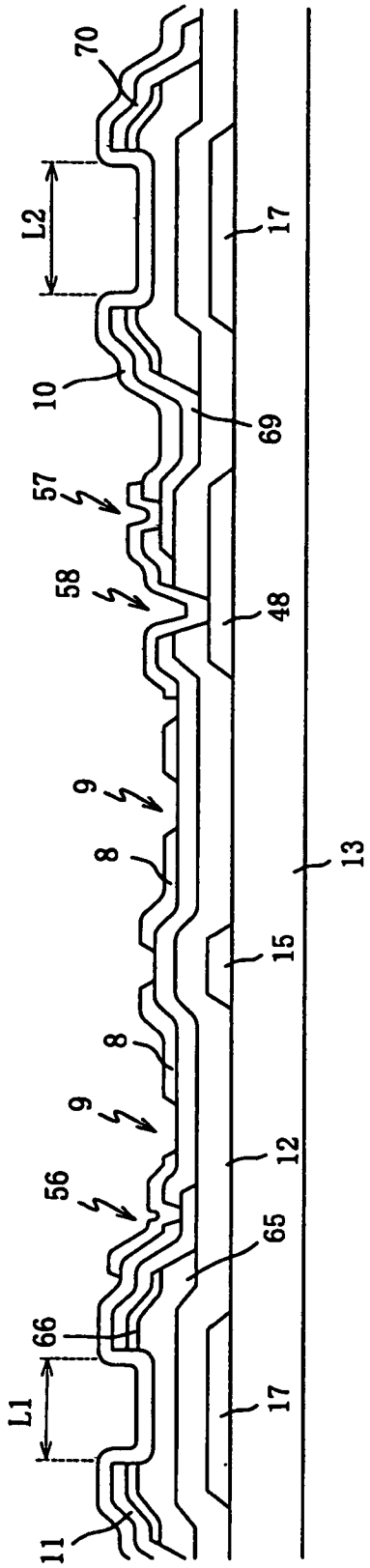


Fig. 66

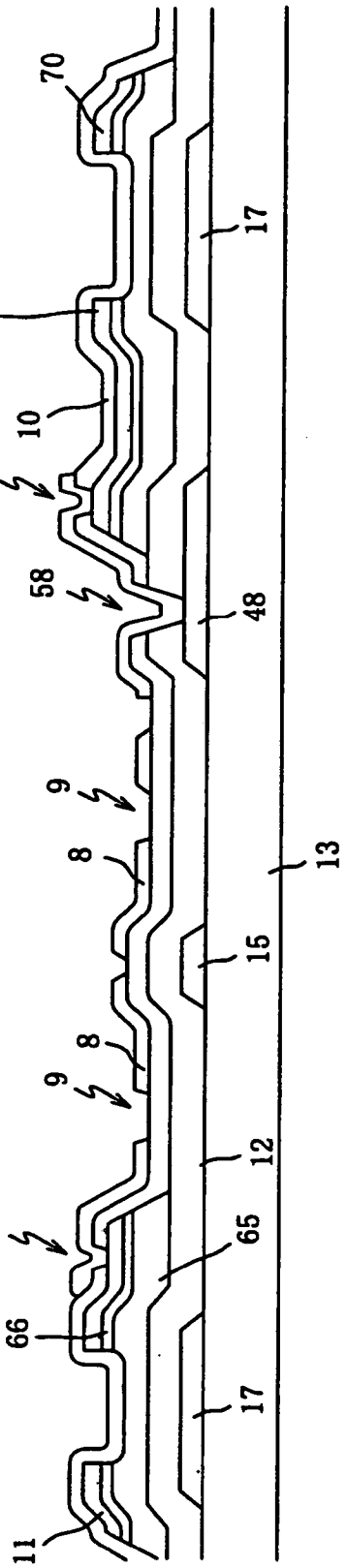


Fig. 67

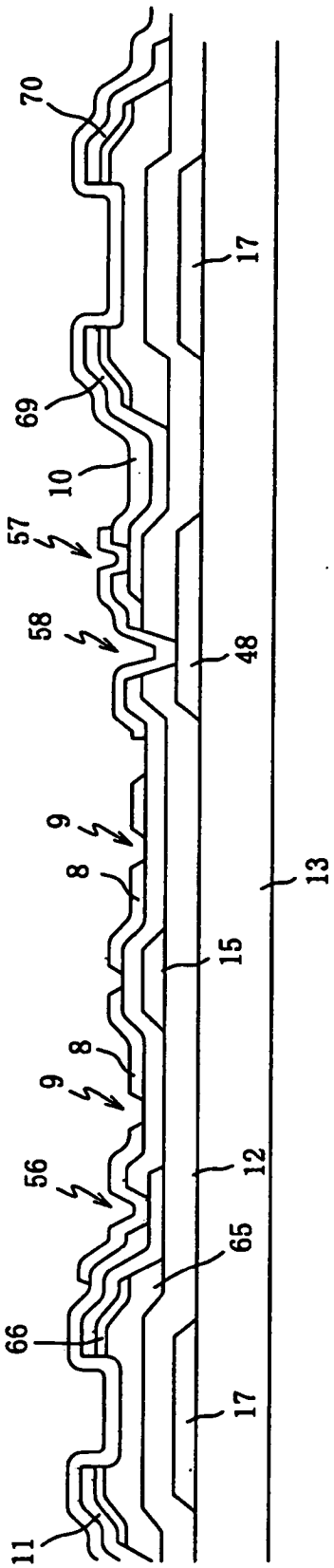
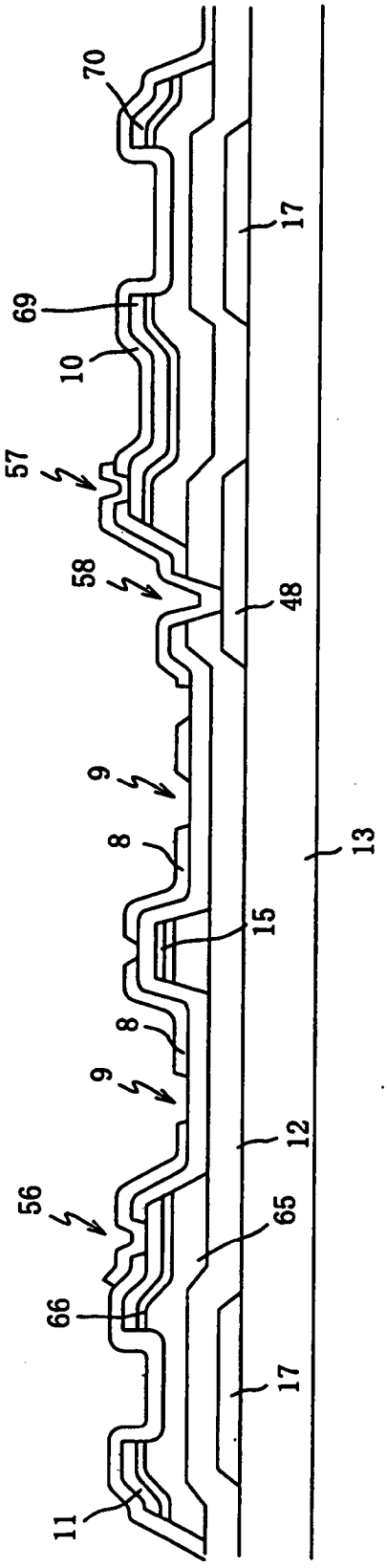


Fig. 68



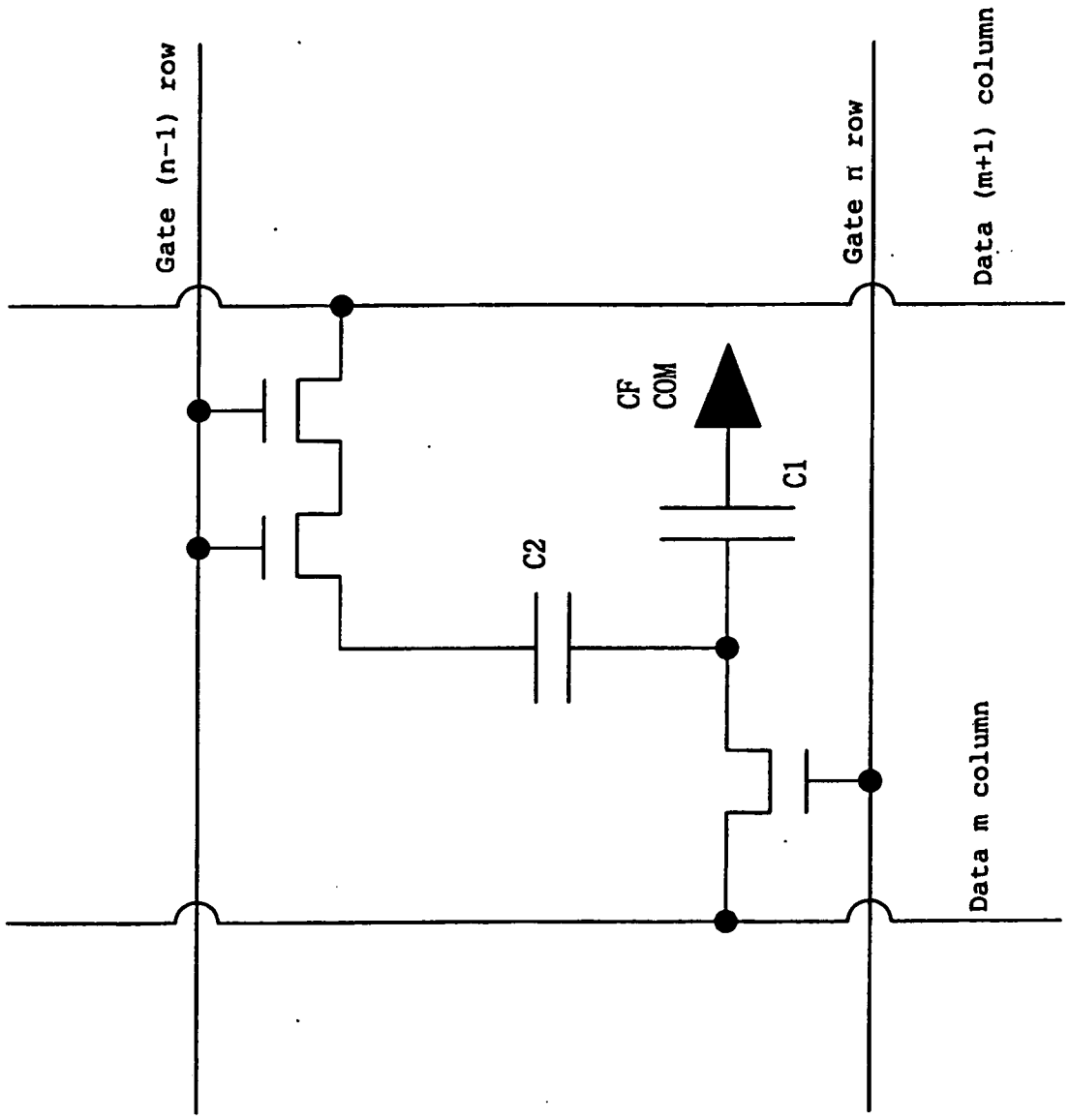


Fig. 69

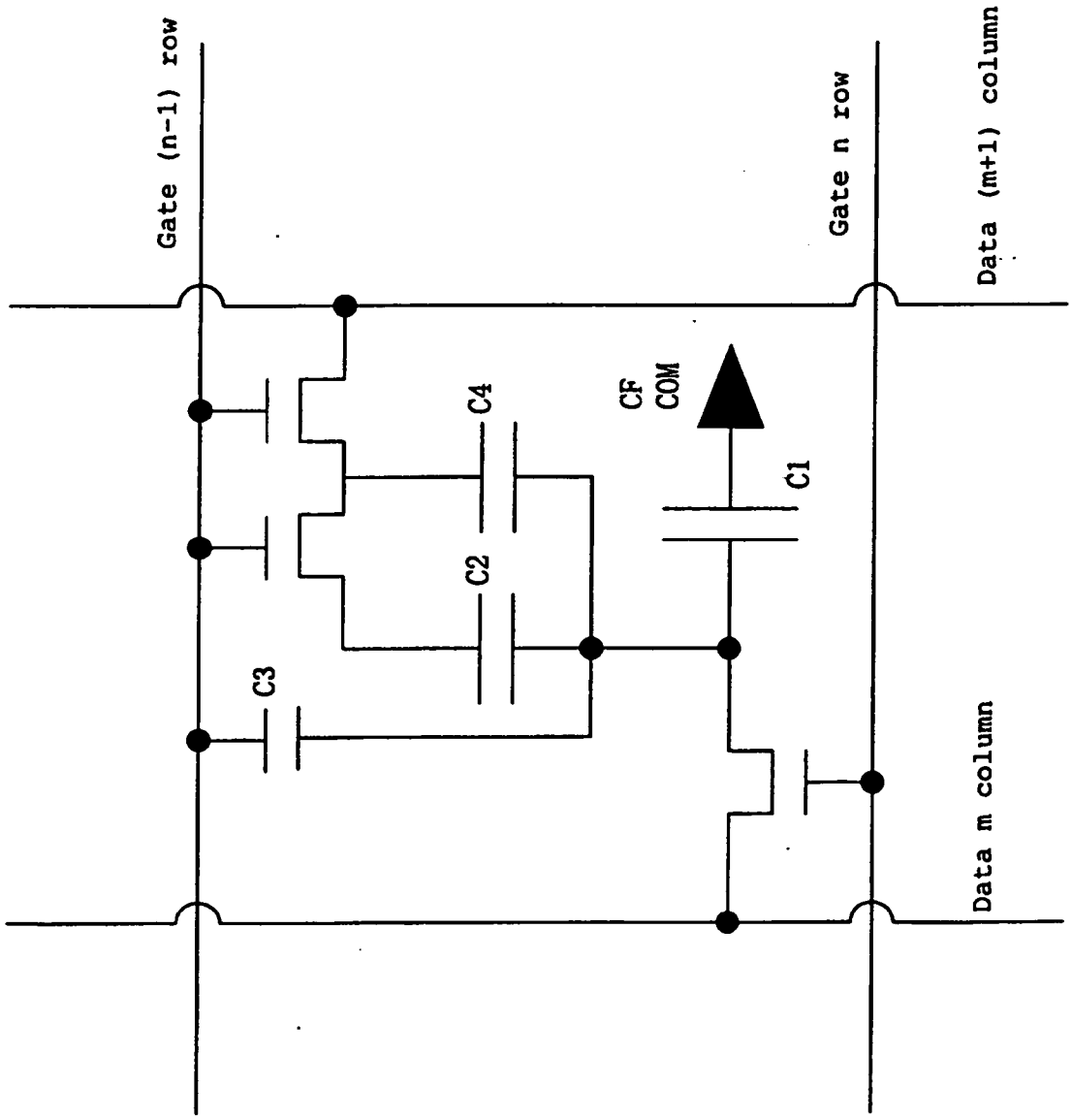

Gate (n-1) row
Gate n row
Data (m+1) column
Data m column
C4
C2
C3
C1
CF
COM

Fig. 70

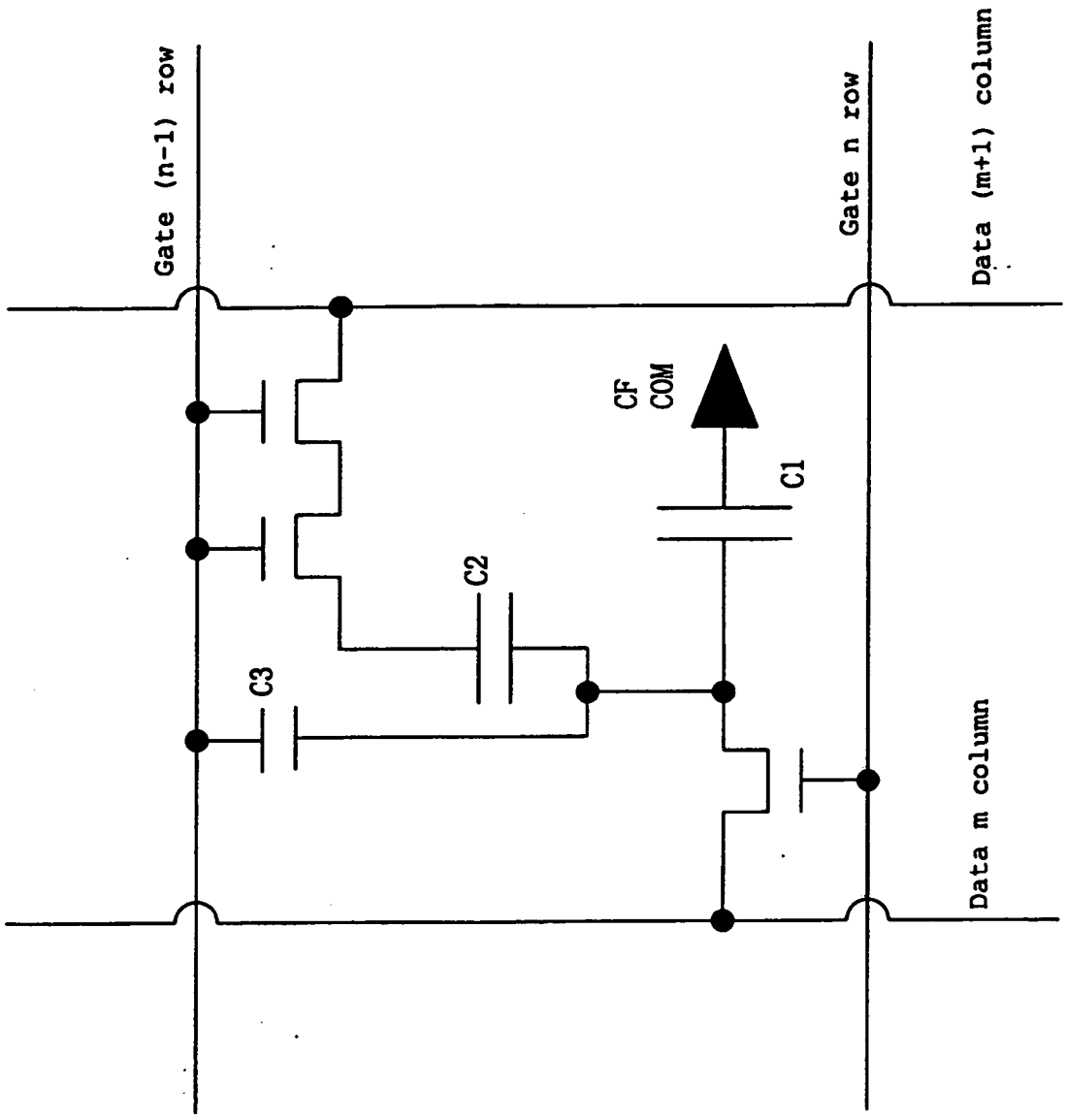

Gate (n-1) row
Gate n row
Data (m+1) column
Data m column
CF
COM
C1
C2
C3

Fig. 71

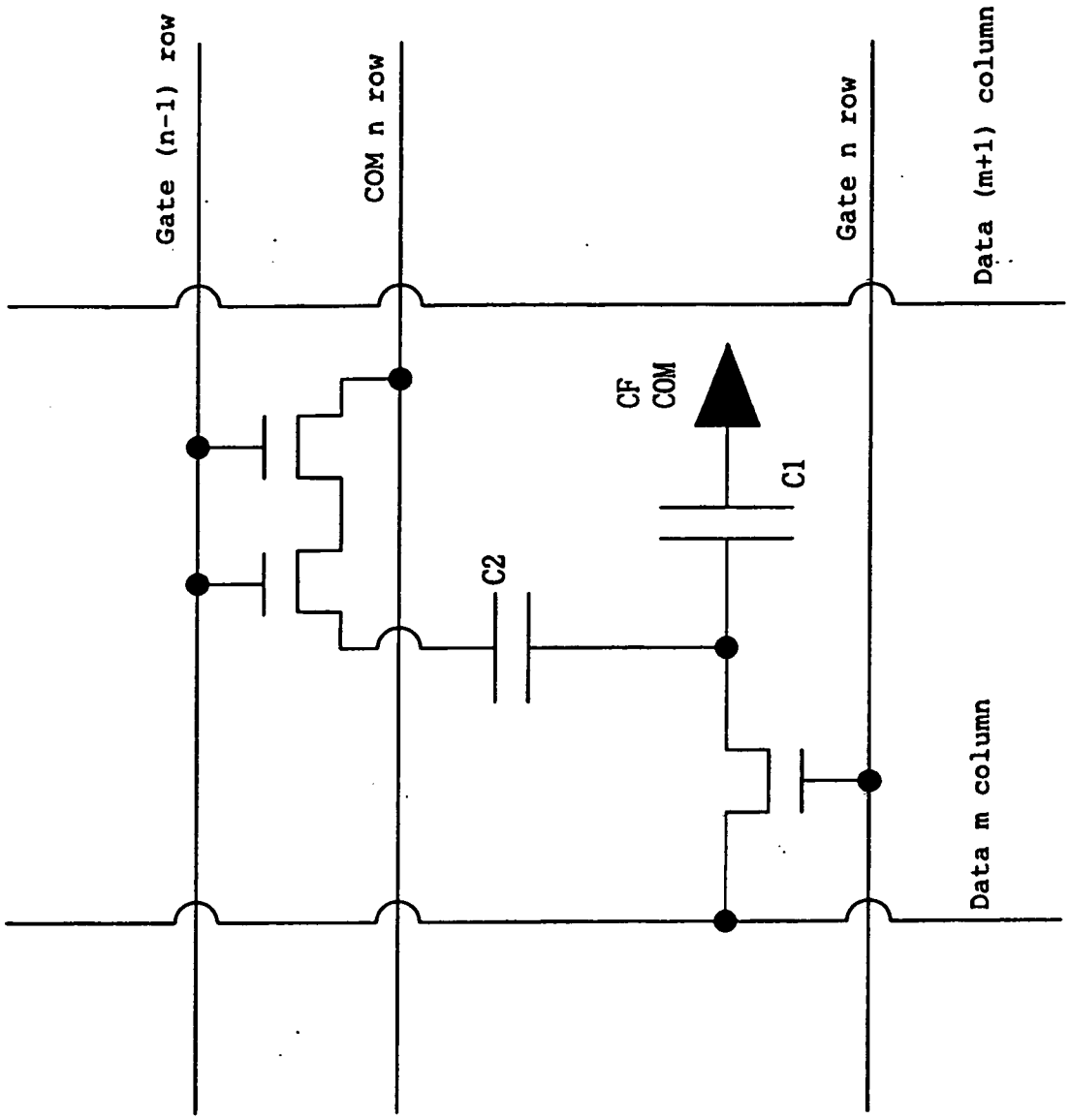

Gate (n-1) row
COM n row
Gate n row
Data (m+1) column
CF COM
C1
C2
Data m column

Fig. 72

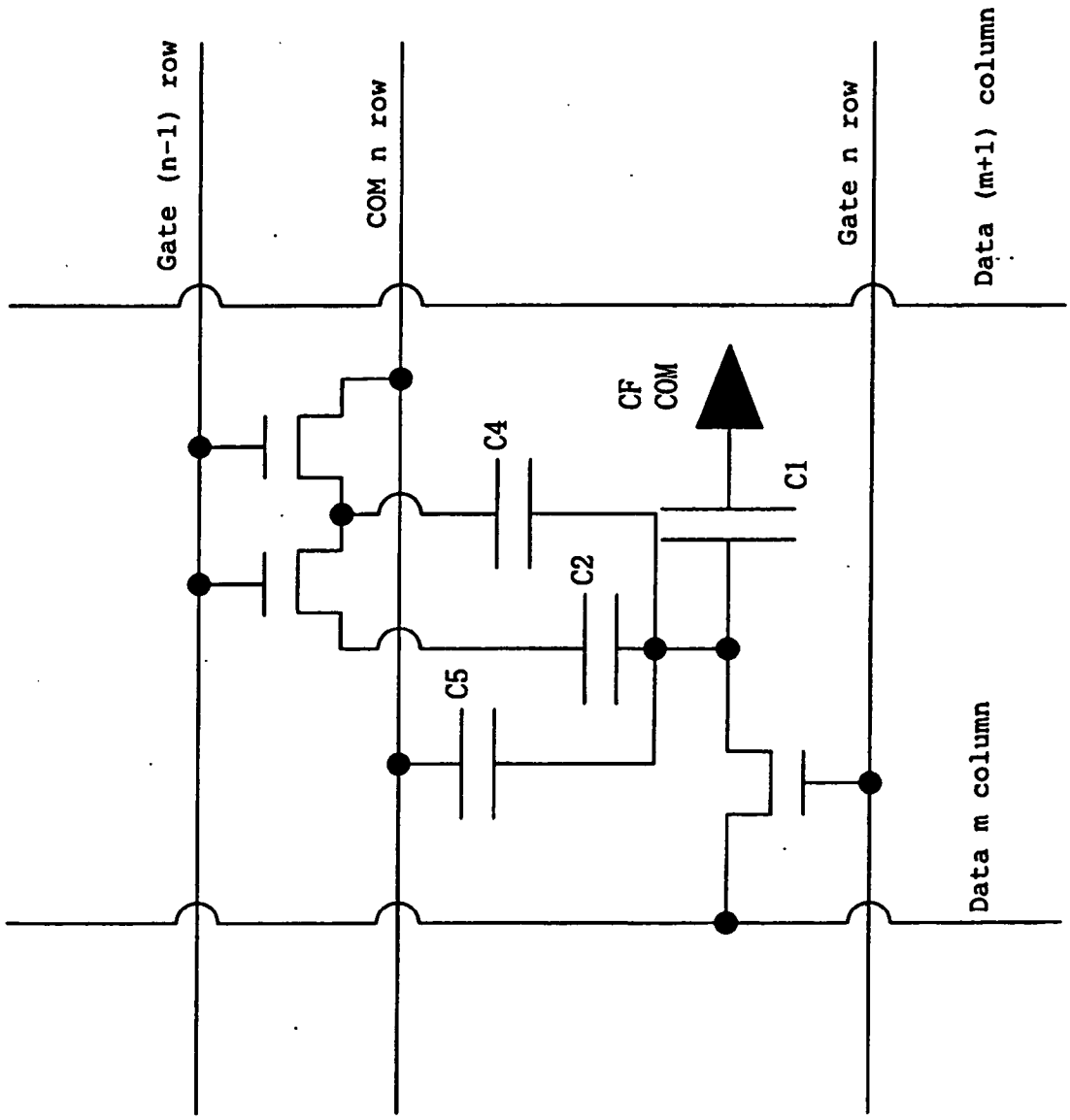

Gate (n-1) row
COM n row
Gate n row
Data (m+1) column
CF
COM
C4
C1
C2
C5
Data m column

Fig. 73

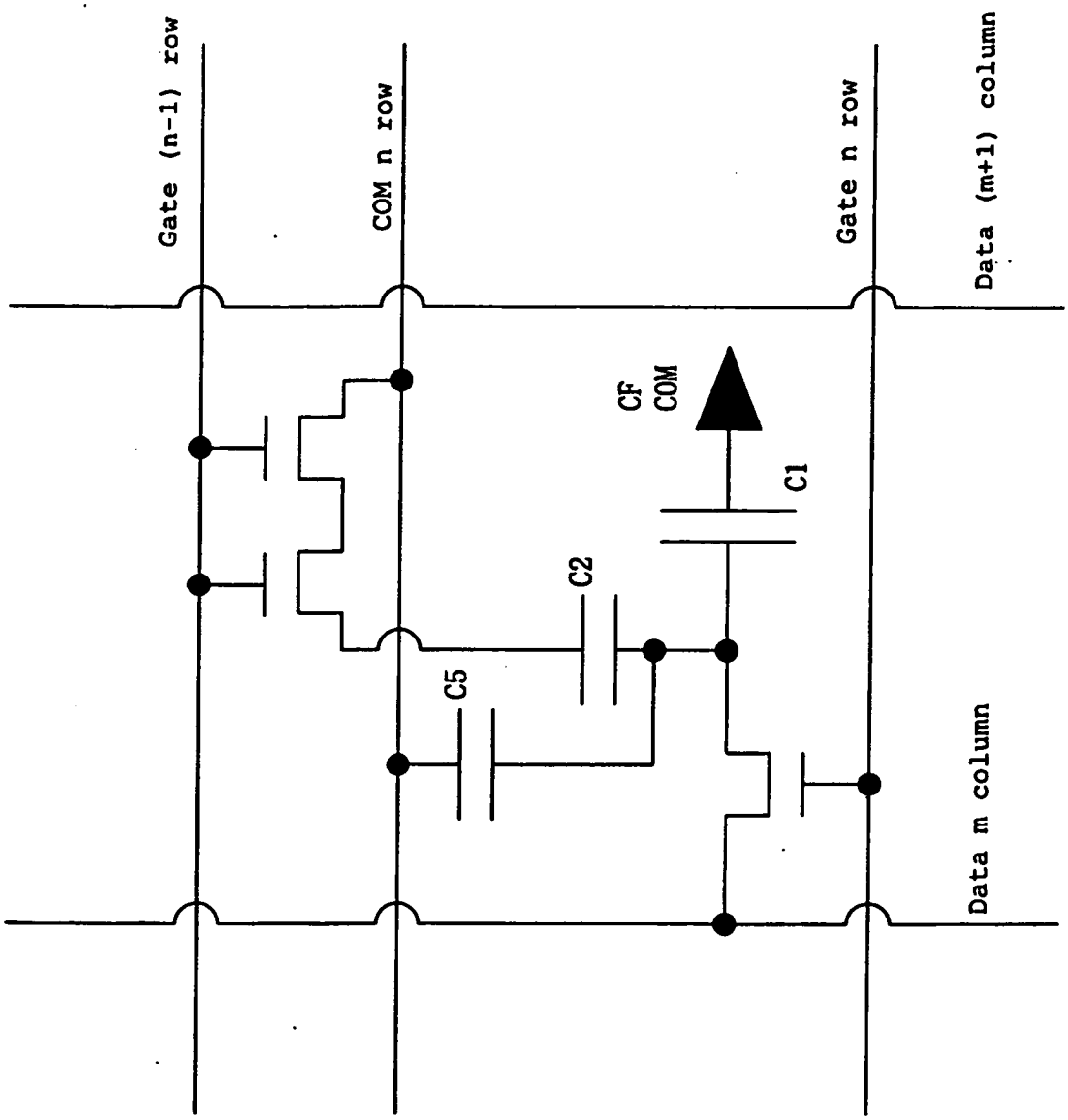

Gate (n-1) row
COM n row
Gate n row
Data (m+1) column
CF
COM
C1
C2
C5
Data m column

Fig. 74

Fig. 75

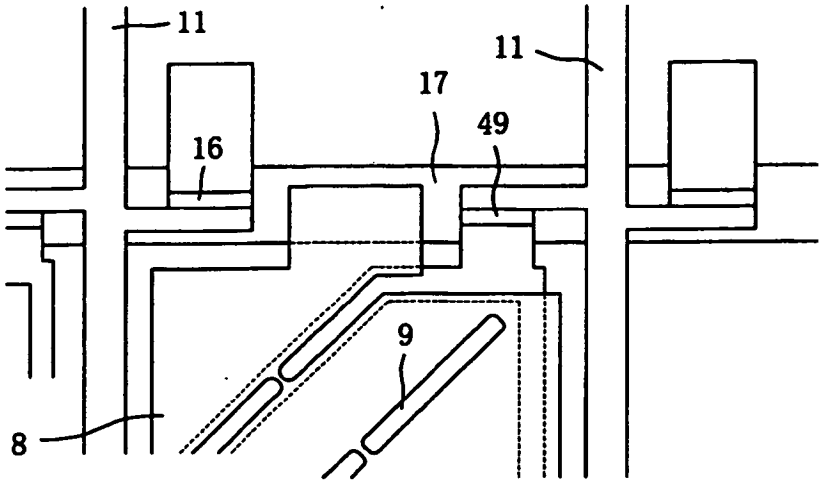


Fig. 76

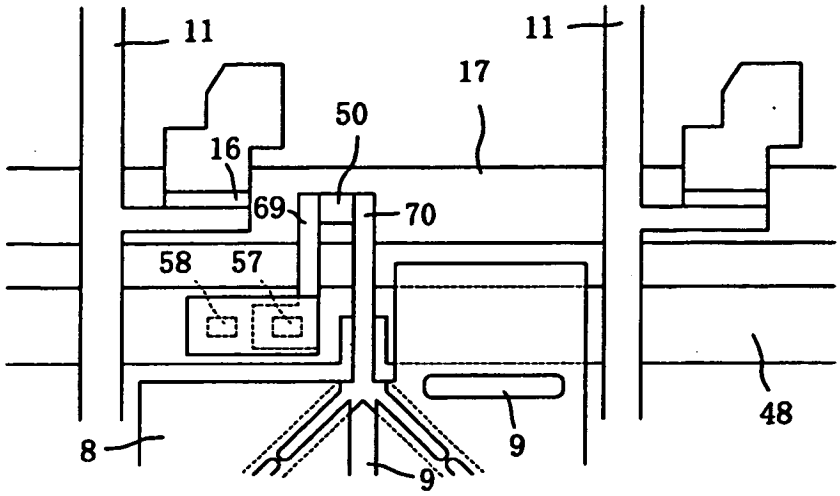


Fig. 77

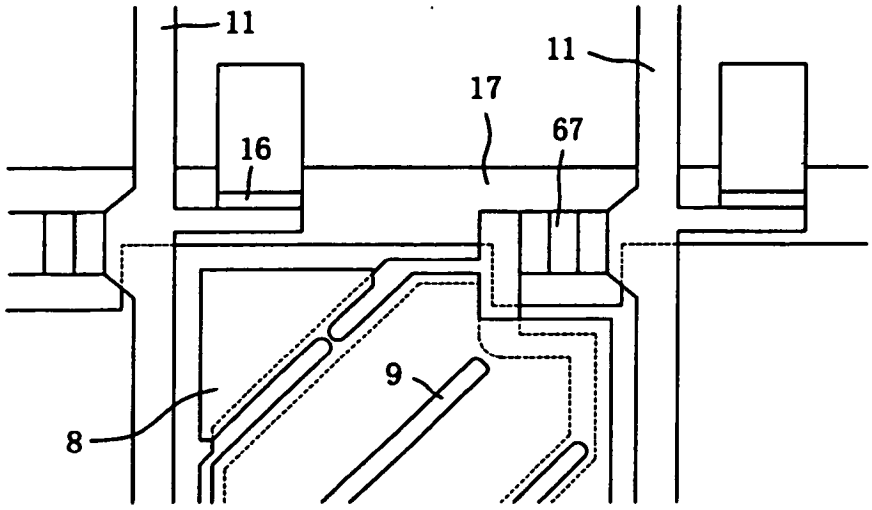


Fig. 78

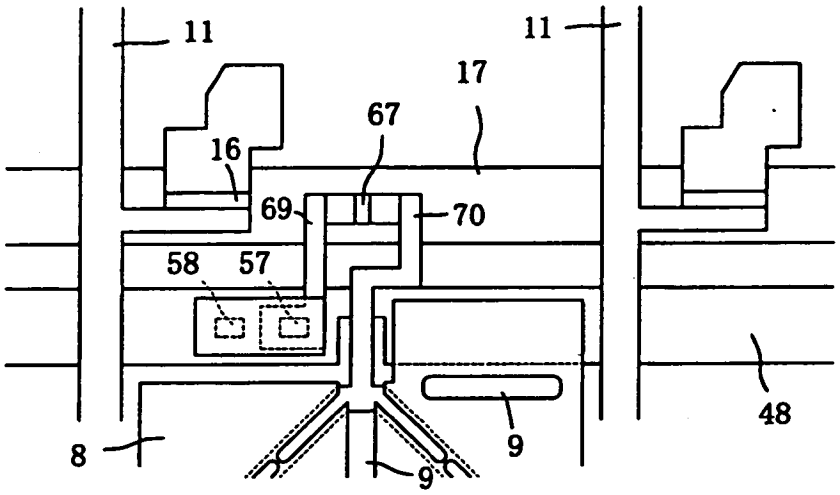


Fig. 79

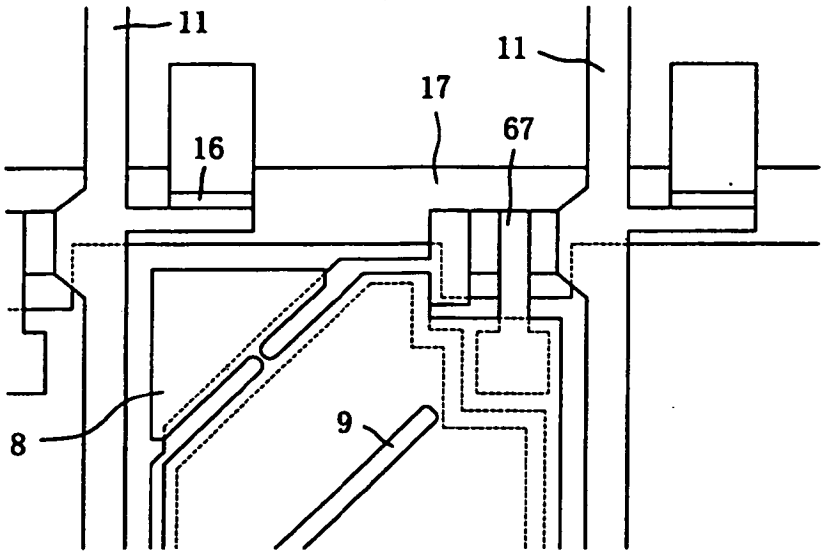


Fig. 80

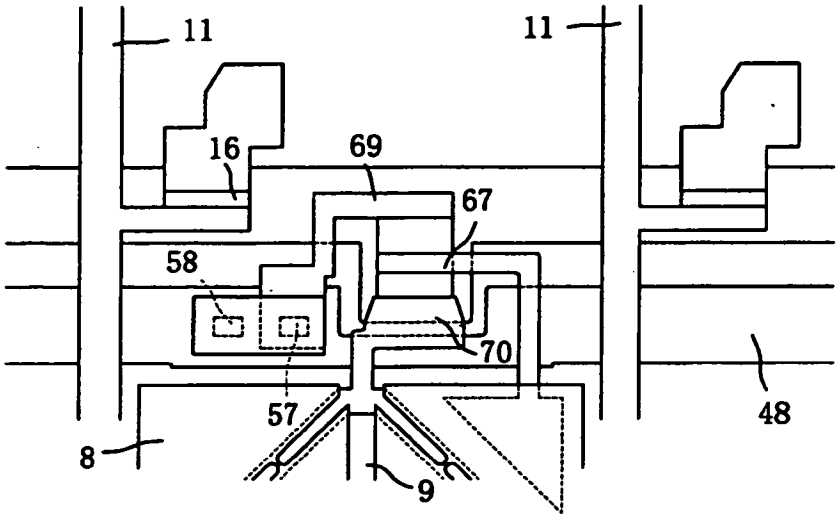


Fig. 81

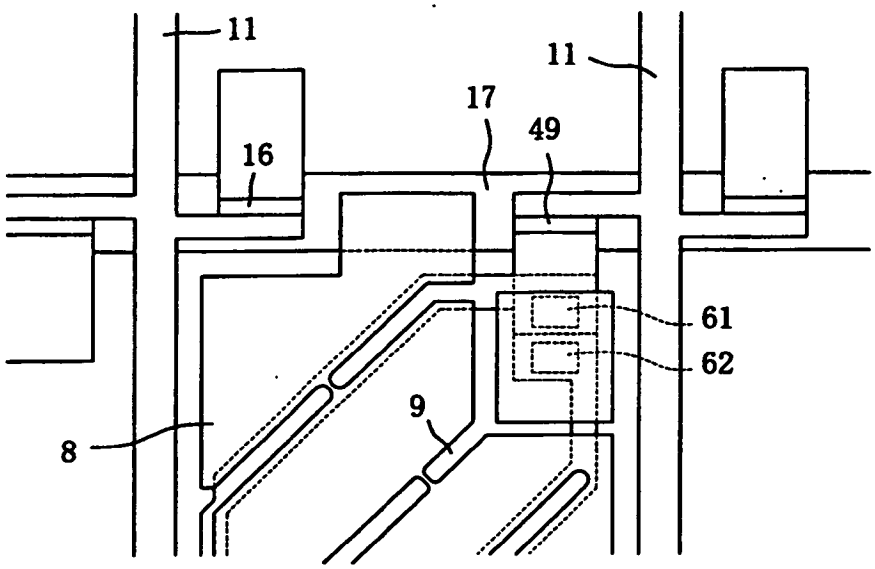


Fig. 82

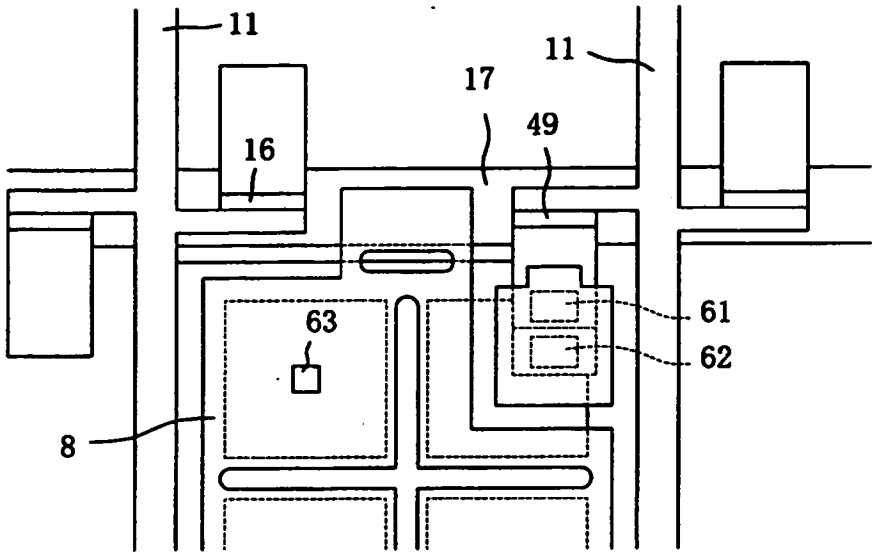


Fig. 83

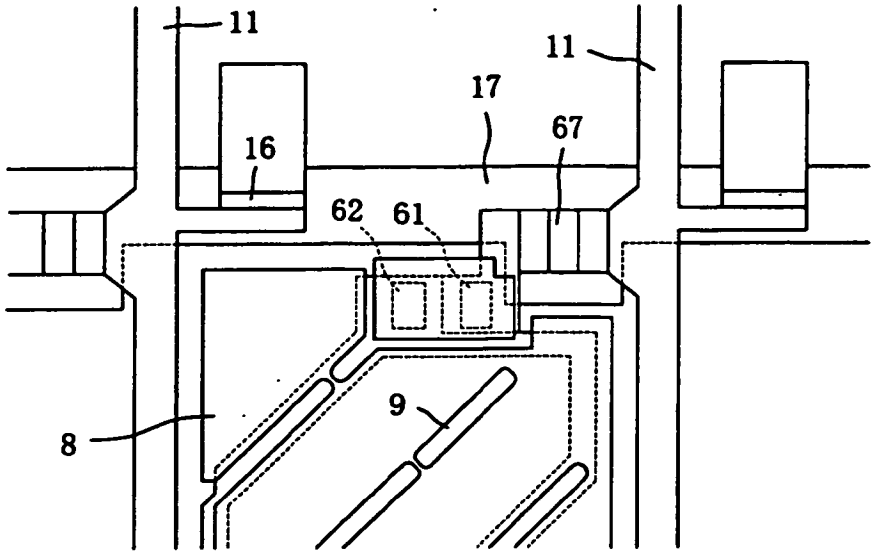


Fig. 84

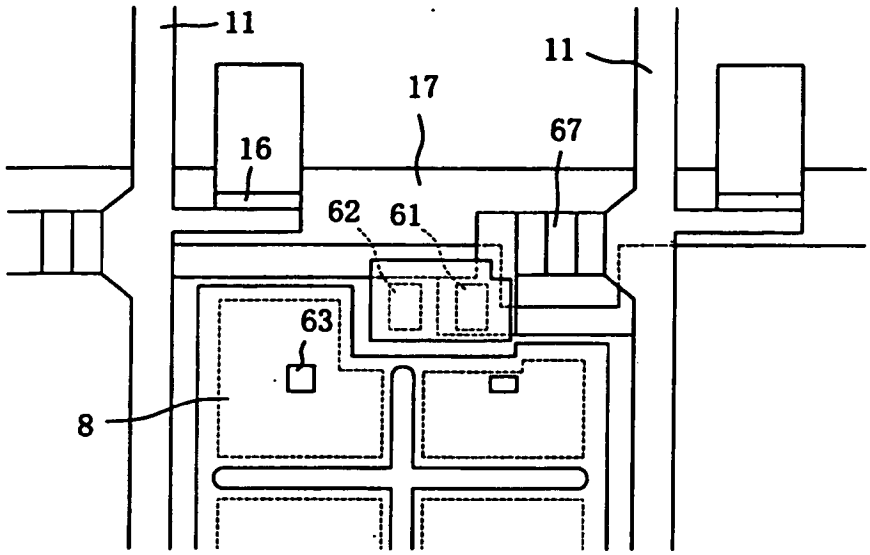


Fig. 85

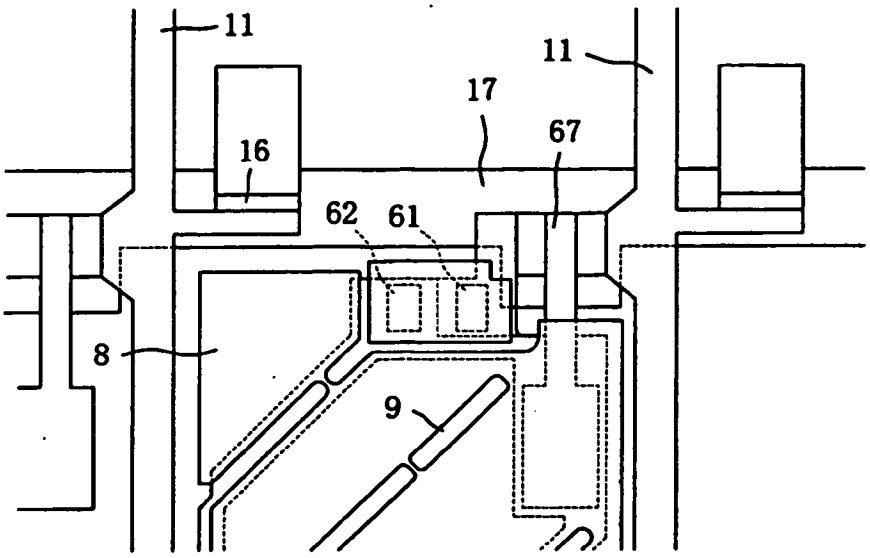
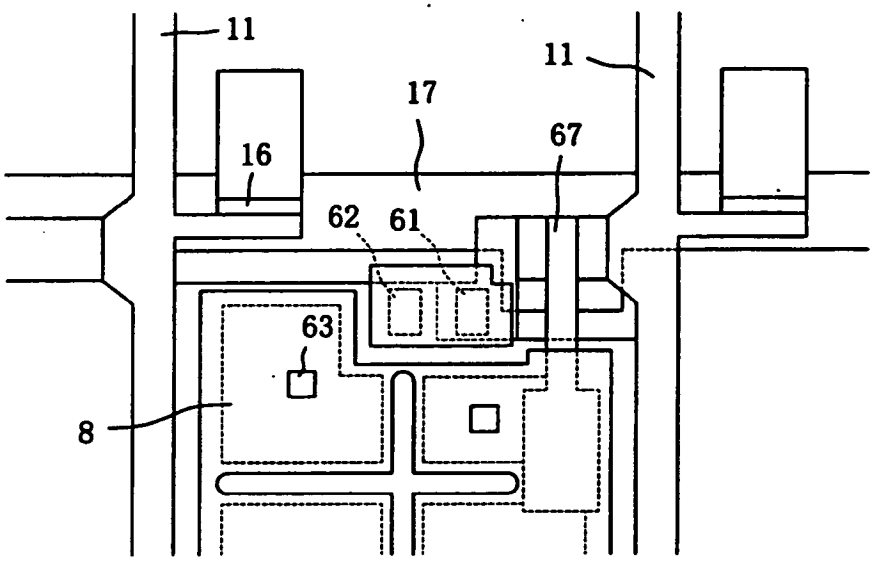


Fig. 86



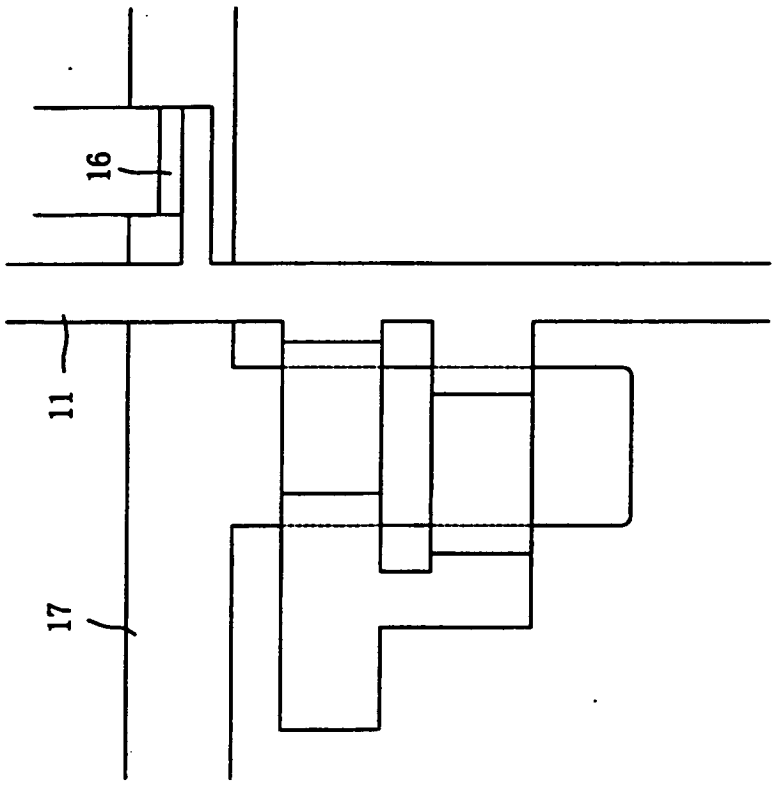


Fig. 87

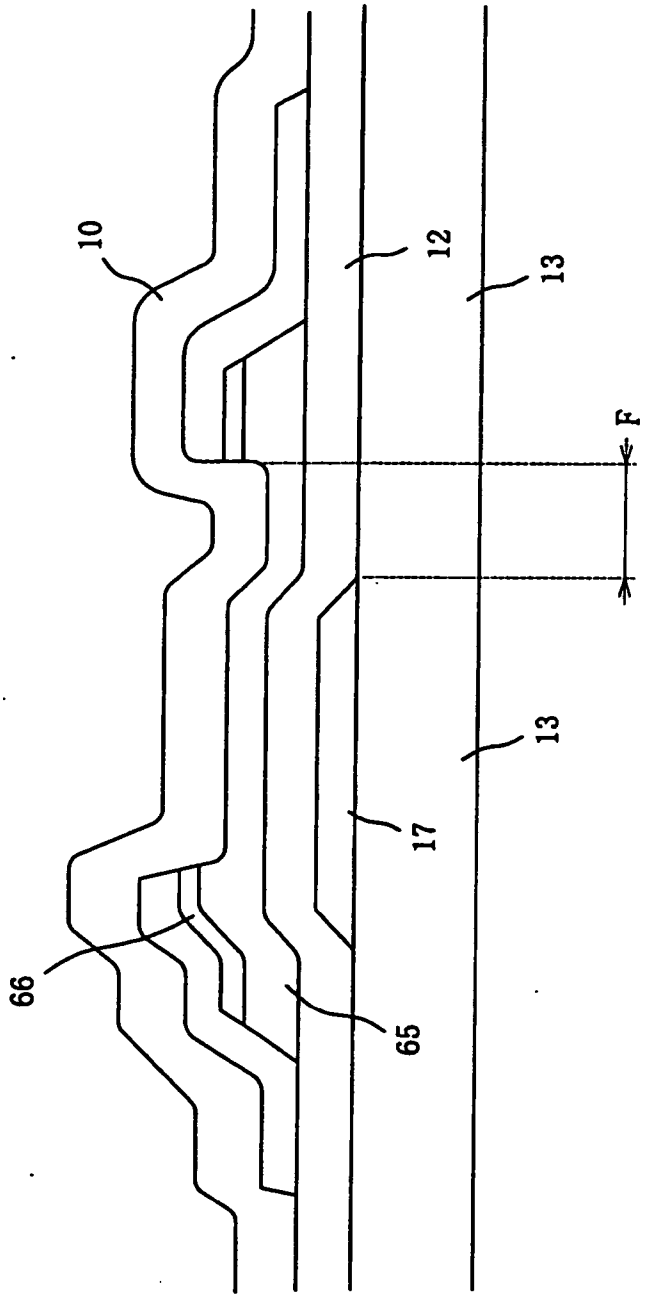


Fig. 88

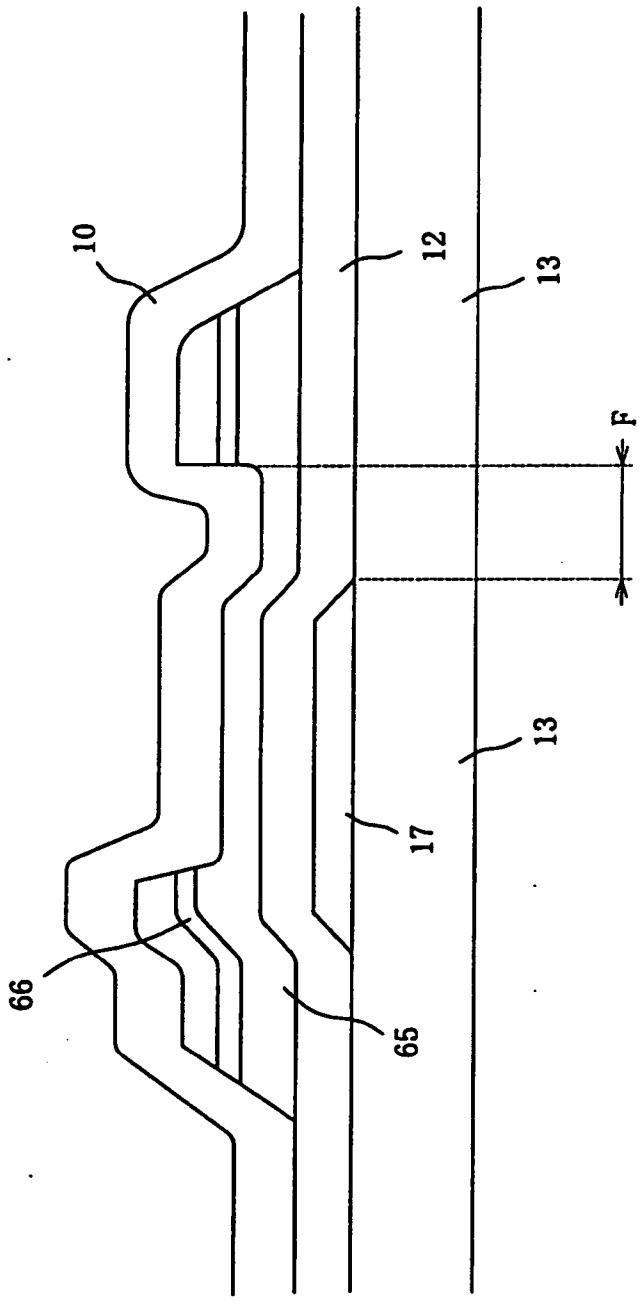


Fig. 89

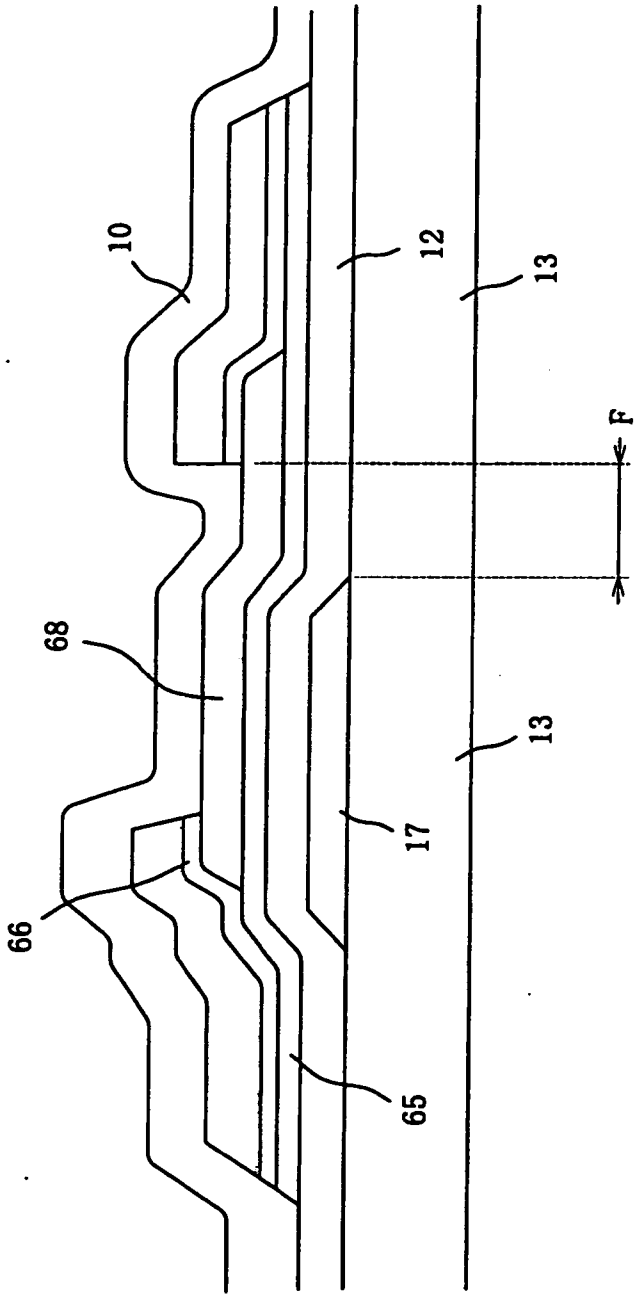


Fig. 90

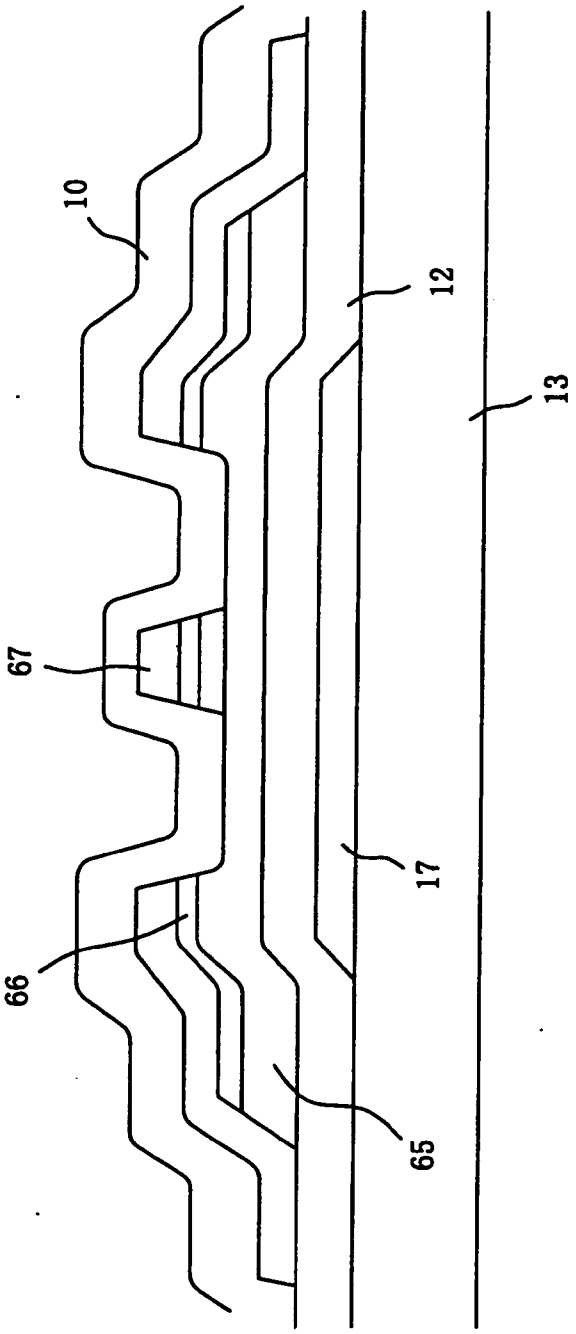


Fig. 91

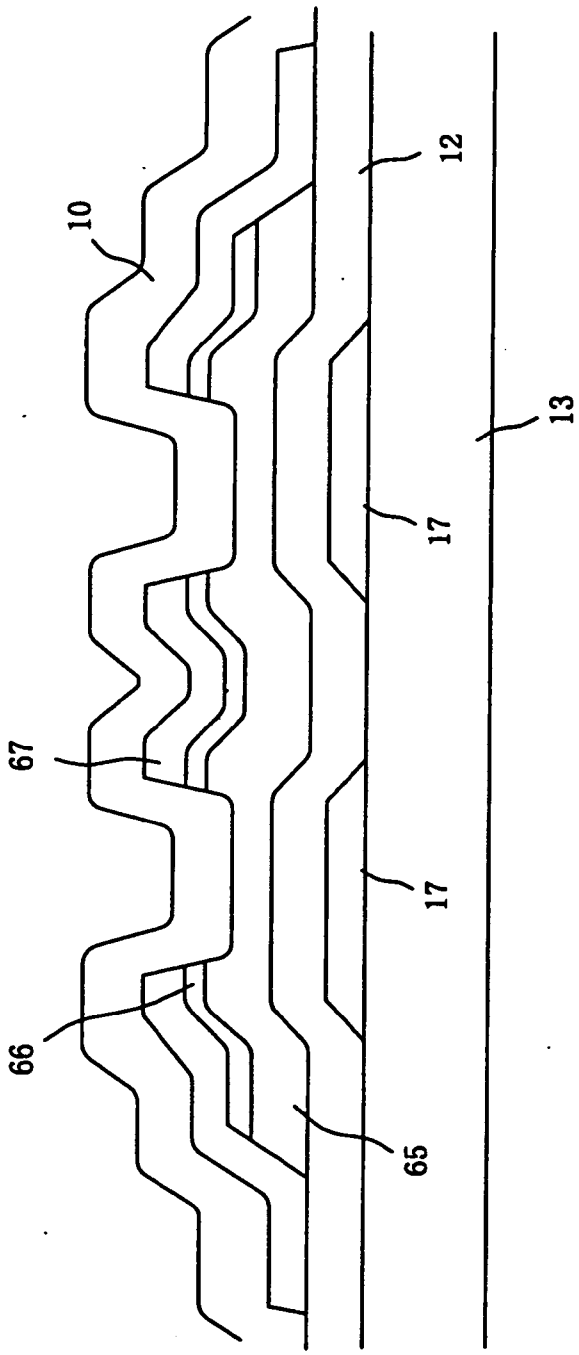


Fig. 92

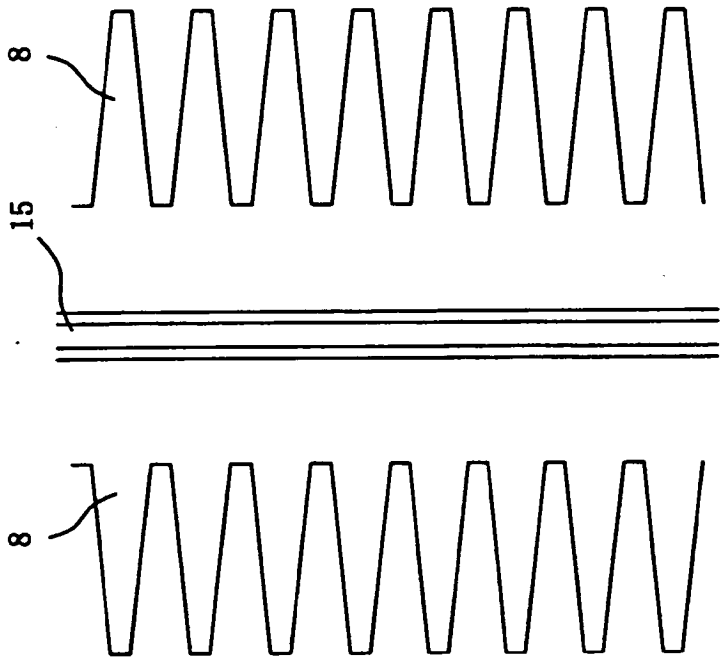


Fig. 93

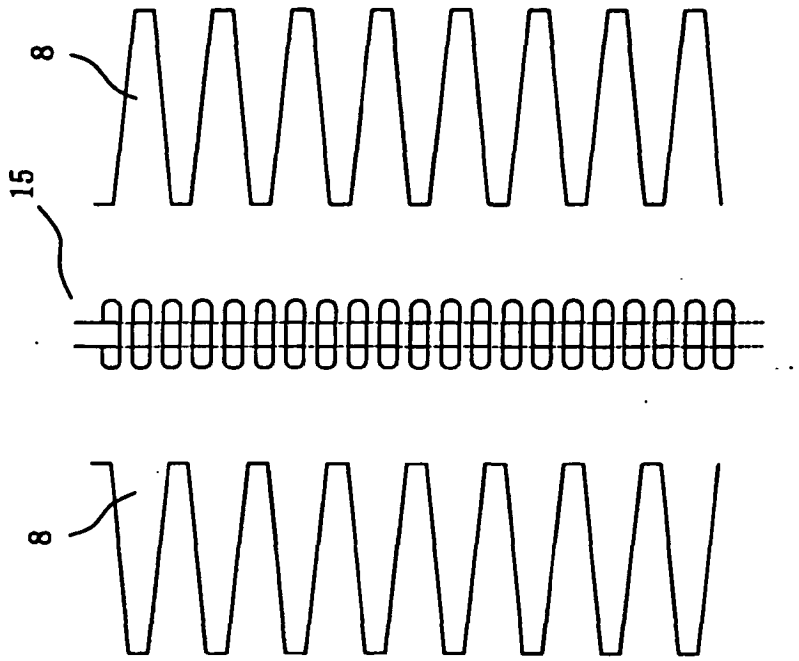


Fig. 94

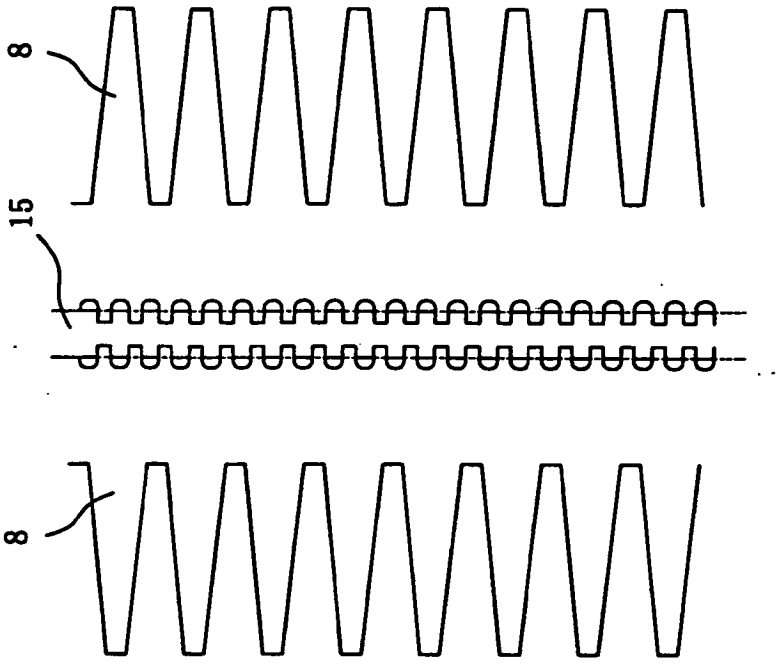
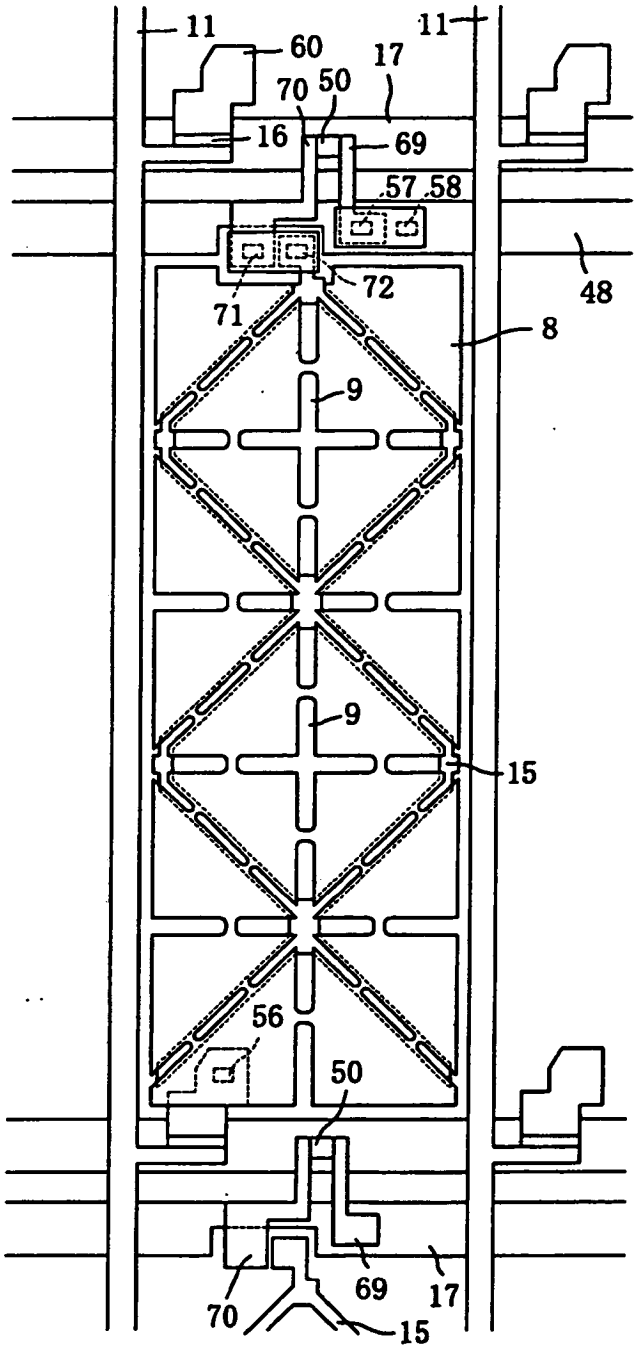


Fig. 95

Fig. 96



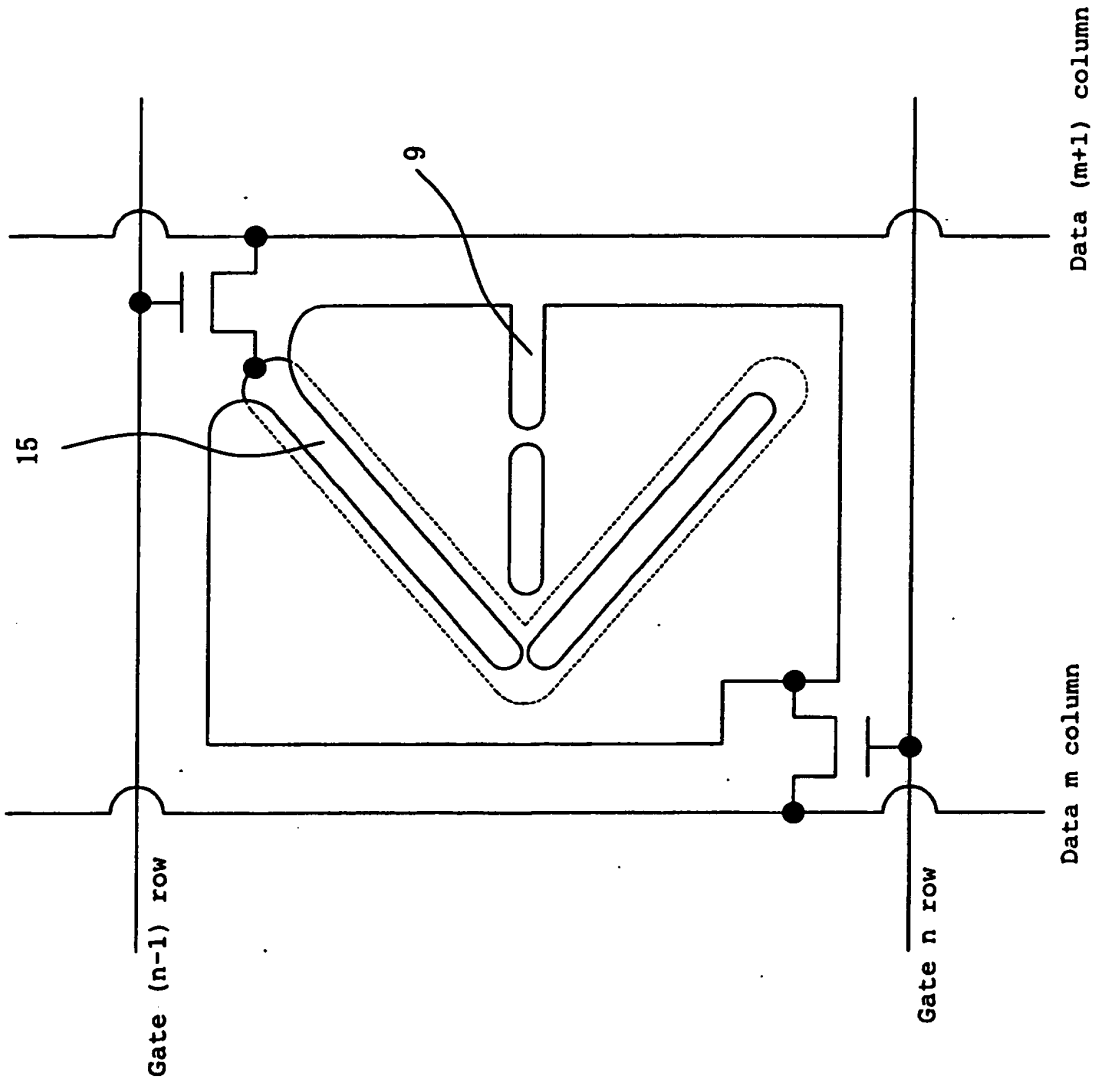


Fig. 97

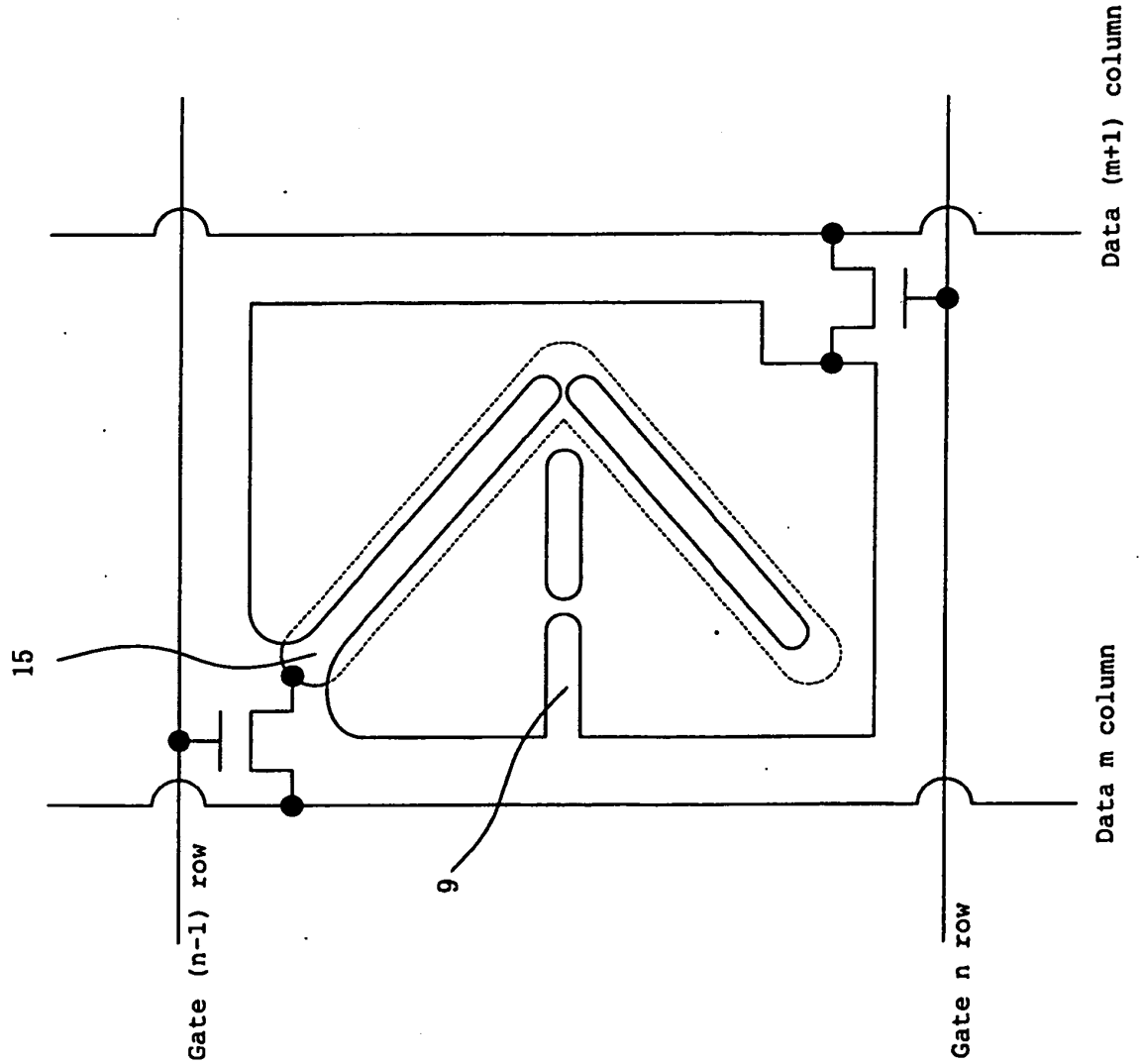


Fig. 98

Fig. 99

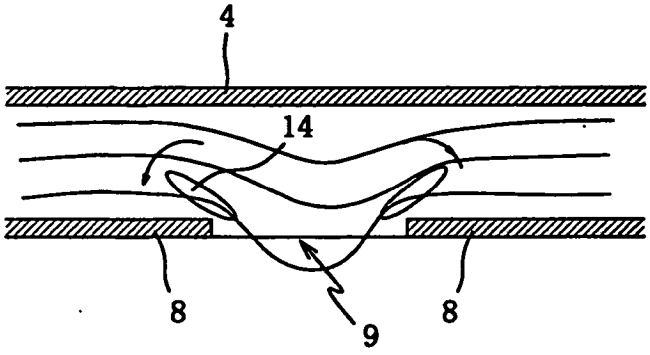


Fig. 100

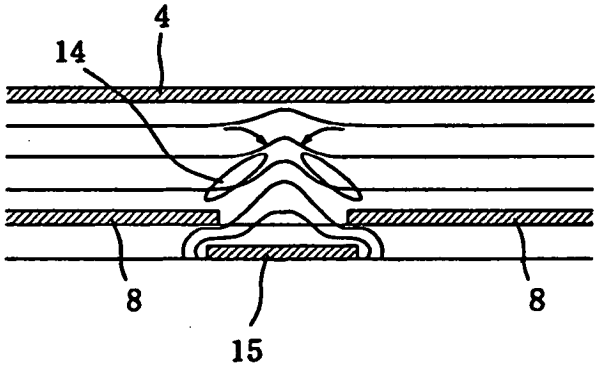
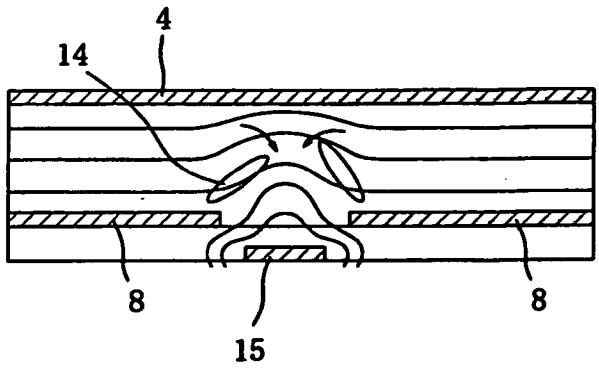


Fig. 101



专利名称(译)	彩色有源矩阵型垂直对准模式液晶显示器及其驱动方法		
公开(公告)号	EP1398658B1	公开(公告)日	2007-01-24
申请号	EP2003020606	申请日	2003-09-10
[标]申请(专利权)人(译)	大林精工株式会社		
申请(专利权)人(译)	OBAYASHISEIKOU CO.，LTD.		
当前申请(专利权)人(译)	OBAYASHISEIKOU CO.，LTD.		
[标]发明人	HIROTA NAOTO		
发明人	HIROTA, NAOTO		
IPC分类号	G02F1/1343 G02F1/1337 G02F1/1333 G09G3/36 G02F1/133 G02F1/139		
CPC分类号	G02F1/133707 G02F1/1393 G02F2201/128 G09G3/3614 G09G3/3648		
优先权	2003110895 2003-02-26 JP 2002316865 2002-09-10 JP		
其他公开文献	EP1398658A1		
外部链接	Espacenet		

摘要(译)

适合于显示具有优异视角特性，优异可靠性和高响应速度并且具有高对比度的运动图像的显示器以低成本实现。垂直对准模式液晶显示器包括扫描布线（17），视频信号布线（11），像素电极（8），对准方向控制电极（15）和形成在其中的薄膜晶体管元件（16）。扫描布线和视频信号布线彼此交叉的位置，以及形成在相对基板侧的公共电极，其中由三个电极形成的电场分布包括所述对准方向控制电极，所述像素电极和形成的公共电极在对应基板侧，可以控制具有负介电常数的垂直排列的各向异性液晶分子的倾斜方向。

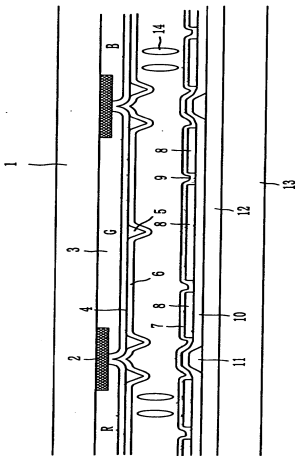


Fig.1