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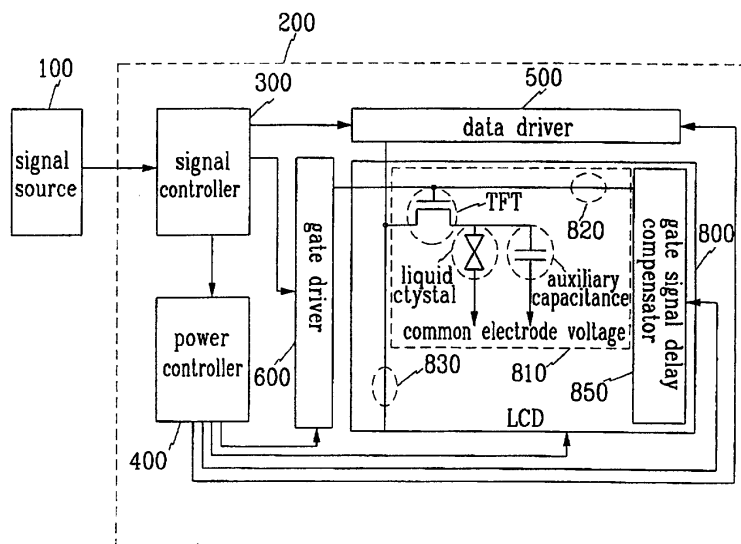
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(54) **Gate signal delay compensating lcd and driving method thereof**

(57) Disclosed is a gate signal delay compensating LCD that comprises an LCD panel including a plurality of gate lines, a plurality of data lines insulated from and crossing the gate lines, a plurality of TFT each of which having a gate electrode connected to the gate line and a source electrode connected to the data line, a pixel electrode connected to a drain electrode of the TFT and a common electrode facing the pixel electrode, liquid crystal filled between the pixel electrode and the common electrode, and a signal delay compensator con-

nected to ends of the gate lines to compensate for the gate signal delay; a gate driver for supplying a gate signal for turning on and off the TFT to the gate line so as to drive the LCD panel; a data driver for supplying a data voltage that represents an image signal to the data line so as to drive the LCD panel; and a signal controller connected to a signal source, the gate driver and the data driver, and processing the image signal provided by the signal source to enable the gate driver to supply a signal for turning on the TFT and the data driver to supply a data voltage to the pixel.

Fig. 1



Description

BACKGROUND OF THE INVENTION

(a) Field of the Invention

[0001] The present invention relates to an LCD, a panel and a method for compensating for gate signal delay. More specifically, the present invention relates to an apparatus and a method for providing a gate signal delay compensating LCD, a panel and a method to be easily implemented without an additional driving integrated circuit (IC) and to compensate for gate-on signal delay due to resistance and capacitance of a gate line without unnecessarily affecting the LCD panel characteristics.

(b) Description of the Related Art

[0002] The thin film transistor liquid crystal display (TFT-LCD) is one of major LCDs, and a target project for the LCD is to increase the size of the LCD panel as well as its resolution. The bigger size and higher resolution of the LCD panel requires longer data lines and gate lines in the panel, which increases line resistance. More crossover points between the lines increase parasitic capacitance of each line. Particularly, when designing a panel of high through-hole ratio to be required in the future, the increased overlaps of the pixels and lines delay signals greatly.

[0003] FIG. 3 shows the above-described gate signal delay of a conventional LCD panel. Referring to FIG. 3, a gate signal is provided as a square wave at an input point. However, when transmitted to a corresponding line on the panel, the signal is delayed at an end of the gate line because of the line resistance and capacitance. Accordingly, the square wave is distorted. The gate signal at the end of the gate line has a delayed waveform because of the distortion. The gate signal delay worsens charging characteristics of each pixel in the LCD panel, because the longer signal delay shortens the gate-on interval of the gate signal. This causes the charging amount at each pixel to fall short from the specification.

[0004] To solve the deteriorated image problem caused by the signal delay at the large LCD panel of high resolution, a driving method for supplying signals at both ends of the gate lines on the LCD panel is suggested. However, this method increases the number of driver IC, and therefore, hindering cost competitiveness.

SUMMARY OF THE INVENTION

[0005] It is an object of the present invention to provide a gate signal delay compensating LCD, its panel and its driving method to be easily implemented without an additional driving integrated circuit (IC). It compensates the delay of a gate-on signal caused by resistance

and capacitance of a gate line without providing unnecessary effects to characteristics of the LCD panel.

[0006] In one aspect of the present invention, a gate signal delay compensating LCD comprises an LCD panel including a plurality of gate lines, a plurality of data lines insulated from and crossing the gate lines, a plurality of TFT each of which having a gate electrode connected to the gate line and a source electrode connected to the data line, and a signal delay compensator having a pixel electrode connected to a drain electrode of the TFT and a common electrode facing the pixel electrode and supplying a common voltage, having liquid crystal filled between the pixel electrode and the common electrode, and connected to ends of the gate lines to compensate for the gate signal delay; a gate driver for supplying a gate signal for turning on and off the TFT to the gate line so as to drive the LCD panel; a data driver for supplying a data voltage that represents an image signal to the data line so as to drive the LCD panel; and a signal controller connected to a signal source, the gate driver and the data driver, and processing the image signal provided by the signal source to enable the gate driver to supply a signal for turning on the TFT and the data driver to supply a data voltage to the pixel.

[0007] The signal delay compensator of the LCD panel comprises a plurality of delay compensation elements each of which connected to an end of the gate line; and a compensation voltage transmission line connected to the delay compensation elements, receiving a predetermined DC voltage from the outside of the LCD panel and transmitting the same to the delay compensation elements.

[0008] The delay compensation element comprises a diode having a current output end connected to an end of the gate line and having a current input end connected to the source electrode of the TFT, and enabling the current to flow in the direction only from the current input end to the current output end; and a delay compensation TFT having a gate electrode connected to the current output end of the diode and the gate line, a source electrode connected to the current input end of the diode and a drain electrode connected to the compensation voltage transmission line so as to enable the current for compensating for the voltage to flow from the drain electrode to the source electrode according to the voltage difference between the gate and source electrodes.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] The accompanying drawings, which are incorporated in and constitute a part of the specification, illustrate an embodiment of the invention, and, together with the description, serve to explain the principles of the invention.

FIG. 1 shows a gate signal delay compensating LCD according to a preferred embodiment of the present invention.

FIG. 2 shows a gate signal delay compensating LCD panel according to a preferred embodiment of the present invention.

FIG. 3 shows a gate signal having a compensated signal delay compared to the delayed gate signal of the conventional device.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0010] In the following detailed description, only the preferred embodiment of the invention has been shown and described, simply by way of illustrating the best mode contemplated by the inventor(s) of carrying out the invention. As will be realized, the invention is capable of modification in various obvious respects, all without departing from the invention. Accordingly, the drawings and description are to be regarded as illustrative in nature, and not restrictive.

[0011] FIG. 1 shows a gate signal delay compensating LCD according to a preferred embodiment of the present invention.

[0012] As shown, the gate signal delay compensating LCD comprises an LCD panel 800 including a plurality of gate lines 820, a plurality of data lines 830, a plurality of TFTs each of which having a gate electrode and a source electrode, a pixel electrode, a common electrode, liquid crystal filled between the pixel electrode and the common electrode, and a signal delay compensator 850 connected to ends of the gate lines 820 to compensate for the gate signal delay; a gate driver 600; a data driver 500; a signal source 100; and a signal controller 300.

[0013] FIG. 2 shows a gate signal delay compensating LCD panel according to a preferred embodiment of the present invention.

[0014] As shown, the gate signal delay compensating LCD panel comprises a plurality of gate lines 820; a plurality of data lines 830; a plurality of TFTs; a pixel electrode; a common electrode; liquid crystal, and a signal delay compensator 850 connected to ends of the gate lines and compensating for gate signal delay. Here, the signal delay compensator 850 is connected to a plurality of delay compensation elements 30, and comprises a compensation voltage transmission line 40 for receiving a predetermined direct current (DC) voltage from the outside of the LCD panel and transmitting the same to the respective delay compensation elements.

[0015] Also, the delay compensation element 30 comprises a diode 10 having a current output end connected to an end of the gate line 820 and a current input end to a source electrode of the TFT 20 in order to flow the current only in the direction from the current input end to the current output end; and a delay compensation TFT 20 having a gate electrode connected to the current output end of the diode 10 and the gate line, a source electrode to the current input end of the diode 10, and a drain electrode to the compensation voltage trans-

mission line 40 in order to flow the voltage compensation current from the drain electrode to the source electrode according to a voltage difference between the gate and source electrodes.

[0016] FIG. 3 shows a gate signal having a compensated signal delay compared with the delayed gate signal in the conventional device.

[0017] As shown, the gate signal delay is compensated, and the gate-on interval during which the gate end maintains high level is recovered to the state of the gate line input waveform of FIG. 3. Accordingly, the problem of shortened charging time caused by the gate signal delay can be overcome.

[0018] When the delayed gate signal is input from the end of the gate line, the voltage of reverse direction is supplied to the diode 10 of the delay compensation element 30, and the current cannot flow through the diode 10. Thus, only the gate voltage of the delay compensating TFT 20 connected to the gate line is increased, and a voltage difference between the gate electrode and source electrode of the TFT 20 is generated, and when the above-noted voltage difference is greater than the threshold voltage, the delay compensating TFT 20 is switched on.

[0019] Accordingly, the compensation current flows from the compensation voltage transmission line 40 connected to the drain electrode of the delay compensating TFT 20 until the potential of the drain electrode becomes equivalent to that of the source electrode. And the potential of the gate line is increased because of the current, and the gate signal delay is compensated. Finally, the waveform of the gate signal as shown at the bottom of FIG. 3 is obtained.

[0020] Also, since no voltage increase as much as the delayed signal is generated at the gate electrode of the delay compensating TFT 20 connected to another gate line to which no gate signal is supplied, the delay compensating TFT 20 cannot be switched on, and as a result, since only the gate line to which the delayed gate signal is supplied is selectively connected to the compensation voltage transmission line 40, an image deterioration problem occurring when another gate line that is not to be driven is concurrently driven is not generated.

[0021] The present invention provides a gate signal delay compensating LCD, its panel and its driving method to be easily implemented without an additional driving integrated circuit (IC). The present invention compensates for the delay of a gate-on signal caused by resistance and capacitance of a gate line without unnecessarily affecting the LCD panel characteristics.

[0022] While this invention has been described in connection with what is presently considered to be the most practical and preferred embodiment, it is to be understood that the invention is not limited to the disclosed embodiments, but, on the contrary, is intended to cover various modifications and equivalent arrangements included within the spirit and scope of the appended

claims.

[0023] Where technical features mentioned in any claim are followed by reference signs, those reference signs have been included for the sole purpose of increasing the intelligibility of the claims and accordingly, such reference signs do not have any limiting effect on the scope of each element identified by way of example by such reference signs.

Claims

1. A gate signal delay compensating liquid crystal display (LCD), comprising:

an LCD panel comprising:

including a plurality of gate lines;
 a plurality of data lines insulated from and crossing the gate lines;
 a plurality of thin film transistors (TFT) each of which having a gate electrode connected to the gate line and a source electrode connected to the data line;
 a pixel electrode connected to a drain electrode of the TFT;
 a common electrode facing the pixel electrode;
 liquid crystal filled between the pixel electrode and the common electrode; and
 a signal delay compensator connected to ends of the gate lines;
 a gate driver for supplying a gate signal for turning on and off the TFT to the gate line so as to drive the LCD panel;
 a data driver for supplying a data voltage that represents an image signal to the data line so as to drive the LCD panel; and
 a signal controller connected to a signal source, the gate driver and the data driver, and processing the image signal provided by the signal source to enable the gate driver to supply a signal for turning on the TFT and the data driver to supply a data voltage to the pixel.

2. The LCD of claim 1, wherein the signal delay compensator of the LCD panel comprises:

a plurality of delay compensation elements, each of which connected to an end of the gate line; and
 a compensation voltage transmission line connected to the delay compensation elements, receiving a predetermined DC voltage from outside of the LCD panel and transmitting the same to the delay compensation elements.

3. The LCD of claim 2, wherein the delay compensation element comprises:

a diode having a current output end connected to an end of the gate line and having a current input end connected to the source electrode of the TFT, and enabling the current to flow in the direction only from the current input end to the current output end; and
 a delay compensation TFT having a gate electrode connected to the current output end of the diode and the gate line, a source electrode connected to the current input end of the diode and a drain electrode connected to the compensation voltage transmission line so as to enable the current for compensating for the voltage to flow from the drain electrode to the source electrode according to the voltage difference between the gate electrode and the source electrode.

4. A liquid crystal display (LCD) panel, comprising:

a plurality of gate lines;
 a plurality of data lines insulated from and crossing the gate lines;
 a plurality of thin film transistors (TFT) each of which having a gate electrode connected to the gate line and a source electrode connected to the data line;
 a pixel electrode connected to a drain electrode of the TFT;
 a common electrode facing the pixel electrode;
 liquid crystal filled between the pixel electrode and the common electrode; and
 a signal delay compensator connected to ends of the gate lines.

5. The LCD of claim 4, wherein the signal delay compensator comprises:

a plurality of delay compensation elements, each connected to an end of the gate line; and
 a compensation voltage transmission line connected to the delay compensation elements, receiving a predetermined DC voltage from outside of the LCD panel and transmitting the same to the respective delay compensation elements.

6. The LCD of claim 5, wherein the delay compensation element comprises:

a diode having a current output end connected to an end of the gate line and having a current input end connected to the source electrode of a TFT, and enabling the current to flow in the direction only from the current input end to the

current output end; and
 a delay compensation TFT having a gate electrode connected to the current output end of the diode and the gate line, a source electrode connected to the current input end of the diode and a drain electrode connected to the compensation voltage transmission line so as to enable the current for compensating for the voltage to flow from the drain electrode to the source electrode according to the voltage difference between the gate electrode and the source electrode.

7. In a signal delay compensating circuit for a liquid crystal display (LCD) panel and compensating for signal delay of a gate line, a signal delay compensating circuit, comprising:

a plurality of delay compensation elements each connected to an end of the gate line; and a compensation voltage transmission line connected to the delay compensation elements, receiving a predetermined DC voltage from outside of the LCD panel and transmitting the same to the respective delay compensation elements.

8. The circuit of claim 7, wherein the delay compensation element comprises:

a diode having a current output end connected to an end of the gate line and having a current input end connected to a source electrode of a TFT, and enabling current to flow in the direction only from the current input end to the current output end; and
 a delay compensation TFT having a gate electrode connected to the current output end of the diode and the gate line, a source electrode connected to the current input end of the diode and a drain electrode connected to the compensation voltage transmission line so as to enable the current for compensating for the voltage to flow from the drain electrode to the source electrode according to the voltage difference between the gate electrode and the source electrode.

9. In a gate signal delay compensation method using a signal delay compensating circuit for a liquid crystal display (LCD) panel and including a plurality of delay compensation elements for compensating for the signal delay of gate lines and a compensation voltage transmission line, a gate signal delay compensation method, comprising steps of:

supplying a predetermined DC voltage to the compensation voltage transmission line; and

connecting only the gate line to which gate signals delayed by the respective delay compensation elements to the compensation voltage transmission line in order to increase the delayed gate signals according to the DC voltage.

10. The method of claim 9, wherein the delay compensation element comprises:

a diode having a current output end connected to an end of the gate line and having a current input end connected to a source electrode of a TFT, and enabling current to flow in the direction only from the current input end to the current output end; and
 a delay compensation TFT having a gate electrode connected to the current output end of the diode and the gate line, a source electrode connected to the current input end of the diode and a drain electrode connected to the compensation voltage transmission line so as to enable the current for compensating for the voltage to flow from the drain electrode to the source electrode according to the voltage difference between the gate electrode and the source electrode.

Fig. 1

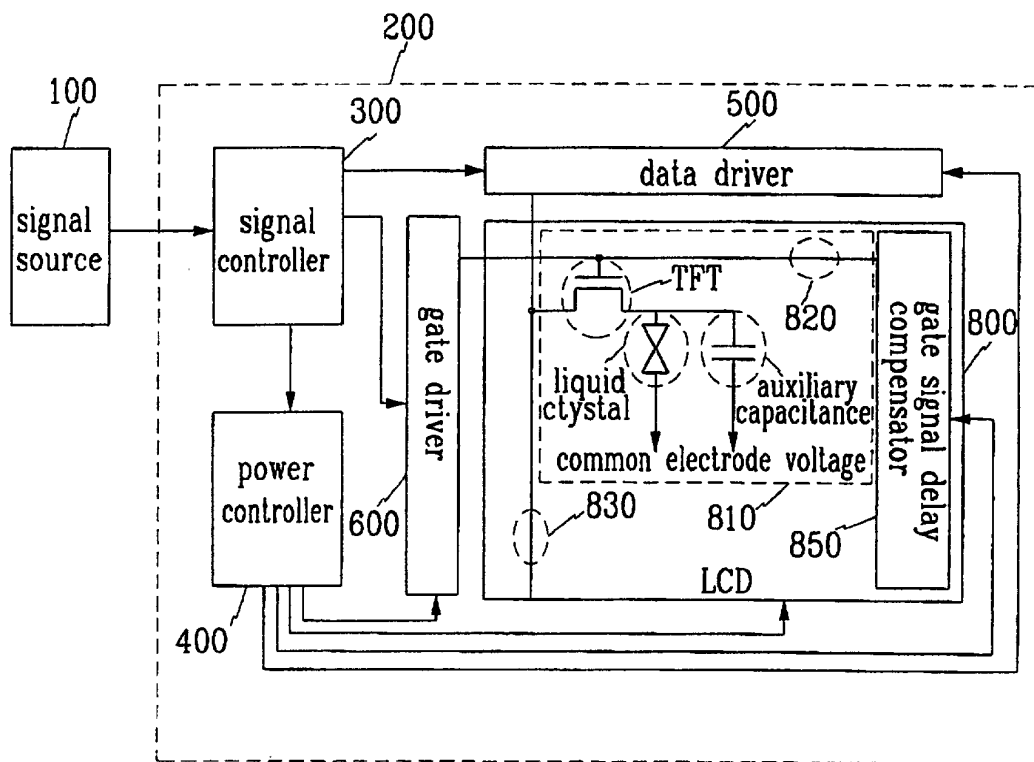


Fig.2

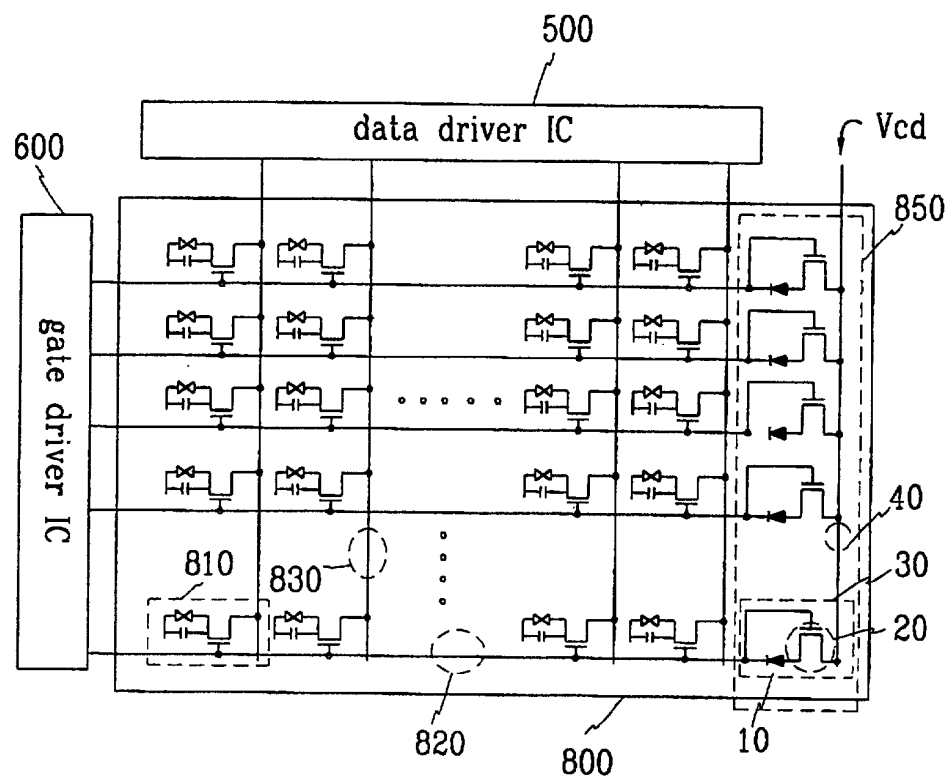
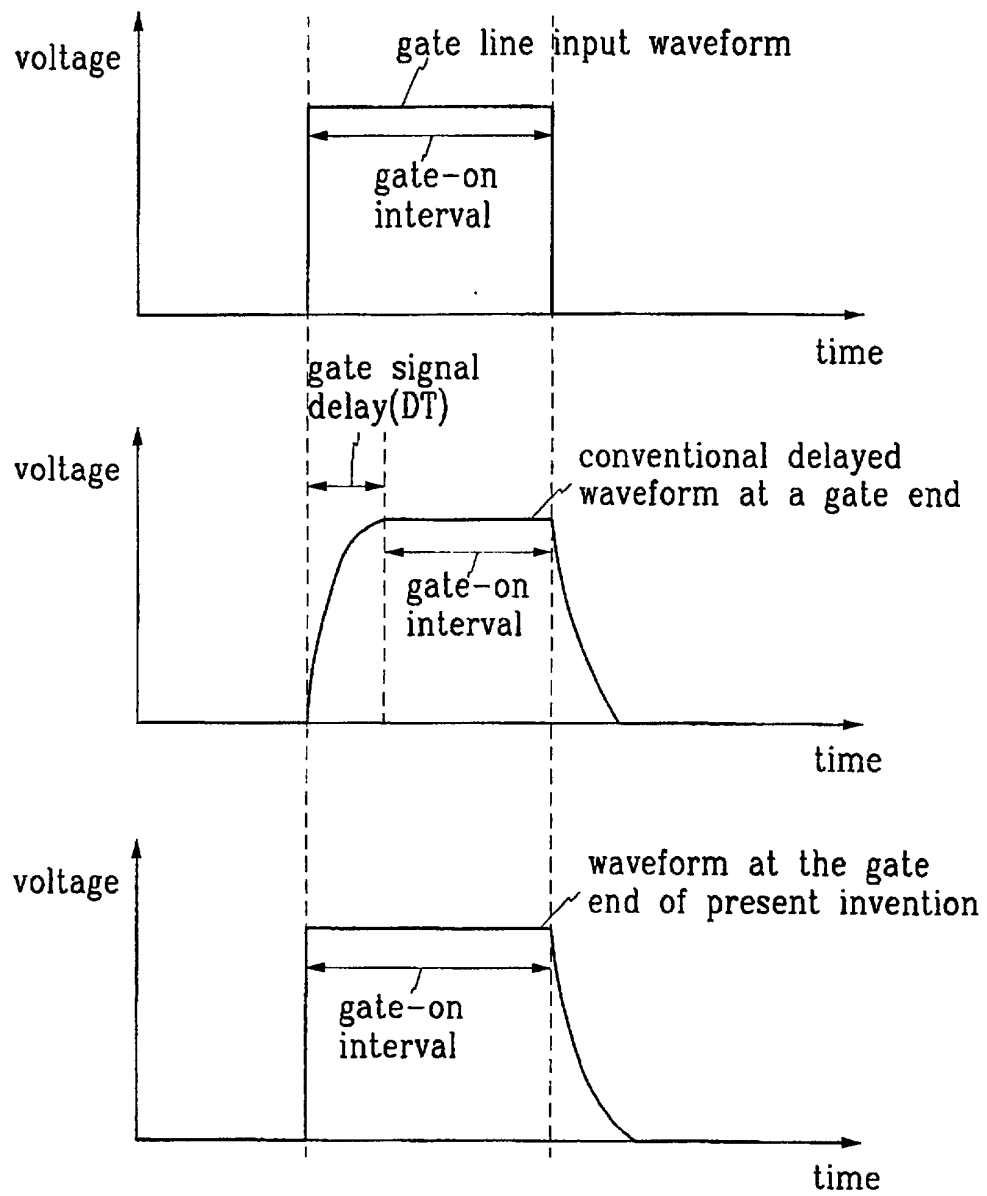


Fig. 3

专利名称(译)	栅极信号延迟补偿液晶显示器及其驱动方法		
公开(公告)号	EP1223571A2	公开(公告)日	2002-07-17
申请号	EP2001125461	申请日	2001-11-05
[标]申请(专利权)人(译)	三星电子株式会社		
申请(专利权)人(译)	SAMSUNG ELECTRONICS CO. , LTD.		
当前申请(专利权)人(译)	三星DISPLAY CO. , LTD.		
[标]发明人	PARK HAENG WON LEE JUNG HEE		
发明人	PARK, HAENG-WON LEE, JUNG-HEE		
IPC分类号	G02F1/1368 G02F1/133 G09G3/20 G09G3/36		
CPC分类号	G09G3/3688 G09G3/3648 G09G2320/0223		
优先权	1020010000420 2001-01-04 KR		
其他公开文献	EP1223571A3		
外部链接	Espacenet		

摘要(译)

公开了一种栅极信号延迟补偿LCD，包括：LCD面板，包括多条栅极线，与栅极线绝缘并与栅极线交叉的多条数据线；多个TFT，每个TFT具有连接到栅极线的栅电极和连接到数据线的源电极，连接到TFT的漏电极的像素电极和面对像素电极的公共电极，填充在像素电极和公共电极之间的液晶，以及连接到端部的信号延迟补偿器栅极线补偿栅极信号延迟；栅极驱动器，用于提供栅极信号，用于导通和关断TFT至栅极线，以驱动LCD面板；数据驱动器，用于向数据线提供表示图像信号的数据电压，以驱动LCD面板；信号控制器，连接信号源，栅极驱动器和数据驱动器，处理信号源提供的图像信号，使栅极驱动器提供开启TFT的信号，数据驱动器提供数据像素的电压。

Fig. 1

