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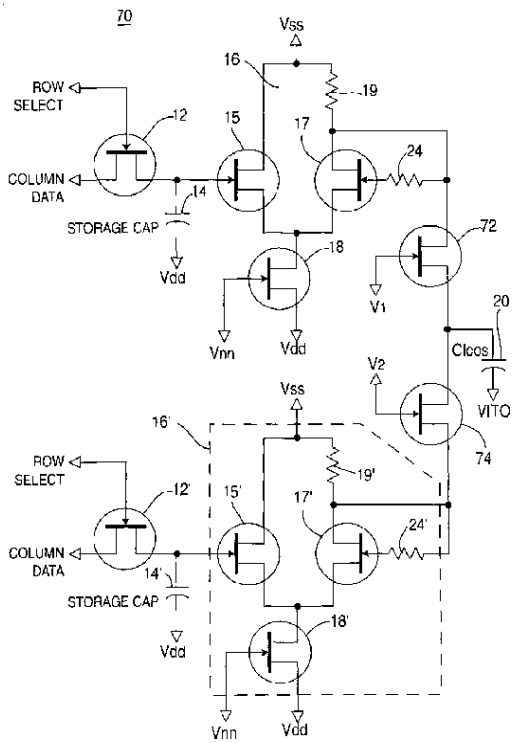
(54)【発明の名称】液晶表示装置用の切替え式増幅器駆動ドライバ回路、方法、および表示装置

(57)【要約】
メモリ素子と、複数の液晶セルのうちの液晶セルとを有する表示ユニット（５０）用のセル・ドライバ（７０）は、第１の記憶コンデンサ（１４）と、第１の記憶コンデンサと液晶セルとの間に選択的に結合されて第１の駆動回路を形成する第１の差動増幅器（１６）とを備える。セル・ドライバはまた、第２の記憶コンデンサ（１４'）と、第２の記憶コンデンサと液晶セルとの間に結合されて第２の駆動回路を形成する第２の差動増幅器（１６'）とを備える。切替え機構（７２および７４）を使用して、第１と第２の駆動回路間で液晶セルを切り替える。



【特許請求の範囲】
【請求項１】
液晶セルのアレイを有する表示装置であって、
表示ドライバ回路のアレイを備え、所定の表示ドライバ回路は、所定の液晶セルに関連し、前記所定の表示ドライバ回路は、
第１の記憶キャパシタンスと、前記第１の記憶キャパシタンスと前記所定の液晶セルとの間に選択可能に結合されて第１の駆動回路を形成する第１の増幅器と、
第２の記憶キャパシタンスと、前記第２の記憶キャパシタンスと前記所定の液晶セルとの間に結合されて第２の駆動回路を形成する第２の増幅器と、
前記第１と第２の駆動回路を切り替えるための切替え手段とを備える表示装置。
【請求項２】
前記第１の増幅器と前記第２の増幅器が、両方とも差動増幅器である、請求項１に記載の表示装置。
【請求項３】
前記差動増幅器が、１対のＮチャネル・トランジスタを備え、前記Ｎチャネル・トランジスタが、結合されたそれぞれのドレイン電極を有し、前記液晶セルへの出力として働く、請求項２に記載の表示装置。
【請求項４】
前記第１と第２の駆動回路が、それぞれ更に、前記それぞれの記憶キャパシタンスと前記増幅器との間に結合された大域スイッチ素子を備え、前記大域スイッチ素子が、前記記憶キャパシタンスからのデータを前記第１と第２の駆動回路の一方に転送する、請求項１に記載の表示装置。
【請求項５】
前記切替え手段が、第１の大域切替え電圧によって駆動される第１のトランジスタと、第２の大域切替え電圧によって駆動される第２のトランジスタとを備える、請求項１に記載の表示装置。
【請求項６】
液晶セル・アレイの所定の液晶セルのための表示ドライバ回路であって、
前記所定の液晶セルの第１のメモリ素子に結合された第１の駆動回路と、
前記所定の液晶セルの第２のメモリ素子に結合された少なくとも第２の駆動回路と、
前記第１と少なくとも第２の駆動回路の間で前記液晶セルを切り替えるための切替え手段とを備える表示ドライバ回路。
【請求項７】
前記第１と第２の駆動回路がそれぞれ、１対のＮチャネル・トランジスタを含む差動増幅器を備え、前記Ｎチャネル・トランジスタが、電流源に結合されたそれぞれのソース電極を有し、前記液晶セルに対する分離増幅器として働く、請求項６に記載の表示ドライバ回路。
【請求項８】
前記第１と第２の駆動回路がそれぞれ、１対のＮチャネル・トランジスタを含む差動増幅器を備え、前記Ｎチャネル・トランジスタが、電流源に結合されたそれぞれのソースを有する、請求項６に記載の表示ドライバ回路。
【請求項９】
前記切替え手段が、第１の大域切替え電圧によって駆動される第１のトランジスタと、第２の大域切替え電圧によって駆動される第２のトランジスタとを備える、請求項６に記載の表示ドライバ回路。
【請求項１０】
記憶コンデンサと差動増幅器との間に結合されて残像およびフリッカを減少させるのに使用される大域スイッチング素子を更に備える、請求項６に記載の表示ドライバ回路。
【請求項１１】
液晶アレイ素子のアレイ全体を同時に更新する、請求項６に記載の表示ドライバ回路。

【請求項１２】
前のフレームから変化したメモリ・セルだけを更新する、請求項６に記載の表示ドライバ回路。
【請求項１３】
ライン間走査アーティファクトを表示することなくメモリ・アレイをインタレース・モードで駆動する、請求項６に記載の表示ドライバ回路。
【請求項１４】
液晶表示装置（ＬＣＤ）／液晶オン・シリコン（ＬＣＯＳ）表示装置を駆動する方法であって、
複数の駆動セルのうちの各駆動セル中で差動増幅器を使用して記憶キャパシタンスと液晶セルとの間の分離を与えるステップと、
前記複数の駆動セル間を切り替えて前記液晶セルを駆動するステップとを含む方法。
【請求項１５】
前記与えるステップが更に、第１の駆動セル中で、第１の差動増幅器を使用して第１の記憶キャパシタンスと前記液晶セルとの間の分離を与え、第２の駆動セル中で、第２の差動増幅器を使用して第２の記憶キャパシタンスと前記液晶セルとの間の分離を与えるステップを含む、請求項１４に記載の方法。
【請求項１６】
前記切り替えるステップが更に、前記第１の駆動セルと前記第２の駆動セルとの間を切り替えるための１対のトランジスタを使用して、前記第１の駆動セルと前記第２の駆動セルとの間を切り替えるステップを含む、請求項１５に記載の方法。
【請求項１７】
フレームを倍増せずにフリッカを無くすステップを更に含む、請求項１５に記載の方法。
【請求項１８】
液晶素子のアレイ全体を同時に更新するステップを更に含む、請求項１４に記載の方法。
【請求項１９】
前のフレームから変化したメモリ・セルだけを更新するステップを更に含む、請求項１４に記載の方法。
【請求項２０】
ライン間走査アーティファクトを表示することなくメモリ・アレイをインタレース・モードで駆動するステップを更に含む、請求項１４に記載の方法。
【請求項２１】
共通電極電圧をフレーム間で変調して、必要とされる液晶駆動電圧を低減するステップを更に含む、請求項１４に記載の方法。
【発明の詳細な説明】
【０００１】
（発明の分野）
本発明は、液晶表示装置（ＬＣＤ：Ｌｉｑｕｉｄ　Ｃｒｙｓｔａｌ　Ｄｉｓｐｌａｙ）または液晶オン・シリコン（ＬＣＯＳ：Ｌｉｑｕｉｄ　Ｃｒｙｓｔａｌ　Ｏｎ　Ｓｉｌｉｃｏｎ）を利用したビデオ・システムの分野に関し、より詳細には、このような表示装置用の切替式ドライバ回路（ｓｗｉｔｃｈｅｄ　ｄｒｉｖｅｒ　ｃｉｒｃｕｉｔ）に関する。
【０００２】
（発明の背景）
液晶オン・シリコン（ＬＣＯＳ）は、シリコン・ウェーハ（ｓｉｌｉｃｏｎ　ｗａｆｅｒ）上に形成された大きな１つの液晶と考えることができる。シリコン・ウェーハは、小さなプレート電極（ｐｌａｔｅ　ｅｌｅｃｔｒｏｄｅ）の増分（ｉｎｃｒｅｍｅｎｔａｌ）アレイ（ａｒｒａｙ：配列）に分割される。液晶の小さな増分領域が、小さな各プレートおよび共通プレート（ｃｏｍｍｏｎ　ｐｌａｔｅ）により発生される電界の影響を受ける。このような小さな各プレートおよび対応する液晶領域は、合わせてイメージャ（ｉｍａｇｅｒ）のセル（ｃｅｌｌ）と呼ばれる。各セルは、個別に制御可能なピクセル（ｐｉｘ

ｅｌ）に対応する。液晶（ＬＣ：Ｌｉｑｕｉｄ　Ｃｒｙｓｔａｌ）の反対側には、共通プレート電極が配置される。駆動電圧が、液晶オン・シリコン（ＬＣＯＳ）アレイの各側のプレート電極に供給される。各セルまたはピクセルは、入力信号が変更されるまで同じ強度で輝き続け、従って、サンプル・アンド・ホールド（ｓａｍｐｌｅ　ａｎｄ　ｈｏｌｄ）回路として働く。共通プレート電極と可変プレート電極の各セット（組）が、イメージャを形成する。イメージャは、各色につき１つ供給され、この場合、赤、緑、青にそれぞれ１つのイメージャが供給される。

【０００３】

通常、液晶オン・シリコン（ＬＣＯＳ）表示装置のイメージャは、３０Ｈｚのフリッカを防止するために、フレームを２倍に倍増させた信号で駆動する。これは、所定の入力ピクチャ（画像）に応答して、各セルに関連する電極の電圧が、共通電極の電圧に対して正（ｐｏｓｉｔｉｖｅ）である第１の正常フレーム（ｎｏｒｍａｌ　ｆｒａｍｅ）（正ピクチャ（ｐｏｓｉｔｉｖｅ　ｐｉｃｔｕｒｅ））を送り、次いで、各セルに関連する電極の電圧が共通電極の電圧に対して負（ｎｅｇａｔｉｖｅ）である逆フレーム（ｉｎｖｅｒｔｅｄ　ｆｒａｍｅ）（負ピクチャ（ｎｅｇａｔｉｖｅ　ｐｉｃｔｕｒｅ））を送ることにより行われる。正と負のピクチャを生成することにより、各ピクセルは、確実に、正の電界で描かれてから負の電界で描かれることになる。その結果得られる駆動電界のＤＣ（直流）成分は、０（零）であり、これは画像の焼き付き、および究極的にはイメージャの永久劣化を防止するのに必要である。人間の目は、これらの正と負のピクチャによって生成されるピクセルの輝度の平均値に応答することが測定されている。

【０００４】

液晶オン・シリコン（ＬＣＯＳ）の現在の技術では、V_{ITO}（またはＶＩＴＯ）として表されるコモンモード電極電圧（ｃｏｍｍｏｎ　ｍｏｄｅ　ｅｌｅｃｔｒｏｄｅ　ｖｏｌｔａｇｅ）を、正確に液晶オン・シリコン（ＬＣＯＳ）についての正と負のフィールド駆動の間に入るように調節することが必要である。下付き文字のＩＴＯは、材料のインジウム錫酸化物（Ｉｎｄｉｕｍ　Ｔｉｎ　Ｏｘｉｄｅ）を表す。フリッカ（ｆｌｉｃｋｅｒ：ちらつき）を最小限に抑え、更に画像の焼き付き（ｉｍａｇｅ　ｓｔｉｃｋｉｎｇ）と呼ばれる現象を防止するには、平均バランス（ａｖｅｒａｇｅ　ｂａｌａｎｃｅ）が必要である。

【０００５】

現在の技術では、液晶オン・シリコン（ＬＣＯＳ）駆動セル（ｄｒｉｖｅ　ｃｅｌｌ）は、従来のアクティブ・マトリックスＬＣＤドライバと類似している。これは、文献で論じられている様々なアーティファクト（ａｒｔｉｆａｃｔ）が原因で、余りうまく機能しない。主な原因は、液晶（ＬＣ）材料のイオン漏出およびバルク抵抗率による、寄生容量漏話（ｐａｒａｓｔｉｃ　ｃａｐａｃｉｔａｎｃｅ　ｃｒｏｓｓ－ｔａｌｋ）、液晶（ＬＣ）セル中の残留電圧、および液晶（ＬＣ）の電圧ドループ（ｄｒｏｏｐ：電圧降下ひずみ）である。これは、主に次のことにより解決されてきた。即ち、１．セル・キャパシタンスを増加させること（物理的領域によって制限される）、２．より高い抵抗率の液晶（ＬＣ）材料に変更すること（フレキシビリティおよび応答時間を制限する）、３．フレーム走査レートを増加させて６０Ｈｚよりも高くすること（高価であり、より多くの帯域幅を要する）、４．デバイスの温度を積極的に制御して高い電圧保持率（ＶＨＲ：Ｖｏｌｔａｇｅ　Ｈｏｌｄｉｎｇ　Ｒａｔｉｏ）を維持することである。

【０００６】

上述のすべての問題の主な原因は、利用可能な電荷が１フレームにつき１度だけしか液晶（ＬＣ）セルに転送されないということである。このことにより、非常に多数のピクセルを有する表示装置では、利用可能な電力が制限され、また、所望の電圧が実際にピクセル電極上で実現されたことを調べる如何なる閉ループ・チェック方法も存在しない。加えて、フリッカ、駆動電圧、および残像の問題は、ディジタル駆動液晶オン・シリコン（ＬＣＯＳ）表示装置については様々な方法で対処されてきたが、そのような方法は、アナログ・システムにおける問題には、継続的な更新が必要なことに因り解決をもたらすことがで

きない。従って、記憶コンデンサと液晶セルとの間に適切な分離（ｉｓｏｌａｔｉｏｎ）を与え、更にフレームを倍増することを必要とせずにフリッカを無くす表示ドライバ回路および方法が必要とされている。

【０００７】

（発明の概要）

本発明の第１の態様では、メモリと、複数の液晶セルのうちの一つの液晶セルとを有する表示ユニット用の表示ドライバは、前記液晶セルの第１のメモリ素子に結合された第１の駆動回路と、前記液晶セルの第２のメモリ素子に結合された第２の駆動回路と、前記第１と第２の駆動回路間で前記液晶セルを切り替えるための切替え機構（回路、手段）とを備える。

【０００８】

本発明の第２の態様では、対応する液晶セル・アレイを有する表示ユニット用の、アレイ・ドライバのアレイのうちの一つの表示ドライバは、第１の記憶キャパシタンスと、前記第１の記憶キャパシタンスと前記液晶セルとの間に選択的に結合されて第１の駆動回路を形成する第１の増幅器と、第２の記憶キャパシタンスと、前記第２の記憶キャパシタンスと前記液晶セルとの間に選択的に結合されて第２の駆動回路を形成する第２の増幅器と、前記第１と第２の駆動回路を切り替えるための切替え機構（回路、手段）とを備える。

【０００９】

本発明の第３の態様では、液晶表示装置（ＬＣＤ）／液晶オン・シリコン（ＬＣＯＳ）表示装置を駆動する方法は、複数の駆動セルのうちの各駆動セル中で差動増幅器を使用して記憶キャパシタンスを液晶セルから分離するステップと、前記複数の駆動セル間を切り替えて液晶セルを駆動するステップとを含んでいる。

【００１０】

（好ましい実施形態の詳細な説明）

前述の問題を解決するため、図１に示すように、内部記憶キャパシタンス（ｉｎｔｅｒｎａｌ　ｓｔｏｒａｇｅ　ｃａｐａｃｉｔａｎｃｅ）１４と液晶（ＬＣ：Ｌｉｑｕｉｄ　Ｃｒｙｓｔａｌ）セル２０との間に差動増幅器（ｄｉｆｆｅｒｅｎｔｉａｌ　ａｍｐｌｉｆｉｅｒ）１６などの増幅器を追加することを提案する。言い換えれば、駆動液晶（ＬＣ）セルに駆動増幅器（ｄｒｉｖｅ　ａｍｐｌｉｆｉｅｒ）を追加する。これにより、記憶コンデンサ（ｓｔｏｒａｇｅ　ｃａｐａｃｉｔｏｒ）と液晶（ＬＣ）セルとの間に分離（ｉｓｏｌａｔｉｏｎ）を加える。電流駆動機能を追加することで、ピクセル上の電圧が素早く所望の電圧になることが保証される。また、これによって、記憶コンデンサからの漏れ電流（ｌｅａｋａｇｅ　ｃｕｒｒｅｎｔ）をごく少なくし（ＦＥＴが非常に高い入力インピーダンスを有するので）、液晶（ＬＣ）上の電圧を継続的にリフレッシュ（ｒｅｆｒｅｓｈ）することができる。これは電圧の下降を引き起こす「ドループ（ｄｒｏｏｐ）」問題を無くし、更に、セルに蓄積される残留ボルタ電位も無くす。これは、フリッカの問題と、セル中のＤＣ（直流）バランスを達成できないことに関連する「画像の焼き付き」問題との両方を改善する。また、いくぶん高温の状況でもセルが良好に動作することを可能にする。

【００１１】

この技法の不利な点は、液晶セルを流れるＤＣ電流が増加することである。この点は、差動増幅器の底部の電流源をゲートすることにより部分的に解決することができる。これには、デバイス中で「ピクセル選択（ｐｉｘｅｌ　ｓｅｌｅｃｔ）」または「行選択（ｒｏｗ　ｓｅｌｅｃｔ）」ビットを使用することができる（図１参照）。このようにして、電力消費を１／ｎｒｏｗだけ低減しながら、電圧の定期的なリフレッシュを達成することができる。ｎｒｏｗは、デバイス中の行の数である。加熱が均一なので、状況によってはこのゲーティング（ｇａｔｉｎｇ）が必要とされない場合もある。

【００１２】

図１には、ＣＭＯＳ（相補型ＭＯＳ）中の典型的な実施形態を示す。各構成要素は、概略的に表すものであり、一般性を失わずに代替構成を用いることができる。重要なポイント

は、液晶（ＬＣ）セルに閉ループ補正電圧を加える増幅器１６と、電力消費の低減を可能にするゲート電流源である。

【００１３】

通常、この回路は、３つのトランジスタを使用して実現することができ、これらのトランジスタは、液晶オン・シリコン（ＬＣＯＳ）表示デバイス中の液晶セルの下に配置することができる。図１の構成で、増幅器１６は液晶（ＬＣ）セルをメモリ素子から分離している。図１には、液晶表示装置用の液晶セル・ドライバ１０が示してある。この液晶セル・ドライバ１０は、図１に示すように、相互に結合された複数のトランジスタ（１２、１５、１７、１８）と、記憶コンデンサ１４などの記憶キャパシタンスと、複数の抵抗器１９および２１を備えていることが好ましい。トランジスタ１５、１７、１８などの３つのトランジスタが増幅器１６を形成することが好ましく、増幅器１６は、バッファ増幅器または分離増幅器として働く差動増幅器の形式をとることが好ましい。差動増幅器１６は、液晶セルへの出力として働くＮチャネル・トランジスタで形成されることが好ましい。加えて、差動増幅器のトランジスタの各ソース電極は、トランジスタ１８のようなゲート制御可能なＮチャネル・トランジスタ等の電流源により駆動される。この電流ミラー構成は、所定のピクセル上で所定の電圧を保証する。差動増幅器１６は、記憶コンデンサ１４との間に結合され、記憶コンデンサ１４と液晶セルまたはピクセルとの間の分離を与える。

【００１４】

図２の構成では、データを記憶素子からドライバに転送するための大域スイッチ素子（ｇｌｏｂａｌ　ｓｗｉｔｃｈ　ｅｌｅｍｅｎｔ）３２を追加している。このことは、同じ回路動作電圧に対してピクセル駆動能力を増大させることを可能にし、また、ピクセル駆動電圧およびＩＴＯ透過性導電電極をフレーム間で反転できるようにすることによって、残像（ｉｍａｇｅ　ｒｅｔｅｎｔｉｏｎ）およびフリッカを減少させる。図２を参照すると、図１の液晶セル・ドライバ１０に類似する別の液晶セル・ドライバ３０が示されている。セル・ドライバ１０に関して先に挙げた要素に加えて、セル・ドライバ３０は更に、記憶コンデンサ１４と差動増幅器１６との間に結合された、トランジスタの形式をとる大域スイッチ素子３２も備える。大域スイッチ素子は、データをメモリ・セルから表示ドライバのドライバ・コンデンサ３６に転送する。

【００１５】

フリッカの問題は、過去に多くの方法によって対処されてきた。また、駆動電圧および残像の問題は、ディジタル駆動液晶オン・シリコン（ＬＣＯＳ）表示装置では対処されてきた。アナログ・システムの場合、駆動電圧および残像の問題は、継続的に更新する必要があるため同様に対処することができる。

【００１６】

本明細書に開示する技法の主な利点は、ドライバ・コンデンサ３６を記憶コンデンサ１４から分離することにある。図２に示すこの分離により、望むなら、液晶（ＬＣ）アレイ全体のセルすべてを一度に更新することができる。この利点には２つの側面がある。第１に、この分離により（液晶（ＬＣ）セルがフレーム間で変化したことを決定するための前処理を追加して）、液晶（ＬＣ）アレイ中で前のフレームから変化したセルだけを更新することもできる。言い換えれば、液晶（ＬＣ）セル上の表示内容を瞬時に変更することなく記憶コンデンサ１４の内容を変更することができる。これにより、静的なピクチャ（画像）に必要なデータ・レートが大きく低減される。また、ライン間走査アーティファクトを表示することなく表示装置をインタレース・モード（ｉｎｔｅｒｌａｃｅｄ　ｍｏｄｅ）で駆動することも可能になる。通常、インタレースされるシステムでは、第１の走査（ｓｃａｎ）で奇数ラインが描かれ、第２の走査（ｓｃａｎ）で偶数ラインが描かれる。この走査方式は、「ライン間フリッカ（ｉｎｔｅｒｌｉｎｅ　ｆｌｉｃｋｅｒ）」と呼ばれるアーティファクトを生じる。これはフィルムなど、本来はインタレースされないデータの場合でも発生する。「ライン間フリッカ」の理由は、あるフレームからの偶数ラインが、前のフレームからの奇数ラインが表示されるのと同時に表示されるからである。フレームのどんな変化部分も、「ライン間フリッカ」を呈することになる。本発明によれば、液晶

（ＬＣ）セル・アレイに対応する記憶コンデンサ（１４）アレイを有する表示装置を通常どおり（偶数ラインに続いて奇数ライン）更新するが、例外として、次いで記憶アレイが満たされた後で液晶（ＬＣ）アレイ全体を更新する。従って、異なるフレームからのラインが同時に表示されることはない。この技法の第２の利点は、共通電極電圧をフレーム間で変調できることである。この変調により、ドライバ回路の所定の動作電圧で液晶（ＬＣ）セルに加えることのできる実効電界（ｅｆｆｅｃｔｉｖｅ　ｅｌｅｃｔｒｉｃ　ｆｉｅｌｄ）が増大する。プロセス・ジオメトリ（ｐｒｏｃｅｓｓ　ｇｅｏｍｅｔｒｙ）が、精緻になるほど最大許容駆動電圧は低下するので、これは大きな利点である。前述の利点は、ピクセルすべてが一度に更新されるときにのみ生じる。ピクセルを同時に更新することは、記憶アレイ（記憶コンデンサ１４のアレイ）が、ドライバ・アレイ（ドライバ・コンデンサ３６のアレイ）から分離されている場合にのみ行うことができる。

【００１７】

この技法は、図１で述べた回路によって最も簡単に実現することができ、図２に示すように変更することもできる。図２の電圧Ｖｎｎは、トランジスタ１５および１７のための電流源を制御する静的な電圧である。行と列のアドレスは、アクティブ・マトリックス・ディスプレイに於ける通常のアドレッシングである。制御信号（転送（Ｔｒａｎｓｆｅｒ）および放電（Ｄｉｓｃｈａｒｇｅ））は、大域的に制御される別々の信号であり、これらの信号は記憶コンデンサ１４上の電荷を駆動コンデンサ３６に転送し、駆動コンデンサ３６は液晶（ＬＣ）セルを駆動する。デバイス上の追加のトランジスタ３２および３４とコンデンサ３６を加えることにより、この新しい回路を実現し、各転送後に記憶コンデンサ１４から適切に電流が放電されるように動作させる。プロセス製造技術が０．１ミクロン以下に向かって進歩しているので、構成要素の追加はそれほど問題にはならない。

【００１８】

図１の構成では、前述のように分離増幅器（ｉｓｏｌａｔｉｏｎ　ａｍｐｌｉｆｉｅｒ）を追加して液晶（ＬＣ）セルをメモリ素子から分離した。図３の本発明の追加実施形態では、第２の記憶セル（好ましくは記憶コンデンサ１４′）と、第２の増幅器（好ましくはトランジスタ１５′、１７′、１８′を含む差動増幅器１６′）と、２つの駆動セル間を高速レートで切り替えるための１対のトランジスタ（７２および７４）とを有する、第２のセル・ドライバ部分を追加する。また、第２の駆動セルは、図１の実施形態と同様に構成されたトランジスタ１２′およびトランジスタ１８′と抵抗器１９′および抵抗器２４′も備えることが好ましい。これにより、フレームを倍増することを必要とせずにフリッカを無くすことができる。また、これを用いて、セル上で利用可能な駆動電圧を増加させることもできる。

【００１９】

液晶オン・シリコン（ＬＣＯＳ）を駆動するための図３の実施形態の基本的な利点は、２つの別々の記憶素子および駆動回路を使用し、これらを切り替えて液晶（ＬＣ）セルを駆動することである。これは高速な切替え周波数を可能にし、それによりセルのフリッカ・レートは、人間の目で検出可能な周波数よりもずっと高い周波数になる。また、シリコン・バックプレーン（ｂａｃｋ　ｐｌａｎｅ）の所定の動作電圧でセル上の可能なＲＭＳ（Ｒｏｏｔ　Ｍｅａｎ　Ｓｑｕａｒｅ：平方自乗平均）電圧を増加させるのに役立つように、共通電極電圧（ＶＩＴＯ）を切り替えることも可能になる。

【００２０】

上側のセル（トランジスタ７２を使用する）は、「正」のフレーム中に液晶（ＬＣ）を駆動するための電圧を含み、下側のセル（トランジスタ７４を使用する）は、「負」のフレーム中に液晶（ＬＣ）を駆動するための電圧を含んでいる。セル上の正味ＤＣ電圧およびその結果生じる残像および信頼性の問題を回避するために、正と負のフレーム中での電圧はＶＩＴＯとバランスが取れていなければならない。ＶｄｄおよびＶｓｓは、ＣＭＯＳデバイスについての高い方（ｕｐｐｅｒ）と低い方（ｌｏｗｅｒ）の動作電圧である。Ｖｎｎは、差動増幅器のトランジスタを通る電流を調整するために設定され、増幅器の電力損失を制御する。Ｖ１およびＶ２は、どの増幅器が液晶セルを駆動しているかを決定する大

域的な切替え電圧である。図６に、静的ＶＩＴＯの場合のタイミング図を示す。図７に、切替え式ＶＩＴＯの場合のタイミング図を示す。

【００２１】

図６および図７を更に参照すると、これらのタイミング図は、図３における上側の記憶セル１４中の「正」のピクチャ・データ（Ｖ＋）と、下側の記憶セル１４′中の「負」のピクチャ・データ（Ｖ－）を反映している。図６の場合、ＶＩＴＯは切り替わらない。Ｖ１が、ハイ（高）に切り替わると（Ｖ２は、ロー（低））、トランジスタ７２がオンになり、Ｖ＋が液晶（ＬＣ）セルに加えられる。セル上の実効電圧は（Ｖ＋　－　ＶＩＴＯ）である。次の切替え時、Ｖ１はロー（低）に切り替わり、Ｖ２はハイ（高）に切り替わる。トランジスタ７４がオンになり、Ｖ－が液晶（ＬＣ）セルに加えられる。セル上の実効電圧は（ＶＩＴＯ　－　Ｖ－）である。

【００２２】

図７の場合、ＶＩＴＯは切り替わる。Ｖ１がハイ（高）に切り替わると（Ｖ２は、ロー（低））、トランジスタ７２がオンになり、Ｖ＋が液晶（ＬＣ）セルに加えられる。同時に、図７に示すようにＶＩＴＯがロー（低）に切り替わる（ＶＩＴＯ－）。この場合、液晶（ＬＣ）セル全体にわたる実効電圧は（Ｖ＋　－　ＶＩＴＯ－）である。次の切替え時には、Ｖ１はロー（低）に設定されてトランジスタ７２はオフになり、Ｖ２はハイ（高）に設定されてトランジスタ７４はオンになる。これはＶ－を、セルに加える。同時に、図７に示すように、ＶＩＴＯは、ハイ（高）に切り替わる（ＶＩＴＯ＋）。この場合、液晶（ＬＣ）セルにわたる実効電圧は（ＶＩＴＯ＋　－　Ｖ－）である。

【００２３】

Ｖ＋およびＶ－の最大値が、バックプレーン・プロセス（ｂａｃｋｐｌａｎｅ　ｐｒｏｃｅｓｓ）の最大電圧で固定されている場合は、図６のような固定値のＶＩＴＯは（Ｖ＋　＋　Ｖ－）／２でなければならない。図７のようにＶＩＴＯを切り替えることができる場合、ＶＩＴＯ－は、Ｖ－とすることができ、ＶＩＴＯ＋は、Ｖ＋とすることができる。従って、液晶（ＬＣ）セル上の最大実効電圧は、図６では（Ｖ＋　－　Ｖ－）／２だが、図７ではＶ＋　－　Ｖ－である。図７のタイミングは、アナログ・システム上で、大域スイッチＶ１およびＶ２によってすべてのセルが同時に更新される場合だけしか達成することができない。

【００２４】

通常、Ｖ１とＶ２で切り替える間の時間は、１または２ミリ秒とすべきである。これは、液晶（ＬＣ）材料とバックプレーンの特性との所定の組み合わせ、およびデバイスの応答時間に対して決定する必要がある。

【００２５】

この方式の不利な点は、多数のトランジスタを実装する必要があることである（おそらく１２個になる）。これは、２０ミクロン・ピクセルおよび０．３５ミクロン・プロセスを用いれば容易に実現可能である。より精緻なプロセス・ジオメトリを用いることにより、より小さなピクセルに対する同様の拡大・縮小も可能である。

【００２６】

次に図４を参照すると、前述の表示ドライバ１０または３０または７０を利用することのできる表示ユニット５０が示されている。表示ユニット５０は、行（ｒｏｗ）と列（ｃｏｌｕｍｎ）のマトリックス（ｍａｔｒｉｘ）に構成された複数の表示素子と、メモリ素子と、液晶セルとを備えることが好ましい。ドライバは、複数の電圧のうちの１つを、行と列のマトリックスのうちの少なくとも１つにある表示素子に切替え可能に出力することが好ましく、表示ユニットは、従来型デコーダ５１を備え、ドライバは、この従来型デコーダ５１によって制御される。ドライバは、記憶コンデンサと、記憶コンデンサと液晶セルとの間に結合された差動増幅器とを備えることができ、それにより差動増幅器は、記憶コンデンサと液晶セルとの間の分離を与える。ドライバは、デコーダ５１と、デコーダ５１の出力信号により開閉するように制御される複数の半導体スイッチとを備えることができる。図４に示すように、表示ユニット５０は、複数の行（走査）アドレス・ライン５６を

有する行駆動回路６０と、複数の列（データ）アドレス・ライン５８を有する列駆動回路６２とを備えることができる。

【００２７】

図５を参照すると、本発明による表示装置駆動方法２００を表すフロー・チャートが示されている。方法２００は、複数の駆動セルのうちの各駆動セル中で差動増幅器を使用してメモリ素子（記憶コンデンサなど）と液晶セルとの間の分離を与えるステップ２０２を含むことが好ましい。この分離は、第１のセル中で、第１の差動増幅器を使用して第１の記憶コンデンサと液晶セルとの間に与えられ、第２のセル中で、第２の差動増幅器を使用して第２の記憶コンデンサと液晶セルとの間に与えられることが好ましい。方法２００はまた、複数の駆動セル間を切り替えて液晶セルを駆動するステップ２０４を含むことが好ましく、１対のトランジスタが、第１と第２の駆動セル間を切り替える機能を実行することが好ましい。ステップ２０８で更に、フレームを倍増せずにフリッカを無くすステップを与えることができる。方法２００は更に、液晶素子のアレイ全体を同時に更新するステップ２１６、および／または、前のフレームから変化したメモリ・セルだけを更新するステップ２１８を含むこともできる。方法２００の追加の利点として、ライン間走査アーティファクトを表示することなくメモリ・アレイをインタレース・モードで駆動するステップ２２０、および／または、共通電極電圧をフレーム間で変調して、必要とされる液晶駆動電圧を低減するステップ２２２を含むこともできる。

【００２８】

本明細書に開示する実施形態に関連して本発明について述べたが、以上の記述は本発明を例示するものであり、特許請求の範囲で定める本発明の範囲を限定するものではないことを理解されたい。

【図面の簡単な説明】

【図１】

本発明による液晶セル・ドライバのブロック図である。

【図２】

本発明による別の液晶セル・ドライバのブロック図である。

【図３】

本発明による切替え式液晶セル・ドライバを利用する表示ユニットのブロック図である。

【図４】

本発明による液晶セル・ドライバを利用する表示ユニットのブロック図である。

【図５】

本発明による表示装置駆動方法を示すフロー・チャートである。

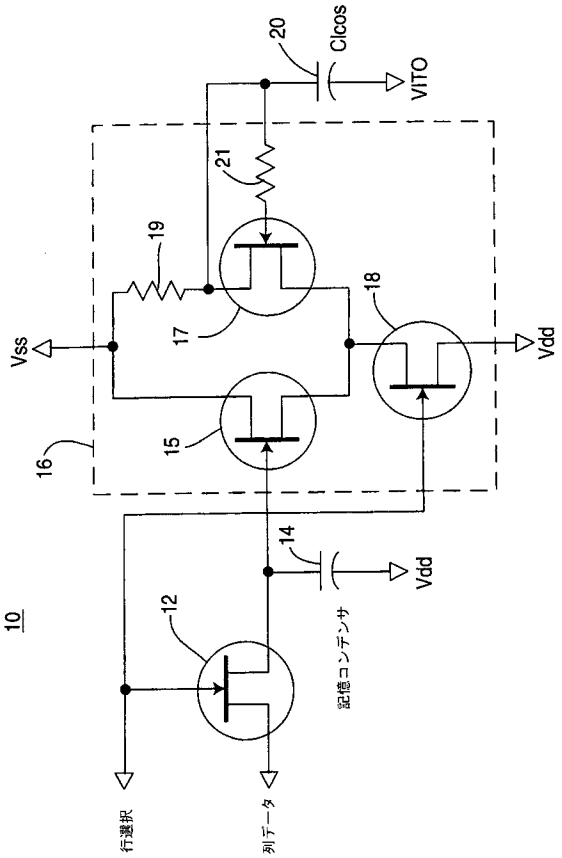
【図６】

本発明による静的ＶＩＴＯの場合のタイミング図である。

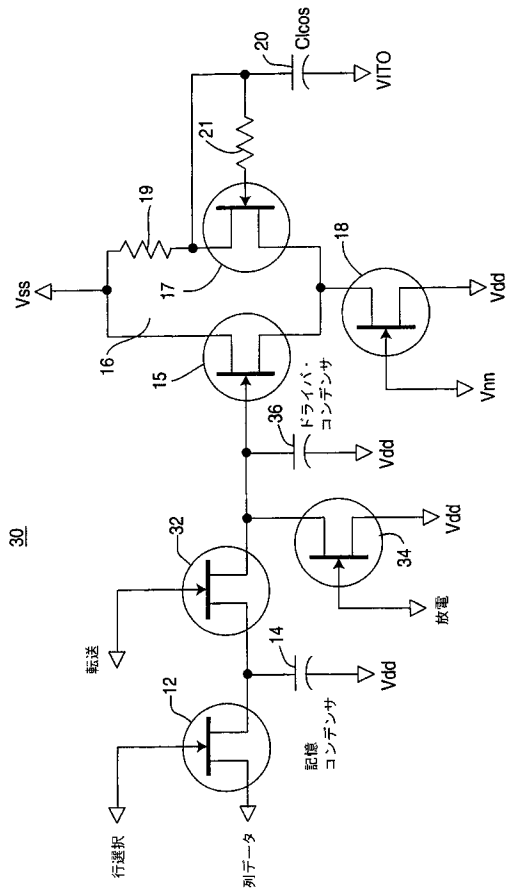
【図７】

本発明による切替え式ＶＩＴＯの場合のタイミング図である。

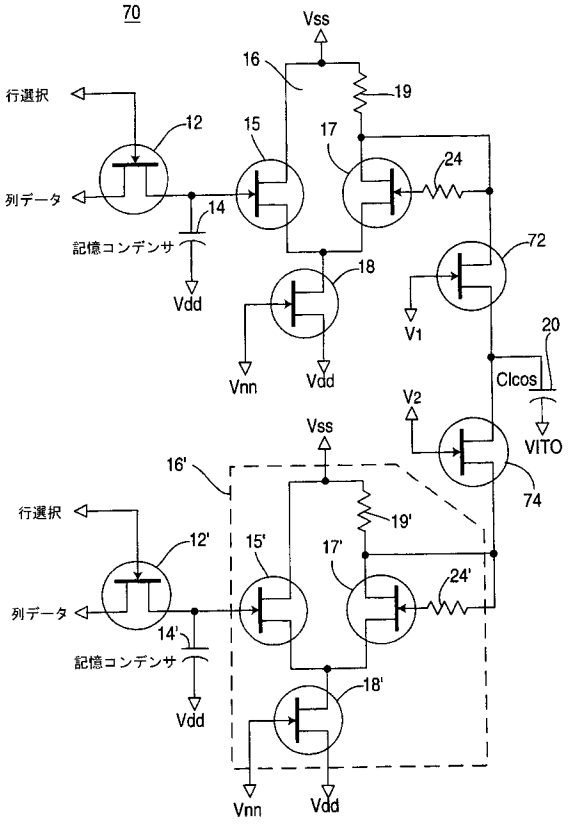
【図１】


20
Clcos
VITO
21
19
18
17
Vss
Vdd
16
15
14
12
Vdd
記憶コンデンサ
10
行選択
列データ

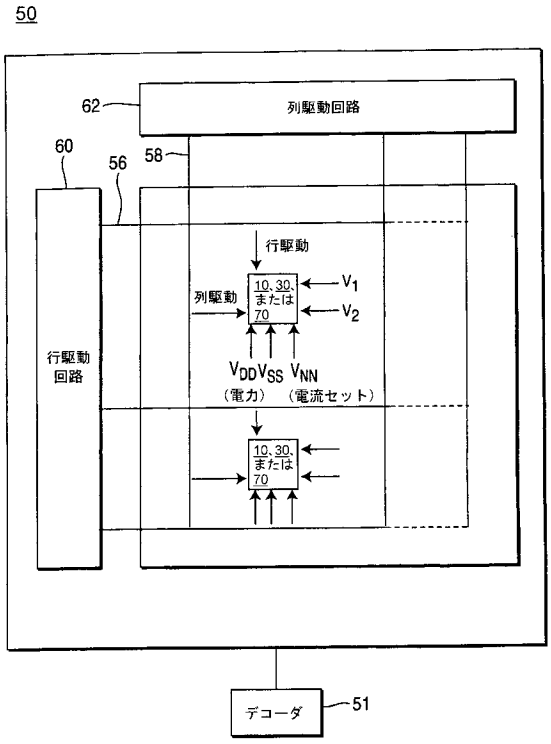
【図２】


20
Clcos
VITO
21
19
18
17
Vss
Vdd
16
15
ドライバ・コンデンサ
Vnn
36
Vdd
30
32
Vdd
34
放電
転送
14
Vdd
12
記憶コンデンサ
行選択
列データ

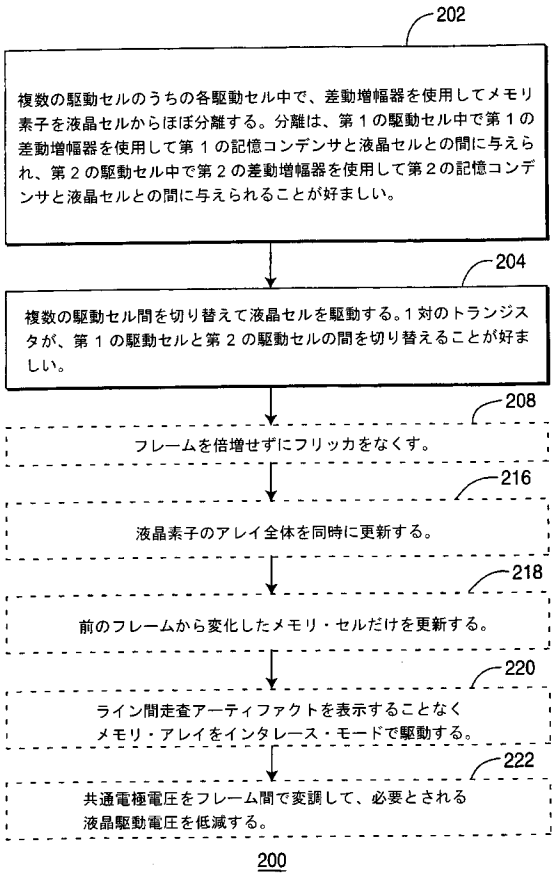
【図３】


70
Vss
16
19
行選択
12
15
17
24
列データ
14
記憶コンデンサ
Vdd
18
72
V1
Vnn
Vdd
20
Clcos
V2
Vss
VITO
74
16'
行選択
19'
12'
15'
17'
24'
列データ
14'
記憶コンデンサ
18'
Vdd
Vnn
Vdd

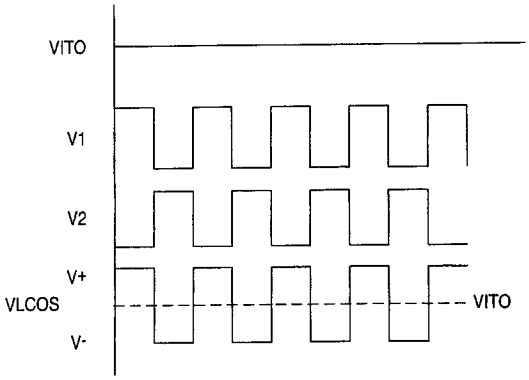
【図４】


50
62
列駆動回路
60
56
58
行駆動
列駆動
10, 30, または 70
V1
V2
行駆動回路
VDD VSS VNN
（電力）
（電流セット）
10, 30, または 70
デコーダ
51

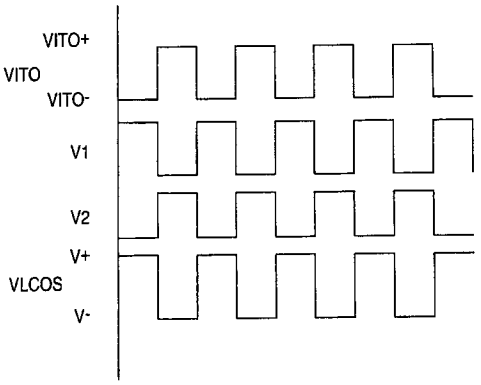
【図５】


202
複数の駆動セルのうちの各駆動セル中で、差動増幅器を使用してメモリ素子を液晶セルからほぼ分離する。分離は、第１の駆動セル中で第１の差動増幅器を使用して第１の記憶コンデンサと液晶セルとの間に与えられ、第２の駆動セル中で第２の差動増幅器を使用して第２の記憶コンデンサと液晶セルとの間に与えられることが好ましい。
204
複数の駆動セル間を切り替えて液晶セルを駆動する。１対のトランジスタが、第１の駆動セルと第２の駆動セルの間を切り替えることが好ましい。
208
フレームを倍増せずにフリッカをなくす。
216
液晶素子のアレイ全体を同時に更新する。
218
前のフレームから変化したメモリ・セルだけを更新する。
220
ライン間走査アーティファクトを表示することなくメモリ・アレイをインタレース・モードで駆動する。
222
共通電極電圧をフレーム間で変調して、必要とされる液晶駆動電圧を低減する。
200

【図６】


VITO
V1
V2
V+
VLCOS
VITO
V-

【図７】


VITO+
VITO
VITO-
V1
V2
V+
VLCOS
V-

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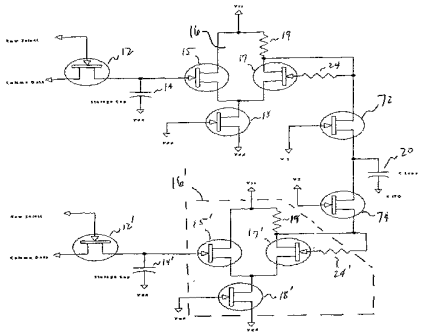
(54) Title: SWITCHED AMPLIFIER DRIVE CIRCUIT FOR LIQUID CRYSTAL DISPLAYS



(57) Abstract: A cell driver (70) for a display unit (50) having a memory element and a liquid crystal cell among a plurality of liquid crystal cells includes a first storage capacitor (14) and a first differential amplifier (16) selectively coupled between the first storage capacitor and the liquid crystal cell forming a first drive circuit. The cell driver also includes a second storage capacitor (14') and a second differential amplifier (16') coupled between the second storage capacitor and the liquid crystal cell forming a second drive circuit. A switching mechanism (72 and 74) is used for switching the liquid crystal cell between the first and second drive circuits.

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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

SWITCHED AMPLIFIER DRIVE CIRCUIT FOR LIQUID CRYSTAL DISPLAYS

Background of the Invention

Field of the Invention

This invention relates to the field of video systems utilizing a liquid crystal display (LCD) or liquid crystal on silicon (LCOS), and in particular, to a switched driver circuit for such displays.

Description of Related Art

Liquid crystal on silicon (LCOS) can be thought of as one large liquid crystal formed on a silicon wafer. The silicon wafer is divided into an incremental array of tiny plate electrodes. A tiny incremental region of the liquid crystal is influenced by the electric field generated by each tiny plate and the common plate. Each such tiny plate and corresponding liquid crystal region are together referred to as a cell of the imager. Each cell corresponds to an individually controllable pixel. A common plate electrode is disposed on the other side of the liquid crystal (LC). The drive voltages are supplied to plate electrodes on each side of the LCOS array. Each cell, or pixel, remains lighted with the same intensity until the input signal is changed, thus acting as a sample and hold. Each set of common and variable plate electrodes forms an imager. One imager is provided for each color, in this case, one imager each for red, green and blue.

It is typical to drive the imager of an LCOS display with a frame-doubled signal to avoid 30 Hz flicker, by sending first a normal frame in which the voltage at the electrodes associated with each cell is positive with respect to the voltage at the common electrode (positive picture) and then an inverted frame in which the voltage at the electrodes associated with each cell is negative with respect the voltage at the common electrode (negative picture) in response to a given input picture. The generation of positive and negative pictures ensures that each pixel will be written with a positive electric field followed by a negative

electric field. The resulting drive field has a zero DC component, which is necessary to avoid the image sticking, and ultimately, permanent degradation of the imager. It has been determined that the human eye responds to the average value of the brightness of the pixels produced by these positive and negative pictures.

The present state of the art in LCOS requires the adjustment of the common-mode electrode voltage, denoted VITO, to be precisely between the positive and negative field drive for the LCOS. The subscript ITO refers to the material indium tin oxide. The average balance is necessary in order to minimize flicker, as well as to prevent a phenomenon known as image sticking.

In the current art, the LCOS drive cell looks much like a conventional Active Matrix LCD driver. This does not work well, due to the various artifacts discussed in the literature. The main causes are parasitic capacitance cross-talk, residual voltage in the LC cell, and voltage droop of the LC, due to ionic leakage and bulk resistivity of the LC material. Mainly this has been solved by: 1. Increasing the cell capacitance (limited by physical area), 2. Changing to higher resistivity LC materials (limits flexibility and response time), 3. Increasing the frame scan rate to more than 60Hz (expensive, and costs more bandwidth). 4. Strongly controlling the temperature of the device, to maintain high voltage holding ratio (VHR).

The main cause for all of the above issues is that the available charge is only transferred to the LC cell once per frame. In a display with a million pixels, this limits the available power and doesn't allow for any closed-loop check that the desired voltage has actually been achieved on the pixel electrode. Additionally, the issues of flicker, drive voltage, and image retention have been addressed in various ways for digital drive LCOS displays, but such methods fail to provide a solution to the problem in analog systems due to the need for continuous updating. Thus, a need exists for a display driver that provides adequate isolation between a storage capacitor and a liquid crystal cell and further eliminates flicker without the need for frame doubling.

Brief Summary of the Invention

In a first aspect of the present invention, a display driver for a display unit having a memory and a liquid crystal cell among a plurality of liquid crystal displays comprises a first drive circuit coupled to a first memory element of the liquid crystal cell, a second drive circuit coupled to a second memory element of the liquid crystal cell, and a switching arrangement for switching the liquid crystal cell between the first and the second drive circuits.

In a second aspect of the present invention, a display driver among an array of array drivers for a display unit having a corresponding array of liquid crystal cells comprises a first storage capacitance and a first amplifier selectively coupled between the first storage capacitance and the liquid crystal cell forming a first drive circuit, a second storage capacitance and a second amplifier coupled between the second storage capacitance and the liquid crystal cell forming a second drive circuit, and a switching arrangement for switching the first and second drive circuits.

In a third aspect of the present invention, a method of driving a LCD/LCOS display comprises the steps of isolating a storage capacitance from a liquid crystal cell using a differential amplifier in each drive cell among a plurality of drive cells and switching among the plurality of drive cells to drive the liquid crystal cell.

Brief Description of the Drawings

FIG. 1 is a block diagram of a liquid crystal cell driver in accordance with the present invention.

FIG. 2 is a block diagram of another liquid crystal cell driver in accordance with the present invention.

FIG. 3 is a block diagram of a display unit utilizing a switching liquid crystal cell driver in accordance with the present invention.

FIG. 4 is a block diagram of a display unit utilizing a liquid crystal cell driver in accordance with the present invention.

FIG. 5 is a flow chart illustrating a method of driving a display in accordance with the present invention.

FIG. 6 is a timing diagram for static Vito in accordance with the present invention.

FIG. 7 is a timing diagram for a switched Vito in accordance with the present invention.

Detailed description of the Preferred Embodiments

In order to overcome the problems described above, it is proposed to add an amplifier such as a differential amplifier 16 between the internal storage capacitance (14), and the LC cell (20) as shown in FIG. 1. In other words, a drive amplifier is added to the driving LC cell. This adds isolation between the storage capacitor and the LC cell. The added current drive capability ensures that the voltage on the pixel will rapidly become that desired. It also allows for very low leakage current from the storage capacitor (FET has very high input impedance), and allows for a continuous refresh of the voltage on the LC, which eliminates the 'droop' problem, as well as the residual voltaic potential stored in the cell. This should improve both the flicker issue, as well as the 'image sticking' problem which is associated with the inability to achieve DC balance in the cell. It should also allow the cell to work well even at somewhat elevated temperatures.

The disadvantage of this technique is that it increases the DC current through the liquid crystal cell. This disadvantage can be overcome in part by gating the current source in the bottom of the differential amplifier. This can use the 'pixel select' or 'row select' bit in the device (see FIG.1). In this way, a periodic refresh of the voltage can be achieved, while reducing the power consumption by 1/nrow, where nrow is the number of rows in the device. Since heating is uniform, this gating in some situations may not be needed.

A typical implementation in CMOS is shown in FIG 1. The components are schematic representations, and alternate configurations can be used without loss of generality. The key points are the amplifier 16, which applies a closed loop correction voltage to the LC cell, and the gated current source which allows reduction of power consumption.

Typically this circuit could be implemented with 3 transistors, which can be placed under the liquid crystal cell in an LCOS display device. In the arrangement of FIG. 1, the amplifier 16 decouples the LC cell from the memory element. FIG. 1 illustrates a liquid crystal cell driver 10 for a liquid crystal display. The liquid crystal cell driver preferably comprises a plurality of transistors (12, 15, 17, and 18) coupled to each other as shown in FIG. 1, a storage capacitance such as a storage capacitor 14, and a plurality of resistors 19 and 21. Preferably, three (3)transistors, such as transistors 15, 17 and 18 form the amplifier 16, preferably in the form of a differential amplifier which serves as the buffer or isolation amplifier. The differential amplifier 16 is preferably comprised of N-Channel transistors serving as an output to the liquid crystal cell. Additionally, the respective source electodes of the transistors of the differential amplifier are driven by a current source such as an N-Channel transistor such as transistor 18 that may be gated. This current mirror arrangement ensures a predetermined voltage on a given pixel. The differential amplifier 16 is coupled between the storage capacitor 14 and provides isolation between the storage capacitor 14 and a liquid crystal cell or pixel.

The arrangement of FIG. 2 adds a global switch element (32) to transfer data from the storage element to the driver. This allows for increased pixel drive for the same circuit operating voltages, and reduces image retention and flicker by allowing for inversion of the pixel drive voltage and the ITO transparent conductive electrode from frame to frame. Referring to FIG. 2, another liquid crystal cell driver 30 is shown similar to the liquid crystal cell driver 10 of FIG. 1. In addition to the elements previously recited with respect to cell driver 10, cell driver 30 further comprises a global switch element 32 in the form of a transistor coupled between the storage capacitor 14 and the differential amplifier 16. The

global switch element transfers data from the memory cell to a driver capacitor 36 of the display driver.

The problem of flicker has been addressed by many mechanisms in the past. The issue of drive voltage and image retention has been addressed in digital drive LCOS displays. For analog systems, drive voltage and image retention issues can be addressed similarly, due to the need for continuous updating.

The main benefit of the technique disclosed herein is to separate the driver capacitor 36 from the storage capacitor 14. This separation as shown in FIG. 2 allows for updating all the cells of entire LC array at one time if desired. The benefit of this is two-fold. First, this separation (with further pre-processing to determine which LC cells have changed from frame to frame) also allows for updating of only the cells in the LC array that have changed from a prior frame. In other words, the contents of the storage capacitor 14 can be changed without instantaneously changing the display content on the LC cells. This greatly reduces the data rate needed for static pictures. It also allows for the possibility of driving the display in an interlaced mode without displaying interline scanning artifacts. In a system which is interlaced, normally odd lines are written on a first scan, and even lines are written on a second scan. This scanning scheme produces the artifact known as 'interline flicker'. This even happens for data which is not intrinsically interlaced, such as film. The reason for "interline flicker" is that the even lines from one frame are displayed at the same time that the odd lines from the previous frame are displayed. Any portion of the frame which changed will show an interline flicker. With the present invention, a display having an array of storage capacitors (14) corresponding to an array of LC cells would be updated just as normal (even lines followed by odd lines), except that the entire LC array would then be updated once the storage array has been filled. Thus, lines from different fames are never displayed simultaneously. The second benefit of this technique is that it allows the common electrode voltage to be modulated from frame to frame. This modulation increases the effective electric field which can be applied to the LC cell for a given operating voltage of the

driver circuit. This is a significant advantage, as finer process geometry will reduce the maximum allowed driving voltage. The benefits described above only occur when the pixels are all updated at once. The simultaneous updating of the pixels can only be done if the storage array (array of storage capacitors (14)) is separated from the driver array (array of driver capacitors (36)).

The technique can most simply be implemented with the circuit described in FIG. 1, with a modification as shown in FIG. 2. The voltage Vnn of FIG. 2 is a static voltage which controls the current source for the transistors 15 and 17. The Row and Column address are normal addressing for an active matrix display. The control signals (Transfer and Discharge) are separate globally controlled signals which transfer the charge on the storage capacitor 14 to the drive capacitor 36, which drives the LC cell. The additional transistors 32 and 34 and capacitor 36 on the device are added to implement the new circuit and operationally allows for the adequate discharge of current from the storage capacitor 14 after each transfer. The additional components should not be significant as process fabrication technology moves forward towards 0.1 microns and below.

In the arrangement of FIG. 1, an isolation amplifier was added to decouple the LC cell from the memory element, as explained before. The additional embodiment of the invention of FIG. 3, adds a second cell driver portion having a second storage cell (preferably storage capacitor 14') and amplifier (preferably differential amplifier 16' including transistors 15' and 17' and 18') and a pair of transistors (72 and 74) to switch between the two drive cells at a high rate of speed. The second drive cell also preferably comprises transistors 12' and 18' and resistors 19' and 24' arranged similarly to the embodiment of FIG. 1.) This eliminates flicker without the need for frame doubling. It can also be used to increase the drive voltage available on the cell.

The basic advantage of the embodiment of FIG. 3 for driving LCOS is that it uses two separate storage elements and drive circuits that are switched to drive the LC cell. This allows a fast switching frequency, which makes the flicker rate of the cell much above frequencies detectable by the human eye. It

also allows for the possibility of switching the common electrode voltage (Vito) to help to increase the possible RMS voltage on the cell for a given operating voltage of the silicon back plane.

The upper cell (using transistor 72) contains the voltage to drive the LC during the 'positive' frame, the lower cell (using transistor 74) contains the voltage to drive the LC in the 'negative' frame. The voltage during the positive and negative frames must be balanced with Vito in order to avoid a net DC voltage on the cell, and resultant imager retention and reliability issues. VDD and VSS are the upper and lower operating voltages for the CMOS devices. VNN is set to regulate the current through the transistors of the differential amplifiers, and controls the power dissipation of the amplifier. V1 and V2 are global switching voltages which determine which amplifier is driving the Liquid Crystal cell. A timing diagram for a static Vito is shown in FIG. 6. A timing diagram for switched Vito is shown in FIG. 7.

Further referring to FIGs. 6 and 7, these timing diagrams reflect the 'positive' picture data (V+) in the upper storage cell (14) in FIG. 3, and the 'negative' picture data (V-) in the lower storage cell (14'). In the case of FIG. 6, Vito is not switched. When V1 is switched high (and V2 being low), the transistor 72 is turned on, and V+ is applied to the LC cell. The effective voltage on the cell is (V+ - Vito). At the next switching time, V1 is switched low, and V2 is switched high. The transistor 74 is turned on, and V- is applied to the LC cell. The effective voltage on the cell is (Vito - V-).

In the case of FIG. 7, Vito is switched. When V1 is switched high (and V2 being low), the transistor 72 is turned on, and V+ is applied to the LC cell. Simultaneously, Vito is switched to low (Vito-), as shown in FIG. 7. The effective voltage across the LC cell is then (V+ - Vito-). At the next switching time, V1 is set to low to turn off transistor 72, and switch V2 high to turn on transistor 74. This applies V- to the cell. Simultaneously, Vito is switched to high (Vito+), as shown in FIG. 7. The effective voltage across the LC cell is then (Vito+ - V-).

If the maximum value of V+ and V- is fixed by the maximum voltage of the backplane process, then a fixed value of Vito as in FIG. 6 must be (V+ + V-)/2. If Vito can be switched, as in FIG. 7, Vito- can be V-, and Vito+ can be V+. Thus, the maximum effective voltage on the LC cell is (V+ - V-)/2 for FIG. 6, but V+ - V- for FIG. 7. The timing of FIG. 7 can ONLY be achieved on an analog system if all of the cells are updated simultaneously by the global switches V1 and V2.

Typically the time between V1 and V2 switching should be 1 or 2 msec. This will need to be determined for a given set of LC materials and the characteristics of the back plane, and response time of the devices.

The obvious detriment of this scheme is that it requires a large number of transistors to implement (perhaps as many as 12). This should be easily possible with a 20 micron pixel and a .35 micron process. Similar scaling on smaller pixels is possible with finer process geometry.

Now referring to FIG. 4, a display unit 50 is shown that can utilize the display drivers 20 or 30 or 70 as previously described above. The display unit 50 preferably includes a plurality of display elements arranged in a matrix of rows and columns and a memory element and a liquid crystal cell. The driver preferably switchably outputs one of a plurality of voltages to the display elements on at least one of the matrix of rows and columns, the display unit including a conventional decoder 51 and the driver controlled by the conventional decoder 51. The driver can include a storage capacitor and a differential amplifier coupled between the storage capacitor and the liquid crystal cell, whereby the differential amplifier provides isolation between the storage capacitor and the liquid crystal cell. The driver can include a decoder and a plurality of semiconductor switched controlled to be opened or closed by an output signal of the decoder 51. As shown in FIG. 4, the display unit 50 can include a row drive circuit having a plurality of row (scanning) address lines 56 and a column drive circuit 62 having a plurality of column (data) address lines 58.

Referring to FIG. 5, a flow chart is shown illustrating a method 200 of driving a display in accordance with the present invention. The method 200

preferably comprises the step 202 of providing isolation between memory elements (such as a storage capacitor) and a liquid crystal cell using a differential amplifier in each drive cell among a plurality of drive cells. Preferably, the isolation is provided between a first storage capacitor and the liquid crystal cell using a first differential amplifier in a first cell and between a second storage capacitor and the liquid crystal cell using a second differential amplifier in a second cell. The method 200 also preferably comprises the step 204 of switching among the plurality of drive cells to drive the liquid crystal cell, where preferably a pair of transistors performs the function of switching between the first and second drive cells. Step 208 can further provide the step of eliminating flicker without frame doubling. The method 200 may further comprise the step 216 of updating an entire array of liquid crystal elements simultaneously and/or the step 218 of updating only a memory cell that has changed from a previous frame. Additional benefits of the method 200 may include the step 220 of driving a memory array in an interlaced mode without displaying interline scanning artifacts and/or the step 222 of modulating a common electrode voltage from frame to frame to reduce a required liquid crystal drive voltage.

Although the present invention has been described in conjunction with the embodiments disclosed herein, it should be understood that the foregoing description is intended to illustrate and not limit the scope of the invention as defined by the claims.

Claims

1. A display unit having an array of liquid crystal cells, comprising:

an array of display drivers, a given display driver being associated with a given liquid crystal cell and including:

a first storage capacitance and a first amplifier selectively coupled between the first storage capacitance and the given liquid crystal cell forming a first drive circuit;

a second storage capacitance and a second amplifier coupled between the second storage capacitance and the given liquid crystal cell forming a second drive circuit; and

a switching arrangement for switching the first and second drive circuits.

2. The display driver of claim 1, wherein the first amplifier and the second amplifier are both differential amplifiers.

3. The display driver of claim 2, wherein the differential amplifier comprises a pair of N-Channel transistors having respective drain electrodes coupled and serving as an output to the liquid crystal cell.

4. The display driver of claim 1, wherein the each of said first and second drive circuits further comprises a global switch element coupled between the respective storage capacitance and the amplifier, wherein the global switch element transfers data from the storage capacitance to one of the first and second drive circuits.

5. The display driver of claim 1, wherein the switching mechanism comprises a first transistor driven by a first global switching voltage and a second transistor driven by a second global switching voltage.

6. A display driver for a given liquid crystal cell of an array of liquid crystal cells, comprising:

a first drive circuit coupled to a first memory element of the given liquid crystal cell;

at least a second drive circuit coupled to a second memory element of the given liquid crystal cell; and

a switching arrangement for switching the liquid crystal cell between the first and at least the second drive circuits.

7. The display driver of claim 6, wherein each of the first and the second drive circuits comprise differential amplifiers comprising a pair of N-Channel transistors having respective source electrodes coupled to a current source and serving as an isolation amplifier to the liquid crystal cell.

8. The display driver of claim 6, wherein each of the first and the second drive circuits comprise differential amplifier comprising a pair of N-Channel transistors having respective sources coupled to a current source.

9. The display driver of claim 6, wherein the switching mechanism comprises a first transistor driven by a first global switching voltage and a second transistor driven by a second global switching voltage.

10. The display driver of claim 6, wherein the display driver further comprises a global switching element which is coupled between a storage capacitor and a differential amplifier and used for reducing image retention and flicker.

11. The display driver of claim 6, wherein the display driver updates an entire array of liquid crystal arrays elements simultaneously.

12. The display driver of claim 6, wherein the display driver updates only a memory cell that has changed from a previous frame.

13. The display driver of claim 6, wherein the display driver drives a memory array in an interlaced mode without displaying interline scanning artifacts.

14. A method of driving a LCD/LCOS display, comprising the steps of:

providing isolation between a storage capacitance and a liquid crystal cell using a differential amplifier in each drive cell among a plurality of drive cells;

switching among the plurality of drive cells to drive the liquid crystal cell.

15. The method of claim 14, wherein the step of providing further comprises the step of providing in a first drive cell isolation between a first storage capacitance and the liquid crystal cell using a first differential amplifier and providing in a second drive cell isolation between a second storage capacitance and the liquid crystal cell using a second differential amplifier.

16. The method of claim 15, wherein the step of switching further comprises the step of switching between the first drive cell and the second drive cell using a pair of transistors to switch between the first drive cell and the second drive cell.

17. The method of claim 15, wherein the method further comprises the step of eliminating flicker without frame doubling.

18. The method of claim 14, wherein the method further comprises the step of updating an entire array of liquid crystal elements simultaneously.

19. The method of claim 14, wherein the method further comprises the step of updating only a memory cell that has changed from a previous frame.

20. The method of claim 14, wherein the method further comprises the step of driving a memory array in an interlaced mode without displaying interline scanning artifacts.

21. The method of claim 14, wherein the method further comprises the step of modulating a common electrode voltage from frame to frame to reduce a required liquid crystal drive voltage.

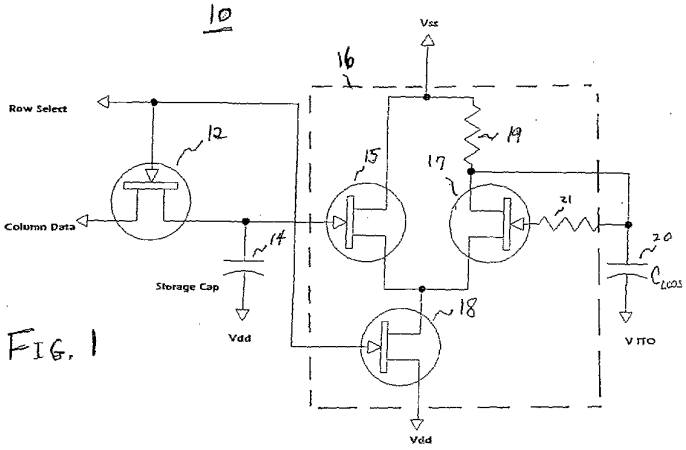

10
16
Vss
Row Select
12
15
19
17
21
Column Data
14
20
Storage Cap
Vdd
18
VITO
Vdd

FIG. 1

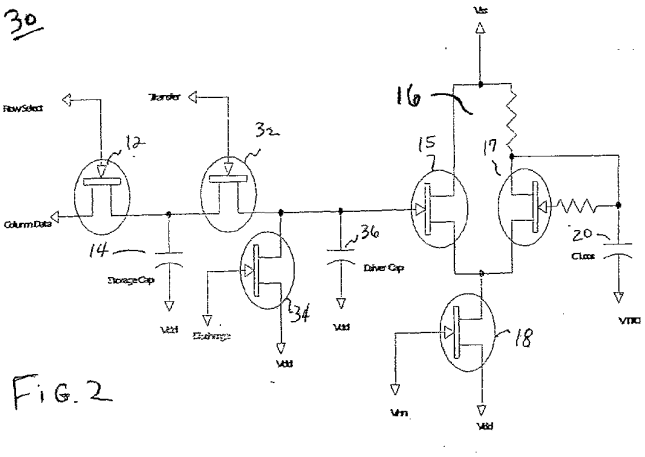

30
RowSelect
Reorder
12
32
16
15
17
ColumnData
14
36
20
StorageCap
DriverCap
Close
34
18
Vdd
Vm
VPIX

FIG. 2

70 FIG. 3

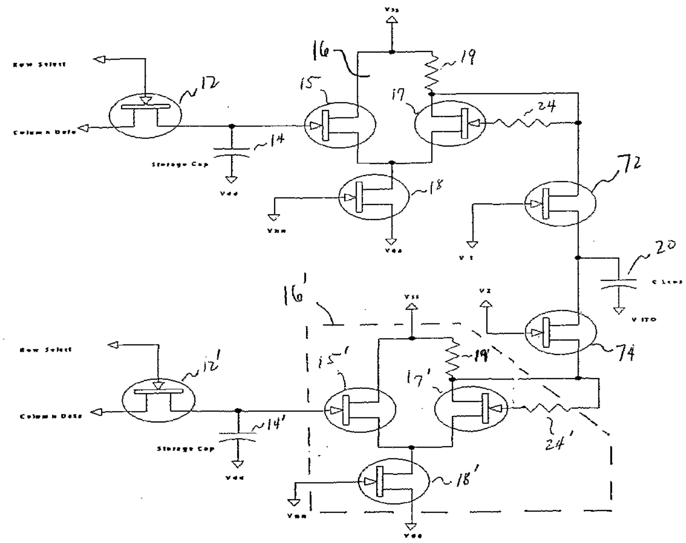


FIG. 4

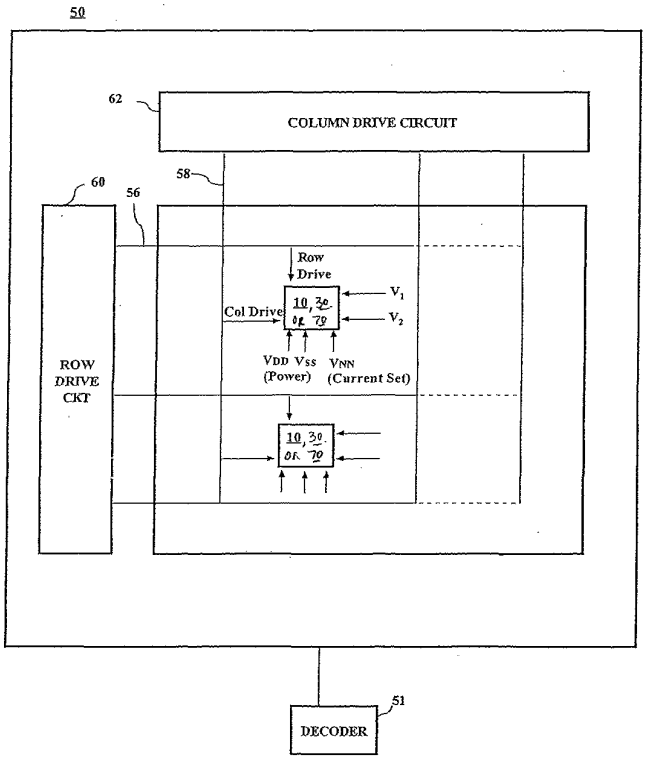
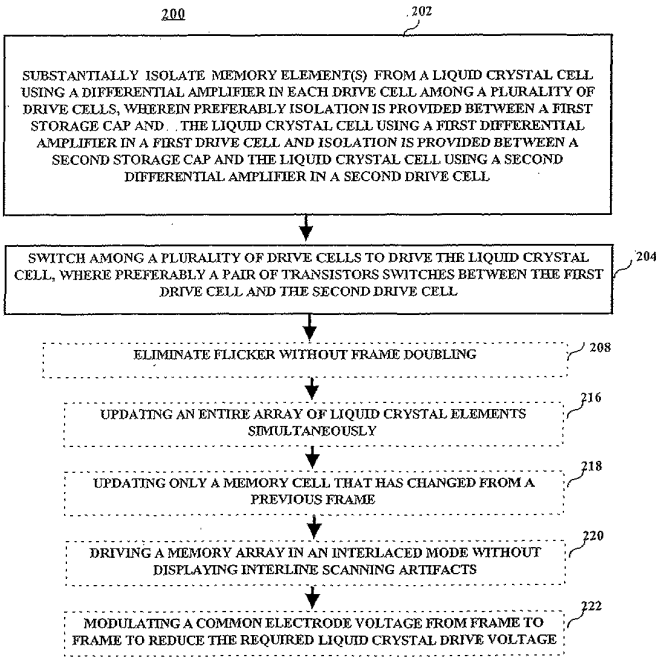

50
62
COLUMN DRIVE CIRCUIT
60
58
56
Row Drive
Col Drive
10, 30 or 70
V1
V2
VDD Vss VNN
(Power) (Current Set)
ROW DRIVE CKT
10, 30 or 70
51
DECODER

FIG. 5


200
202
SUBSTANTIALLY ISOLATE MEMORY ELEMENT(S) FROM A LIQUID CRYSTAL CELL USING A DIFFERENTIAL AMPLIFIER IN EACH DRIVE CELL AMONG A PLURALITY OF DRIVE CELLS, WHEREIN PREFERABLY ISOLATION IS PROVIDED BETWEEN A FIRST STORAGE CAP AND . THE LIQUID CRYSTAL CELL USING A FIRST DIFFERENTIAL AMPLIFIER IN A FIRST DRIVE CELL AND ISOLATION IS PROVIDED BETWEEN A SECOND STORAGE CAP AND THE LIQUID CRYSTAL CELL USING A SECOND DIFFERENTIAL AMPLIFIER IN A SECOND DRIVE CELL
SWITCH AMONG A PLURALITY OF DRIVE CELLS TO DRIVE THE LIQUID CRYSTAL CELL, WHERE PREFERABLY A PAIR OF TRANSISTORS SWITCHES BETWEEN THE FIRST DRIVE CELL AND THE SECOND DRIVE CELL
204
ELIMINATE FLICKER WITHOUT FRAME DOUBLING
208
UPDATING AN ENTIRE ARRAY OF LIQUID CRYSTAL ELEMENTS SIMULTANEOUSLY
216
UPDATING ONLY A MEMORY CELL THAT HAS CHANGED FROM A PREVIOUS FRAME
218
DRIVING A MEMORY ARRAY IN AN INTERLACED MODE WITHOUT DISPLAYING INTERLINE SCANNING ARTIFACTS
220
MODULATING A COMMON ELECTRODE VOLTAGE FROM FRAME TO FRAME TO REDUCE THE REQUIRED LIQUID CRYSTAL DRIVE VOLTAGE
222

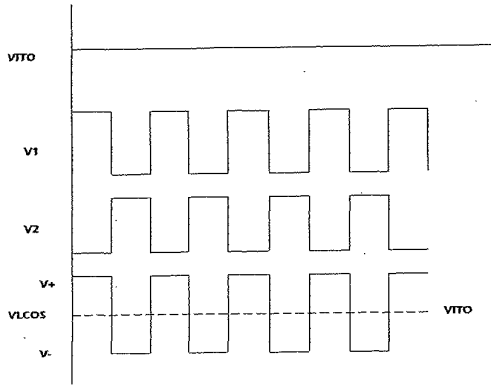


FIG. 6

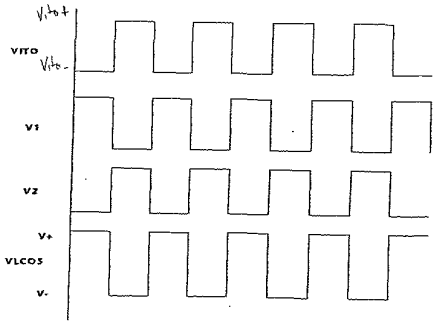


FIG. 7

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(74) Agents: TRIPOLI, Joseph, S. et al.; Thomson multimedia Licensing Inc., P.O. Box 5312, Princeton, NJ 08540 (US).

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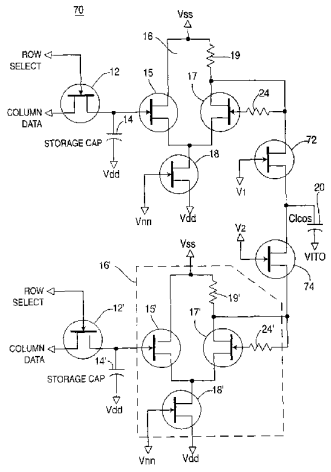
(54) Title: SWITCHED AMPLIFIER DRIVE CIRCUIT FOR LIQUID CRYSTAL DISPLAYS



(57) Abstract: A cell driver (70) for a display unit (50) having a memory element and a liquid crystal cell among a plurality of liquid crystal cells includes a first storage capacitor (14) and a first differential amplifier (16) selectively coupled between the first storage capacitor and the liquid crystal cell forming a first drive circuit. The cell driver also includes a second storage capacitor (14') and a second differential amplifier (16') coupled between the second storage capacitor and the liquid crystal cell forming a second drive circuit. A switching mechanism (72 and 74) is used for switching the liquid crystal cell between the first and second drive circuits.

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Published:
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Date of publication of the amended claims: 20 March 2003

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

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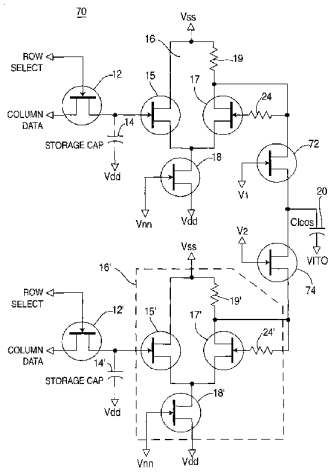
(54) **Title:** SWITCHED AMPLIFIER DRIVE CIRCUIT FOR LIQUID CRYSTAL DISPLAYS



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SWITCHED AMPLIFIER DRIVE CIRCUIT FOR LIQUID CRYSTAL DISPLAYS

Background of the Invention

Field of the Invention

This invention relates to the field of video systems utilizing a liquid crystal display (LCD) or liquid crystal on silicon (LCOS), and in particular, to a switched driver circuit for such displays.

Description of Related Art

Liquid crystal on silicon (LCOS) can be thought of as one large liquid crystal formed on a silicon wafer. The silicon wafer is divided into an incremental array of tiny plate electrodes. A tiny incremental region of the liquid crystal is influenced by the electric field generated by each tiny plate and the common plate. Each such tiny plate and corresponding liquid crystal region are together referred to as a cell of the imager. Each cell corresponds to an individually controllable pixel. A common plate electrode is disposed on the other side of the liquid crystal (LC). The drive voltages are supplied to plate electrodes on each side of the LCOS array. Each cell, or pixel, remains lighted with the same intensity until the input signal is changed, thus acting as a sample and hold. Each set of common and variable plate electrodes forms an imager. One imager is provided for each color, in this case, one imager each for red, green and blue.

It is typical to drive the imager of an LCOS display with a frame-doubled signal to avoid 30 Hz flicker, by sending first a normal frame in which the voltage at the electrodes associated with each cell is positive with respect to the voltage at the common electrode (positive picture) and then an inverted frame in which the voltage at the electrodes associated with each cell is negative with respect the voltage at the common electrode (negative picture) in response to a given input picture. The generation of positive and negative pictures ensures that each pixel will be written with a positive electric field followed by a negative

electric field. The resulting drive field has a zero DC component, which is necessary to avoid the image sticking, and ultimately, permanent degradation of the imager. It has been determined that the human eye responds to the average value of the brightness of the pixels produced by these positive and negative pictures.

The present state of the art in LCOS requires the adjustment of the common-mode electrode voltage, denoted VITO, to be precisely between the positive and negative field drive for the LCOS. The subscript ITO refers to the material indium tin oxide. The average balance is necessary in order to minimize flicker, as well as to prevent a phenomenon known as image sticking.

In the current art, the LCOS drive cell looks much like a conventional Active Matrix LCD driver. This does not work well, due to the various artifacts discussed in the literature. The main causes are parasitic capacitance cross-talk, residual voltage in the LC cell, and voltage droop of the LC, due to ionic leakage and bulk resistivity of the LC material. Mainly this has been solved by: 1. Increasing the cell capacitance (limited by physical area), 2. Changing to higher resistivity LC materials (limits flexibility and response time), 3. Increasing the frame scan rate to more than 60Hz (expensive, and costs more bandwidth). 4. Strongly controlling the temperature of the device, to maintain high voltage holding ratio (VHR).

The main cause for all of the above issues is that the available charge is only transferred to the LC cell once per frame. In a display with a million pixels, this limits the available power and doesn't allow for any closed-loop check that the desired voltage has actually been achieved on the pixel electrode. Additionally, the issues of flicker, drive voltage, and image retention have been addressed in various ways for digital drive LCOS displays, but such methods fail to provide a solution to the problem in analog systems due to the need for continuous updating. Thus, a need exists for a display driver that provides adequate isolation between a storage capacitor and a liquid crystal cell and further eliminates flicker without the need for frame doubling.

Brief Summary of the Invention

In a first aspect of the present invention, a display driver for a display unit having a memory and a liquid crystal cell among a plurality of liquid crystal displays comprises a first drive circuit coupled to a first memory element of the liquid crystal cell, a second drive circuit coupled to a second memory element of the liquid crystal cell, and a switching arrangement for switching the liquid crystal cell between the first and the second drive circuits.

In a second aspect of the present invention, a display driver among an array of array drivers for a display unit having a corresponding array of liquid crystal cells comprises a first storage capacitance and a first amplifier selectively coupled between the first storage capacitance and the liquid crystal cell forming a first drive circuit, a second storage capacitance and a second amplifier coupled between the second storage capacitance and the liquid crystal cell forming a second drive circuit, and a switching arrangement for switching the first and second drive circuits.

In a third aspect of the present invention, a method of driving a LCD/LCOS display comprises the steps of isolating a storage capacitance from a liquid crystal cell using a differential amplifier in each drive cell among a plurality of drive cells and switching among the plurality of drive cells to drive the liquid crystal cell.

Brief Description of the Drawings

FIG. 1 is a block diagram of a liquid crystal cell driver in accordance with the present invention.

FIG. 2 is a block diagram of another liquid crystal cell driver in accordance with the present invention.

FIG. 3 is a block diagram of a display unit utilizing a switching liquid crystal cell driver in accordance with the present invention.

FIG. 4 is a block diagram of a display unit utilizing a liquid crystal cell driver in accordance with the present invention.

FIG. 5 is a flow chart illustrating a method of driving a display in accordance with the present invention.

FIG. 6 is a timing diagram for static Vito in accordance with the present invention.

FIG. 7 is a timing diagram for a switched Vito in accordance with the present invention.

Detailed description of the Preferred Embodiments

In order to overcome the problems described above, it is proposed to add an amplifier such as a differential amplifier 16 between the internal storage capacitance (14), and the LC cell (20) as shown in FIG. 1. In other words, a drive amplifier is added to the driving LC cell. This adds isolation between the storage capacitor and the LC cell. The added current drive capability ensures that the voltage on the pixel will rapidly become that desired. It also allows for very low leakage current from the storage capacitor (FET has very high input impedance), and allows for a continuous refresh of the voltage on the LC, which eliminates the 'droop' problem, as well as the residual voltaic potential stored in the cell. This should improve both the flicker issue, as well as the 'image sticking' problem which is associated with the inability to achieve DC balance in the cell. It should also allow the cell to work well even at somewhat elevated temperatures.

The disadvantage of this technique is that it increases the DC current through the liquid crystal cell. This disadvantage can be overcome in part by gating the current source in the bottom of the differential amplifier. This can use the 'pixel select' or 'row select' bit in the device (see FIG.1). In this way, a periodic refresh of the voltage can be achieved, while reducing the power consumption by 1/nrow, where nrow is the number of rows in the device. Since heating is uniform, this gating in some situations may not be needed.

A typical implementation in CMOS is shown in FIG 1. The components are schematic representations, and alternate configurations can be used without loss of generality. The key points are the amplifier 16, which applies a closed loop correction voltage to the LC cell, and the gated current source which allows reduction of power consumption.

Typically this circuit could be implemented with 3 transistors, which can be placed under the liquid crystal cell in an LCOS display device. In the arrangement of FIG. 1, the amplifier 16 decouples the LC cell from the memory element. FIG. 1 illustrates a liquid crystal cell driver 10 for a liquid crystal display. The liquid crystal cell driver preferably comprises a plurality of transistors (12, 15, 17, and 18) coupled to each other as shown in FIG. 1, a storage capacitance such as a storage capacitor 14, and a plurality of resistors 19 and 21. Preferably, three (3)transistors, such as transistors 15, 17 and 18 form the amplifier 16, preferably in the form of a differential amplifier which serves as the buffer or isolation amplifier. The differential amplifier 16 is preferably comprised of N-Channel transistors serving as an output to the liquid crystal cell. Additionally, the respective source electodes of the transistors of the differential amplifier are driven by a current source such as an N-Channel transistor such as transistor 18 that may be gated. This current mirror arrangement ensures a predetermined voltage on a given pixel. The differential amplifier 16 is coupled between the storage capacitor 14 and provides isolation between the storage capacitor 14 and a liquid crystal cell or pixel.

The arrangement of FIG. 2 adds a global switch element (32) to transfer data from the storage element to the driver. This allows for increased pixel drive for the same circuit operating voltages, and reduces image retention and flicker by allowing for inversion of the pixel drive voltage and the ITO transparent conductive electrode from frame to frame. Referring to FIG. 2, another liquid crystal cell driver 30 is shown similar to the liquid crystal cell driver 10 of FIG. 1. In addition to the elements previously recited with respect to cell driver 10, cell driver 30 further comprises a global switch element 32 in the form of a transistor coupled between the storage capacitor 14 and the differential amplifier 16. The

global switch element transfers data from the memory cell to a driver capacitor 36 of the display driver.

The problem of flicker has been addressed by many mechanisms in the past. The issue of drive voltage and image retention has been addressed in digital drive LCOS displays. For analog systems, drive voltage and image retention issues can be addressed similarly, due to the need for continuous updating.

The main benefit of the technique disclosed herein is to separate the driver capacitor 36 from the storage capacitor 14. This separation as shown in FIG. 2 allows for updating all the cells of entire LC array at one time if desired. The benefit of this is two-fold. First, this separation (with further pre-processing to determine which LC cells have changed from frame to frame) also allows for updating of only the cells in the LC array that have changed from a prior frame. In other words, the contents of the storage capacitor 14 can be changed without instantaneously changing the display content on the LC cells. This greatly reduces the data rate needed for static pictures. It also allows for the possibility of driving the display in an interlaced mode without displaying interline scanning artifacts. In a system which is interlaced, normally odd lines are written on a first scan, and even lines are written on a second scan. This scanning scheme produces the artifact known as 'interline flicker'. This even happens for data which is not intrinsically interlaced, such as film. The reason for "interline flicker" is that the even lines from one frame are displayed at the same time that the odd lines from the previous frame are displayed. Any portion of the frame which changed will show an interline flicker. With the present invention, a display having an array of storage capacitors (14) corresponding to an array of LC cells would be updated just as normal (even lines followed by odd lines), except that the entire LC array would then be updated once the storage array has been filled. Thus, lines from different fames are never displayed simultaneously. The second benefit of this technique is that it allows the common electrode voltage to be modulated from frame to frame. This modulation increases the effective electric field which can be applied to the LC cell for a given operating voltage of the

driver circuit. This is a significant advantage, as finer process geometry will reduce the maximum allowed driving voltage. The benefits described above only occur when the pixels are all updated at once. The simultaneous updating of the pixels can only be done if the storage array (array of storage capacitors (14)) is separated from the driver array (array of driver capacitors (36)).

The technique can most simply be implemented with the circuit described in FIG. 1, with a modification as shown in FIG. 2. The voltage Vnn of FIG. 2 is a static voltage which controls the current source for the transistors 15 and 17. The Row and Column address are normal addressing for an active matrix display. The control signals (Transfer and Discharge) are separate globally controlled signals which transfer the charge on the storage capacitor 14 to the drive capacitor 36, which drives the LC cell. The additional transistors 32 and 34 and capacitor 36 on the device are added to implement the new circuit and operationally allows for the adequate discharge of current from the storage capacitor 14 after each transfer. The additional components should not be significant as process fabrication technology moves forward towards 0.1 microns and below.

In the arrangement of FIG. 1, an isolation amplifier was added to decouple the LC cell from the memory element, as explained before. The additional embodiment of the invention of FIG. 3, adds a second cell driver portion having a second storage cell (preferably storage capacitor 14') and amplifier (preferably differential amplifier 16' including transistors 15' and 17' and 18') and a pair of transistors (72 and 74) to switch between the two drive cells at a high rate of speed. The second drive cell also preferably comprises transistors 12' and 18' and resistors 19' and 24' arranged similarly to the embodiment of FIG. 1.) This eliminates flicker without the need for frame doubling. It can also be used to increase the drive voltage available on the cell.

The basic advantage of the embodiment of FIG. 3 for driving LCOS is that it uses two separate storage elements and drive circuits that are switched to drive the LC cell. This allows a fast switching frequency, which makes the flicker rate of the cell much above frequencies detectable by the human eye. It

also allows for the possibility of switching the common electrode voltage (Vito) to help to increase the possible RMS voltage on the cell for a given operating voltage of the silicon back plane.

The upper cell (using transistor 72) contains the voltage to drive the LC during the 'positive' frame, the lower cell (using transistor 74) contains the voltage to drive the LC in the 'negative' frame. The voltage during the positive and negative frames must be balanced with Vito in order to avoid a net DC voltage on the cell, and resultant imager retention and reliability issues. VDD and VSS are the upper and lower operating voltages for the CMOS devices. VNN is set to regulate the current through the transistors of the differential amplifiers, and controls the power dissipation of the amplifier. V1 and V2 are global switching voltages which determine which amplifier is driving the Liquid Crystal cell. A timing diagram for a static Vito is shown in FIG. 6. A timing diagram for switched Vito is shown in FIG. 7.

Further referring to FIGs. 6 and 7, these timing diagrams reflect the 'positive' picture data (V+) in the upper storage cell (14) in FIG. 3, and the 'negative' picture data (V-) in the lower storage cell (14'). In the case of FIG. 6, Vito is not switched. When V1 is switched high (and V2 being low), the transistor 72 is turned on, and V+ is applied to the LC cell. The effective voltage on the cell is (V+ - Vito). At the next switching time, V1 is switched low, and V2 is switched high. The transistor 74 is turned on, and V- is applied to the LC cell. The effective voltage on the cell is (Vito - V-).

In the case of FIG. 7, Vito is switched. When V1 is switched high (and V2 being low), the transistor 72 is turned on, and V+ is applied to the LC cell. Simultaneously, Vito is switched to low (Vito-), as shown in FIG. 7. The effective voltage across the LC cell is then (V+ - Vito-). At the next switching time, V1 is set to low to turn off transistor 72, and switch V2 high to turn on transistor 74. This applies V- to the cell. Simultaneously, Vito is switched to high (Vito+), as shown in FIG. 7. The effective voltage across the LC cell is then (Vito+ - V-).

If the maximum value of V+ and V- is fixed by the maximum voltage of the backplane process, then a fixed value of Vito as in FIG. 6 must be (V+ + V-)/2. If Vito can be switched, as in FIG. 7, Vito- can be V-, and Vito+ can be V+. Thus, the maximum effective voltage on the LC cell is (V+ - V-)/2 for FIG. 6, but V+ - V- for FIG. 7. The timing of FIG. 7 can ONLY be achieved on an analog system if all of the cells are updated simultaneously by the global switches V1 and V2.

Typically the time between V1 and V2 switching should be 1 or 2 msec. This will need to be determined for a given set of LC materials and the characteristics of the back plane, and response time of the devices.

The obvious detriment of this scheme is that it requires a large number of transistors to implement (perhaps as many as 12). This should be easily possible with a 20 micron pixel and a .35 micron process. Similar scaling on smaller pixels is possible with finer process geometry.

Now referring to FIG. 4, a display unit 50 is shown that can utilize the display drivers 20 or 30 or 70 as previously described above. The display unit 50 preferably includes a plurality of display elements arranged in a matrix of rows and columns and a memory element and a liquid crystal cell. The driver preferably switchably outputs one of a plurality of voltages to the display elements on at least one of the matrix of rows and columns, the display unit including a conventional decoder 51 and the driver controlled by the conventional decoder 51. The driver can include a storage capacitor and a differential amplifier coupled between the storage capacitor and the liquid crystal cell, whereby the differential amplifier provides isolation between the storage capacitor and the liquid crystal cell. The driver can include a decoder and a plurality of semiconductor switched controlled to be opened or closed by an output signal of the decoder 51. As shown in FIG. 4, the display unit 50 can include a row drive circuit having a plurality of row (scanning) address lines 56 and a column drive circuit 62 having a plurality of column (data) address lines 58.

Referring to FIG. 5, a flow chart is shown illustrating a method 200 of driving a display in accordance with the present invention. The method 200

preferably comprises the step 202 of providing isolation between memory elements (such as a storage capacitor) and a liquid crystal cell using a differential amplifier in each drive cell among a plurality of drive cells. Preferably, the isolation is provided between a first storage capacitor and the liquid crystal cell using a first differential amplifier in a first cell and between a second storage capacitor and the liquid crystal cell using a second differential amplifier in a second cell. The method 200 also preferably comprises the step 204 of switching among the plurality of drive cells to drive the liquid crystal cell, where preferably a pair of transistors performs the function of switching between the first and second drive cells. Step 208 can further provide the step of eliminating flicker without frame doubling. The method 200 may further comprise the step 216 of updating an entire array of liquid crystal elements simultaneously and/or the step 218 of updating only a memory cell that has changed from a previous frame. Additional benefits of the method 200 may include the step 220 of driving a memory array in an interlaced mode without displaying interline scanning artifacts and/or the step 222 of modulating a common electrode voltage from frame to frame to reduce a required liquid crystal drive voltage.

Although the present invention has been described in conjunction with the embodiments disclosed herein, it should be understood that the foregoing description is intended to illustrate and not limit the scope of the invention as defined by the claims.

Claims

1. A display unit having an array of liquid crystal cells, comprising:

an array of display drivers, a given display driver being associated with a given liquid crystal cell and including:

a first storage capacitance and a first amplifier selectively coupled between the first storage capacitance and the given liquid crystal cell forming a first drive circuit;

a second storage capacitance and a second amplifier coupled between the second storage capacitance and the given liquid crystal cell forming a second drive circuit; and

a switching arrangement for switching the first and second drive circuits.

2. The display driver of claim 1, wherein the first amplifier and the second amplifier are both differential amplifiers.

3. The display driver of claim 2, wherein the differential amplifier comprises a pair of N-Channel transistors having respective drain electrodes coupled and serving as an output to the liquid crystal cell.

4. The display driver of claim 1, wherein the each of said first and second drive circuits further comprises a global switch element coupled between the respective storage capacitance and the amplifier, wherein the global switch element transfers data from the storage capacitance to one of the first and second drive circuits.

5. The display driver of claim 1, wherein the switching mechanism comprises a first transistor driven by a first global switching voltage and a second transistor driven by a second global switching voltage.

6. A display driver for a given liquid crystal cell of an array of liquid crystal cells, comprising:

a first drive circuit coupled to a first memory element of the given liquid crystal cell;

at least a second drive circuit coupled to a second memory element of the given liquid crystal cell; and

a switching arrangement for switching the liquid crystal cell between the first and at least the second drive circuits.

7. The display driver of claim 6, wherein each of the first and the second drive circuits comprise differential amplifiers comprising a pair of N-Channel transistors having respective source electrodes coupled to a current source and serving as an isolation amplifier to the liquid crystal cell.

8. The display driver of claim 6, wherein each of the first and the second drive circuits comprise differential amplifier comprising a pair of N-Channel transistors having respective sources coupled to a current source.

9. The display driver of claim 6, wherein the switching mechanism comprises a first transistor driven by a first global switching voltage and a second transistor driven by a second global switching voltage.

10. The display driver of claim 6, wherein the display driver further comprises a global switching element which is coupled between a storage capacitor and a differential amplifier and used for reducing image retention and flicker.

11. The display driver of claim 6, wherein the display driver updates an entire array of liquid crystal arrays elements simultaneously.

12. The display driver of claim 6, wherein the display driver updates only a memory cell that has changed from a previous frame.

13. The display driver of claim 6, wherein the display driver drives a memory array in an interlaced mode without displaying interline scanning artifacts.

14. A method of driving a LCD/LCOS display, comprising the steps of:

providing isolation between a storage capacitance and a liquid crystal cell using a differential amplifier in each drive cell among a plurality of drive cells;

switching among the plurality of drive cells to drive the liquid crystal cell.

15. The method of claim 14, wherein the step of providing further comprises the step of providing in a first drive cell isolation between a first storage capacitance and the liquid crystal cell using a first differential amplifier and providing in a second drive cell isolation between a second storage capacitance and the liquid crystal cell using a second differential amplifier.

16. The method of claim 15, wherein the step of switching further comprises the step of switching between the first drive cell and the second drive cell using a pair of transistors to switch between the first drive cell and the second drive cell.

17. The method of claim 15, wherein the method further comprises the step of eliminating flicker without frame doubling.

18. The method of claim 14, wherein the method further comprises the step of updating an entire array of liquid crystal elements simultaneously.

19. The method of claim 14, wherein the method further comprises the step of updating only a memory cell that has changed from a previous frame.

20. The method of claim 14, wherein the method further comprises the step of driving a memory array in an interlaced mode without displaying interline scanning artifacts.

21. The method of claim 14, wherein the method further comprises the step of modulating a common electrode voltage from frame to frame to reduce a required liquid crystal drive voltage.

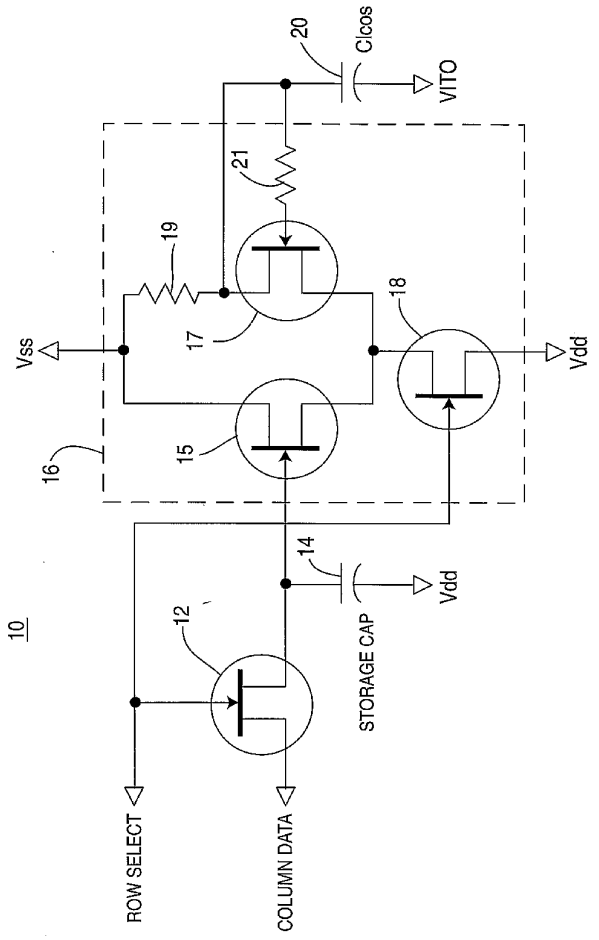
10
20
Cicos
ViTO
21
19
18
17
Vss
Vdd
16
15
14
Vdd
12
STORAGE CAP
ROW SELECT
COLUMN DATA

FIG. 1

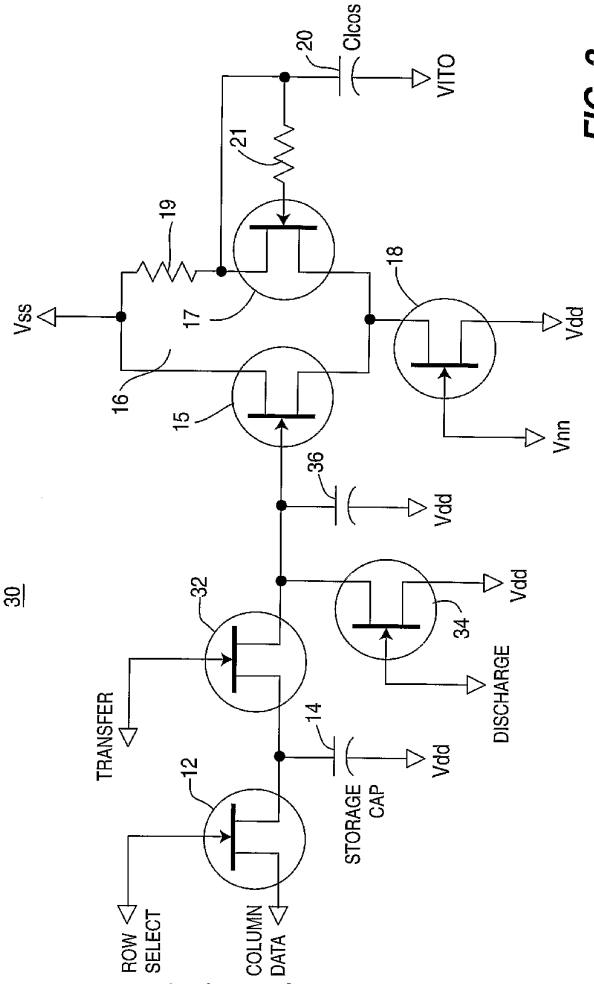
30
20
Clcos
VITO
21
19
18
Vss
17
Vdd
16
15
Vnn
36
Vdd
32
Vdd
34
DISCHARGE
TRANSFER
14
Vdd
12
STORAGE CAP
ROW SELECT
COLUMN DATA

FIG. 2

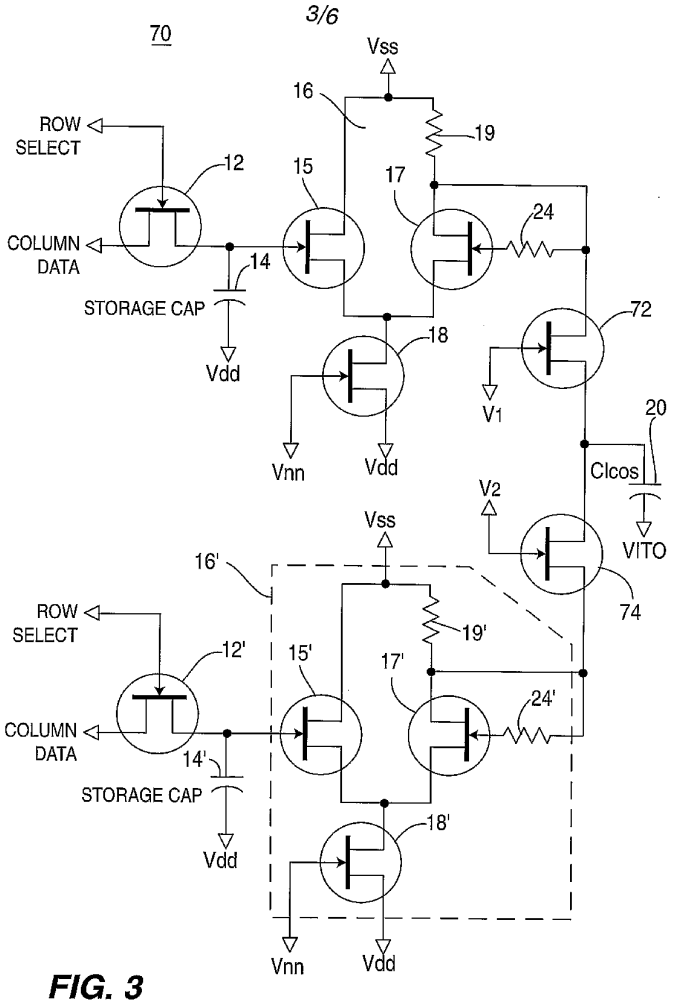
70
Vss
16
19
ROW SELECT
12
15
17
24
COLUMN DATA
14
STORAGE CAP
Vdd
18
72
V1
20
Vnn
Vdd
Clcos
V2
Vss
VITO
16'
74
ROW SELECT
19'
12'
15'
17'
24'
COLUMN DATA
14'
STORAGE CAP
Vdd
18'
Vnn
Vdd

FIG. 3

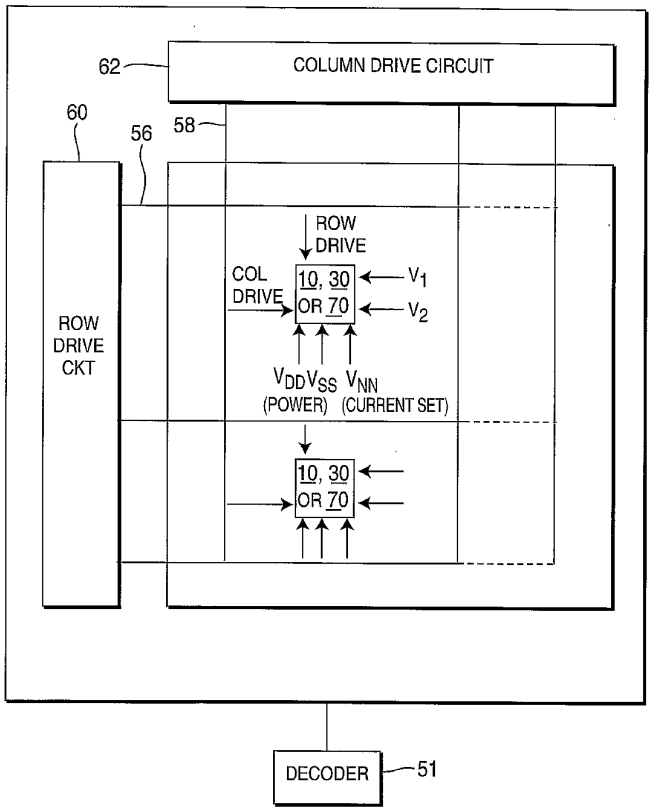
62
COLUMN DRIVE CIRCUIT
60
56
58
ROW DRIVE
COL DRIVE
10, 30
OR 70
V_1
V_2
ROW DRIVE CKT
V_{DD} V_{SS} V_{NN}
(POWER) (CURRENT SET)
10, 30
OR 70
DECODER
51

FIG. 4

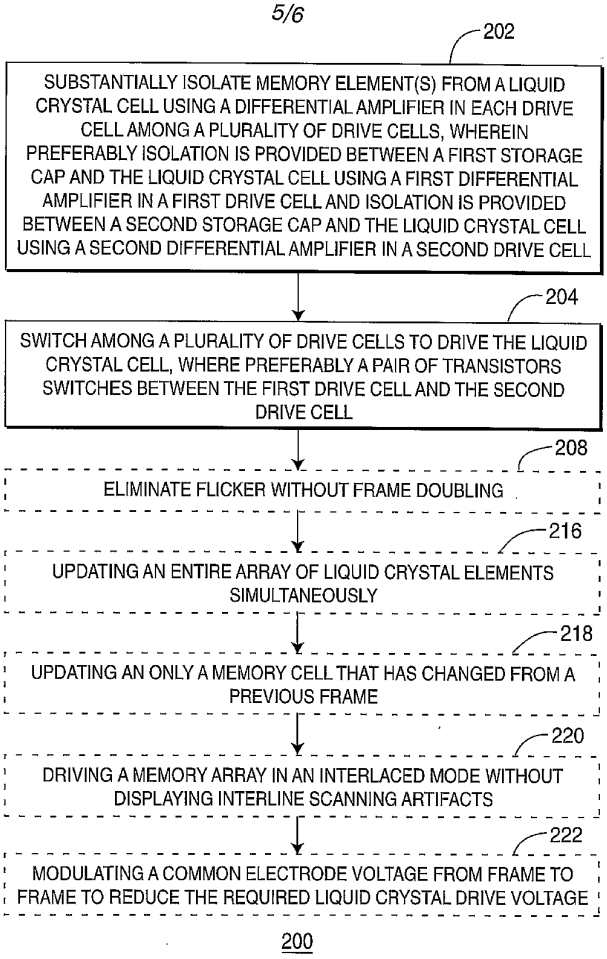
202
SUBSTANTIALLY ISOLATE MEMORY ELEMENT(S) FROM A LIQUID CRYSTAL CELL USING A DIFFERENTIAL AMPLIFIER IN EACH DRIVE CELL AMONG A PLURALITY OF DRIVE CELLS, WHEREIN PREFERABLY ISOLATION IS PROVIDED BETWEEN A FIRST STORAGE CAP AND THE LIQUID CRYSTAL CELL USING A FIRST DIFFERENTIAL AMPLIFIER IN A FIRST DRIVE CELL AND ISOLATION IS PROVIDED BETWEEN A SECOND STORAGE CAP AND THE LIQUID CRYSTAL CELL USING A SECOND DIFFERENTIAL AMPLIFIER IN A SECOND DRIVE CELL
204
SWITCH AMONG A PLURALITY OF DRIVE CELLS TO DRIVE THE LIQUID CRYSTAL CELL, WHERE PREFERABLY A PAIR OF TRANSISTORS SWITCHES BETWEEN THE FIRST DRIVE CELL AND THE SECOND DRIVE CELL
208
ELIMINATE FLICKER WITHOUT FRAME DOUBLING
216
UPDATING AN ENTIRE ARRAY OF LIQUID CRYSTAL ELEMENTS SIMULTANEOUSLY
218
UPDATING AN ONLY A MEMORY CELL THAT HAS CHANGED FROM A PREVIOUS FRAME
220
DRIVING A MEMORY ARRAY IN AN INTERLACED MODE WITHOUT DISPLAYING INTERLINE SCANNING ARTIFACTS
222
MODULATING A COMMON ELECTRODE VOLTAGE FROM FRAME TO FRAME TO REDUCE THE REQUIRED LIQUID CRYSTAL DRIVE VOLTAGE
200

FIG. 5

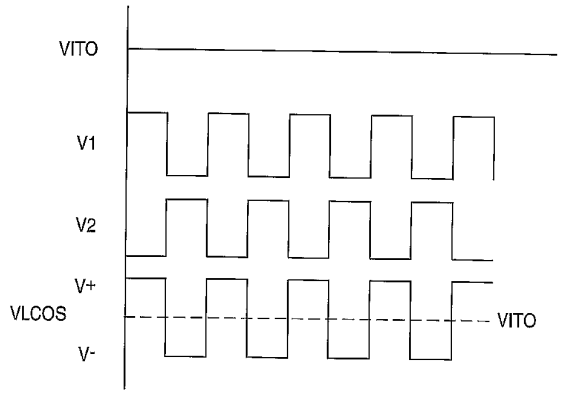

FIG. 6

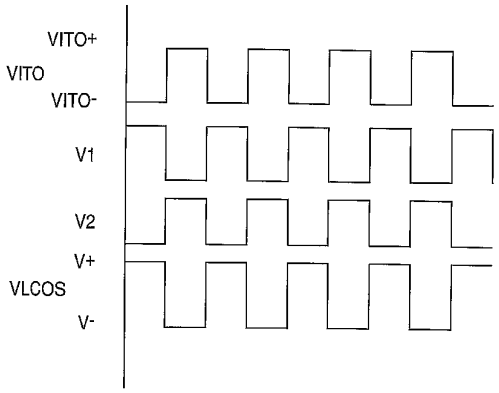

FIG. 7

【手続補正書】
【提出日】平成14年6月10日(2002.6.10)
【手続補正１】
【補正対象書類名】明細書
【補正対象項目名】特許請求の範囲
【補正方法】変更
【補正の内容】
【特許請求の範囲】
【請求項１】
液晶セルのアレイを有する表示装置であって、
表示ドライバ回路のアレイを備え、所定の表示ドライバ回路は、所定の液晶セルに関連し、前記所定の表示ドライバ回路は、
第１の記憶キャパシタンスと、前記第１の記憶キャパシタンスと前記所定の液晶セルとの間に選択可能に結合されて第１の駆動回路を形成する第１の増幅器と、
第２の記憶キャパシタンスと、前記第２の記憶キャパシタンスと前記所定の液晶セルとの間に結合されて第２の駆動回路を形成する第２の増幅器と、
前記第１と第２の駆動回路を前記所定の液晶セルに切り替えるための切替え手段とを備える表示装置。
【請求項２】
前記第１の増幅器と前記第２の増幅器が、両方とも差動増幅器である、請求項１に記載の表示装置。
【請求項３】
前記差動増幅器が、１対のＮチャネル・トランジスタを備え、前記Ｎチャネル・トランジスタが、結合されたそれぞれのドレイン電極を有し、前記液晶セルへの出力として働く、請求項２に記載の表示装置。
【請求項４】
前記第１と第２の駆動回路が、それぞれ更に、前記それぞれの記憶キャパシタンスと前記増幅器との間に結合された大域スイッチ素子を備え、前記大域スイッチ素子が、前記記憶キャパシタンスからのデータを前記第１と第２の駆動回路の一方に転送する、請求項１に記載の表示装置。
【請求項５】
前記切替え手段が、第１の大域切替え電圧によって駆動される第１のトランジスタと、第２の大域切替え電圧によって駆動される第２のトランジスタとを備える、請求項１に記載の表示装置。
【請求項６】
液晶セル・アレイの所定の液晶セルのための表示ドライバ回路であって、
前記所定の液晶セルの第１のメモリ素子に結合された第１の駆動回路と、前記所定の液晶セルの第２のメモリ素子に結合された少なくとも第２の駆動回路であって、前記第１の駆動回路と前記少なくとも第２の駆動回路とのうちの少なくとも１つが増幅器を含み、
前記第１と少なくとも第２の駆動回路の間で前記液晶セルを切り替えるための切替え手段とを備える表示ドライバ回路。
【請求項７】
前記第１と第２の駆動回路がそれぞれ、１対のＮチャネル・トランジスタを含む差動増幅器を備え、前記Ｎチャネル・トランジスタが、電流源に結合されたそれぞれのソース電極を有し、前記液晶セルに対する分離増幅器として働く、請求項６に記載の表示ドライバ回路。
【請求項８】
前記第１と第２の駆動回路がそれぞれ、１対のＮチャネル・トランジスタを含む差動増幅器を備え、前記Ｎチャネル・トランジスタが、電流源に結合されたそれぞれのソースを有する、請求項６に記載の表示ドライバ回路。

【請求項９】
前記切替え手段が、第１の大域切替え電圧によって駆動される第１のトランジスタと、第２の大域切替え電圧によって駆動される第２のトランジスタとを備える、請求項６に記載の表示ドライバ回路。
【請求項１０】
記憶コンデンサと差動増幅器との間に結合されて残像およびフリッカを減少させるのに使用される大域スイッチング素子を更に備える、請求項６に記載の表示ドライバ回路。
【請求項１１】
液晶アレイ素子のアレイ全体を同時に更新する、請求項６に記載の表示ドライバ回路。
【請求項１２】
前のフレームから変化したメモリ・セルだけを更新する、請求項６に記載の表示ドライバ回路。
【請求項１３】
ライン間走査アーティファクトを表示することなくメモリ・アレイをインタレース・モードで駆動する、請求項６に記載の表示ドライバ回路。
【請求項１４】
液晶表示装置（ＬＣＤ）／液晶オン・シリコン（ＬＣＯＳ）表示装置を駆動する方法であって、
複数の駆動セルのうちの各駆動セル中で差動増幅器を使用して記憶キャパシタンスと液晶セルとの間の分離を与えるステップと、
前記複数の駆動セル間を切り替えて前記液晶セルを駆動するステップとを含む方法。
【請求項１５】
前記与えるステップが更に、第１の駆動セル中で、第１の差動増幅器を使用して第１の記憶キャパシタンスと前記液晶セルとの間の分離を与え、第２の駆動セル中で、第２の差動増幅器を使用して第２の記憶キャパシタンスと前記液晶セルとの間の分離を与えるステップを含む、請求項１４に記載の方法。
【請求項１６】
前記切り替えるステップが更に、前記第１の駆動セルと前記第２の駆動セルとの間を切り替えるための１対のトランジスタを使用して、前記第１の駆動セルと前記第２の駆動セルとの間を切り替えるステップを含む、請求項１５に記載の方法。
【請求項１７】
フレームを倍増せずにフリッカを無くすステップを更に含む、請求項１５に記載の方法。
【請求項１８】
液晶素子のアレイ全体を同時に更新するステップを更に含む、請求項１４に記載の方法。
【請求項１９】
前のフレームから変化したメモリ・セルだけを更新するステップを更に含む、請求項１４に記載の方法。
【請求項２０】
ライン間走査アーティファクトを表示することなくメモリ・アレイをインタレース・モードで駆動するステップを更に含む、請求項１４に記載の方法。
【請求項２１】
共通電極電圧をフレーム間で変調して、必要とされる液晶駆動電圧を低減するステップを更に含む、請求項１４に記載の方法。

【国際調査報告】

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US01/44896

A. CLASSIFICATION OF SUBJECT MATTER
IPC(7) : G09G 3/36, 5/00
US CL : 345/90, 205
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 345/87, 90, 92, 93, 96, 98, 204, 205; 348/790, 793; 349/42, 48

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5,627,557 A (YAMAGUCHI et al.) 06 May 1997, abstract, column 2, line 50 - column 4, line 40; column 8, lines 5-50.	1, 4, 5
---		---
Y		2, 3
Y	US 5,680,149 A (KOYAMA et al.) 21 October 1997, abstract, column 4, line 20 - column 5, line 46.	2, 3, 7, 8, 10, 14-21
X	US 5,945,972 A (OKUMURA et al.) 31 August 1999, abstract, column 18, lines 7-36.	6, 9, 11,
---		---
Y		7, 8, 10, 12-21
Y	US 5,856,817 A (MATSUZAKI) 05 January 1999, abstract, column 2, lines 2-23.	12, 19
Y	US 5,828,366 A (HURST) 27 October 1998, column 1, line 29- column 2, line 22..	13, 20
Y	US 5,852,426 A (ERHART et al.) 22 December 1998, abstract.	21
A	US 6,137,465 A (SEKINE et al.) 24 October 2000, abstract, column 4, line 20 - column 7, line 12.	1-21

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent published on or after the international filing date
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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search
13 March 2002 (13.03.2002)

Date of mailing of the international search report
09 APR 2002

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摘要(译)

用于具有存储元件和多个液晶单元中的液晶单元的显示单元（50）的单元驱动器（70）包括第一存储电容器（14），第一存储电容器和液晶单元并且第一差分放大器（16）选择性地耦合在第一和第二差分放大器之间以形成第一驱动电路。单元驱动器还包括第二存储电容器（14'），第二差分放大器（16'），耦合在第二存储电容器和液晶单元之间，以形成第二驱动电路，设置有门。切换机构（72和74）用于在第一和第二驱动电路之间切换液晶单元。