(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 187 091 A2

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
13.03.2002 Bulletin 2002/11

(51) Int Cl.[7]: **G09G 3/36**

(21) Application number: **01307578.3**

(22) Date of filing: **06.09.2001**

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE TR
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: **08.09.2000 KR 2000053555**

(71) Applicant: **Kwon, Oh-Kyong**
Seoul, 138-240 (KR)

(72) Inventor: **Kwon, Oh-Kyong**
Seoul, 138-240 (KR)

(74) Representative: **Neobard, William John**
W.H. Beck, Greener & Co.,
7 Stone Buildings,
Lincoln's Inn
London WC2A 3SZ (GB)

(54) Method of driving scanning lines of a active matrix liquid crystal device

(57) A method of driving a gate line in a liquid crystal device such as a liquid crystal display enables an extended line time by causing scan signals to fall at different times while concurrently driving plural gate lines. In the method, scan signals which rise concurrently are applied to at least two gate lines while rendering the scan signals to fall at different timings such that said gate lines are concurrently driven and video signals are sampled by pixels corresponding to said gate lines at different falling times. The present invention makes it possible to extend a line time without lowering of the resolution of the device and without degradation of quality.

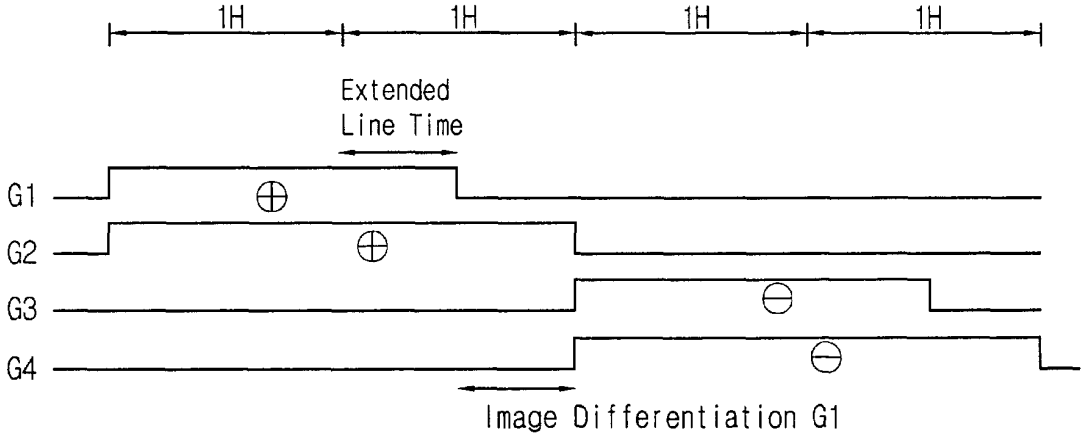

Figure 5

EP 1 187 091 A2

Description

[0001] The present invention relates to the driving technology of liquid crystal devices and more particularly liquid crystal displays (LCD). Embodiments relate to a method of driving a gate line in a large sized and high resolution LCD which enables extension of a line time by making a falling time of scan signals different while concurrently driving plural gate lines.

[0002] Generally, liquid crystal devices utilize the optical property of liquid crystal in which a molecular arrangement of the liquid crystal is varied when an electric field is applied to the liquid crystal. Different applications of liquid crystal devices include beam steering devices, light modulators and displays used for displaying characters, symbols, or graphics. The LCD is one kind of flat panel display in which liquid crystal technologies are combined with semiconductor technologies.

[0003] Thin film transistor (TFT) LCDs have thin film transistors as the switching element for turning on and off pixels. As the TFTs are turned on or off, the pixels are turned on or off.

[0004] As shown in Fig. 1, a general TFT LCD includes a plurality of cells arranged in a matrix configuration. A unit cell includes a TFT 132 serving as the switching element, a liquid crystal cell 134 and a storage capacitor C_{STG}. Sources of the TFTs are connected to data lines (D1-DN) arranged in a column direction and the data lines are connected to a source driver 120. Gates of the TFTs are connected to gate lines (G1-GM) arranged in a row direction and the gate lines are connected to a gate driver 110, thereby enabling a display having an P×Q resolution. For instance, SVGA level has a resolution of 800×600, XGA level has a resolution of 1024×768 and UXGA level has a resolution of 1,600×1200.

[0005] The source driver 120 may also be referred to as a data driver or column driver and the gate driver as a scan driver or row driver.

[0006] Referring to Fig. 1, the liquid crystal cell 134 is connected to the drain of the TFT 132 at a pixel electrode and is disposed between the pixel electrode and a common electrode of an upper panel. The pixel electrode is made of a transparent conductive material such as indium tin oxide (ITO). When a turn on signal is applied to gate of the TFT 132, the pixel electrode transfers a signal voltage applied through the source driver 120 to the liquid crystal cell 134. The common electrode may also be made of a transparent conductive material such as ITO and applies a common voltage VCOM to the liquid crystal cells. The storage capacitor C_{STG} maintains a voltage applied to the pixel electrode during a constant time and controls light transmittance by varying an orientation state of liquid crystal molecules in the liquid crystal cell. One end of the storage C_{STG} can be connected to an independent electrode or gate electrode, which is called "storage on gate" mode.

[0007] In driving this pixel array, if a driving voltage is applied to the liquid crystal only in one direction, degradation of the liquid crystal is accelerated. To avoid this, there is used an inversion which periodically applies an image data voltage applied to the liquid crystal in an opposite polarity. The period of such an inversion is normally one field.

[0008] There are four inversion driving methods, i.e., a field inversion driving method which changes the voltage polarity of all pixels every field at once, a line inversion driving method which changes the voltage polarity of every pixel connected to a single scan line, a column inversion driving method which changes the voltage polarity of a column every field and a dot inversion which changes the polarity of pixel units. In any case, the voltage, which is applied to the pixel electrode through the drain electrode of the TFT is alternately changed such that it has a positive (+) or negative (-) direction with respect to the common voltage VCOM.

[0009] Fig. 2 is a schematic view showing a general gate driver. Referring to Fig. 2, a gate driver 110 includes a shift register 111, a level shifter 112 and output buffers 113. The shift register 111 receives a vertical synchronous signal and a vertical clock signal, and thereby generates scan pulses sequentially. The level shifter 112 shifts a voltage level of the scan pulses to approximately 30 V. The output buffers 113 provide respective gate lines of G1-GM with the level-shifted scan pulses.

[0010] Here, the most general driving method that is used to drive gates is the progressive scanning method as shown in Fig. 3. Since the progressive scanning method scans only a single gate line (or scan line) during one line time (1H), respective gate driving signals are sequentially applied to gate lines every 1H.

[0011] On the other hand, as liquid crystal devices increase in size, the resistance of data lines and the load of capacitance increase. Thus in a display the time for which the data driving circuit transmits a video signal to the pixel is more and more shortened. This may lead to insufficient charge of the pixel and lowers image quality. Therefore, this problem should be necessarily resolved.

[0012] Fig. 4 shows driving signals used in the conventional interlace scanning method in order to increase the line time. Referring to Fig. 4, the conventional interlace scanning method has a line time twice as long as the progressive scanning method.

[0013] However, the interlace scanning method has a drawback in that the vertical resolution decreases by half since the same video signal is transmitted into pixels connected to two gate lines. Accordingly, these conventional gate-driving methods are not alternative methods when considering the current trend for high resolution.

[0014] Accordingly, the present invention is directed to a method for driving gates of an LCD that substantially obviates one or more problems due to limitations and disadvantages of the related art.

[0015] An aim of embodiments of the present invention is to provide a method for driving gates of an LCD enabling to extend the line time without lowering the resolution by rendering a falling time of scan signals different while driving plural gate lines at the same time.

[0016] According to one aspect of the invention there is provided a method for driving gates of an LCD in which scan signals which rise concurrently are applied to at least two gate lines while rendering said scan signals to fall at different timings such that said gate lines are concurrently driven and video signals are sampled by pixels corresponding to said gate lines at different falling times.

[0017] According to another aspect of the invention, there is provided a method for driving gates of an LCD in which scan signals which fall concurrently are applied to at least two gate lines while rendering said scan signals to rise at different timings such that said gate lines are concurrently driven and video signals are sampled by pixels corresponding to said gate lines at different rising timings.

[0018] According to yet another aspect of the invention there is provided a method for operating a pixellated liquid crystal display device, the device having a plurality of data lines and a plurality of scan lines; the method comprising providing scan signals having substantially concurrent first level transitions and second level transitions opposite to said first transitions which occur at mutually different times; and applying said scan signals to at least two scan lines, whereby said scan lines are concurrently driven and data signals on the data lines are sampled by pixels corresponding to said scan lines at different times corresponding to the second transitions.

[0019] Additional advantages, objects, and features of the invention will be set forth in part in the description which follows and in part will become apparent to those having ordinary skill in the art upon examination of the following or may be learned from practice of the invention. The objectives and other advantages of the invention may be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

[0020] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this application, illustrate embodiment(s) of the invention and together with the description serve to explain the principle of the invention. In the drawings:

Fig.1 is an equivalent circuit diagram of a general TFT-LCD;
Fig.2 is a schematic view of a general gate driving circuit;
Fig.3 shows waveforms of gate driving signals of a general progressive scanning method;
Fig.4 shows waveforms of gate driving signals of an interlace scanning method so as to increase the line time;
Fig. 5 shows waveforms of gate driving signals of a line time extending driving method to scan two gate lines concurrently in accordance with an embodiment of the present invention;
Fig. 6 shows waveforms of gate driving signals of a line time extending driving method to scan three gate lines concurrently in accordance with an embodiment of the present invention;
Fig. 7 shows waveforms of gate driving signals of a line time extending driving method to scan four gate lines concurrently in accordance with an embodiment of the present invention;
Fig. 8 is a table showing a line polarity of N-th and (N+1)-th when inversion-driving two gate lines in accordance with the embodiment of Fig. 5;
Fig. 9 is a general circuit diagram of a TFT-LCD pixel useful in understanding the present invention; and
Fig. 10 shows waveforms of gate driving signals of a line time extending driving method to scan two gate lines concurrently in accordance with an embodiment of the present invention.

[0021] Referring now to the first embodiment, Fig.5 shows waveforms of gate driving signals in a line time extending driving method to scan two gate lines concurrently in accordance with the present invention.

[0022] Referring to Fig. 5, in this embodiment gate driving signals applied to two gate lines rise concurrently but fall at different timings. In the conventional two gate lines driving method, if gate driving signals are concurrently applied to gate lines G1 and G2, identical image signals are applied to pixels sharing the same data line. By contrast, in the gate line driving method of the present invention, since the first gate driving signal G1 falls first, an image signal corresponding to pixels connected to the first gate line is sampled. After that, the second gate driving signal G2 falls and thereby an image signal corresponding to pixels connected to the second gate line is sampled.

[0023] Using the gate driving method of the present invention, it becomes possible to extend the line time 30-70% longer than that in the normal progressive scanning method and at the same time it becomes possible to transmit image signals corresponding to pixels connected to each of the gate lines unlike the conventional interlace scanning method in which two gate lines are concurrently driven and they concurrently fall. Here, a specific extending percentage of the line time may be different depending on a panel characteristic.

[0024] For example, when driving gate lines of an LCD panel having a resolution of XGA level (1024×768) using a

frame frequency of 75 Hz, the conventional progressive scanning method has a line time of approximately 17 μsec but a line time extending driving method of the present invention can have a line time of approximately 22-30 μsec.

[0025] The line time extending driving method of the present invention is executed by concurrently driving a chosen number N of gate lines. For instance, Fig. 5 corresponds to a method of concurrently selecting two gate lines, Fig. 6 corresponds to a method of concurrently selecting three gate lines and Fig. 7 corresponds to a method of concurrently selecting four gate lines.

[0026] Thus, as the number of lines which can be concurrently selected and then driven increases, it is possible to secure longer line times and to extend the number of selectable lines. And, as shown in Fig. 5, 6 and 7, the line time extending driving method of the present invention performs an N-line inversion driving in which image signals having the same polarity are transferred to pixels connected gate lines which are concurrently selected. In other words, as shown in Fig. 8 of describing one example of two lines inversion driving, such an inversion is performed every line in the column direction and is performed every two lines in the row direction. When driving N lines concurrently, such an inversion is performed every N lines.

[0027] In the meanwhile, according to the gate line driving method of the present invention in which the falling timings of two gate lines are different from each other while the two gate lines are concurrently driven, it is possible to anticipate an extension of the line time but there may be occur a voltage difference of ΔVp between pixels in even gate lines and odd gate lines. This voltage difference will now be explained.

[0028] Pixels of a TFT-LCD can be modeled in a circuit diagram of Fig. 9. In Fig. 9, symbols D1 and D2 are data lines, G1 and G2 are gate lines, C_{LC} is a liquid crystal cell modeled as a capacitor and C_{STG} is a storage capacitance, respectively. Symbols C_{GS1} and C_{GS2} indicate parasitic capacitances.

[0029] Referring to Fig. 9, as a gate driving signal of G1 falls, a voltage of the liquid crystal cell C_{LC} is coupled through the parasitic capacitance C_{GS1} and thereby the voltage is varied. A variation amount in this voltage ΔV_{P1} can be obtained from equation 1:-

$$\Delta V_{P_1} = \frac{C_{GS_1}}{C_{LC} + C_{STG} + C_{GS_1} + C_{GS_2}} \times (-V_G) \qquad \text{Equation 1}$$

where C_{LC} is a capacitance of the liquid crystal and V_G is a magnitude in the gate driving signal.

[0030] A voltage variation amount is also generated by the parasitic capacitance C_{GS2}. In other words, as a gate signal of G2 rises, a voltage of the liquid crystal is coupled with the parasitic capacitance C_{GS2} and thereby the voltage is varied.

[0031] As shown in Fig. 9, the pixels connected to an odd gate line generate only a voltage variation amount of ΔV_{P1} defined by the equation 1 while the pixels connected to an even gate line generate a voltage variation amount corresponding to a sum of ΔV_{P1} and ΔV ΔV_{P2} defined by equation 2.

$$\Delta V_{P_2} = \frac{C_{GS_1}}{C_{LC} + C_{STG} + C_{GS_1} + C_{GS_2}} (-V_G) + \frac{C_{GS_2}}{C_{LC} + C_{STG} + C_{GS_1} + C_{GS_2}} V_G \qquad \text{Equation 2}$$

[0032] Thus, the pixels connected to the odd gate lines have a different voltage variation to that of the pixels connected to the even gate lines. This is because when the image signal is sampled to the pixels connected to the gate line of G1, only a gate driving signal applied to the gate line of G1 falls while when the image signal is sampled to the pixels connected to the gate line of G2, falling of a gate driving signal applied to the gate line of G2 and rising of a gate driving signal applied to the gate line of G3 are concurrently generated. As a result, a voltage difference ΔVp between even gate lines and odd gate lines is generated and thereby the picture quality may be lowered.

[0033] In order to resolve the aforementioned drawbacks, as shown in Fig. 10, another embodiment of the present invention partially modifies the gate driving method of the present invention provided previously. In other words, as aforementioned, since the voltage difference ΔVp between pixels connected to even gate lines and odd gate lines is due to a difference between the gate driving signals applied to the even gate lines and the odd gate lines, the present embodiment renders the odd gate lines and the even gate lines to be under the same driving condition.

[0034] For instance, when driving two gate lines as shown in Fig. 10, gate driving signals which are applied to even gate lines of G2, G4 and so on fall before gate driving signals which are applied to odd gate lines of G1, G3 and so on fall, and the gate driving signals applied to even gate lines of G2, G4 and so on again rise when the gate driving signals which are being applied to odd gate lines of G1, G3 and so on fall. As a result, all of the pixels connected to the even and odd gate lines have an identical condition for generation of the voltage difference ΔVp and thus the voltage difference problem between the pixels connected to the even and odd gate lines can be resolved.

[0035] While the driving method of the present invention shows and describes embodiments in which the gate driving

signals applied to the gate lines rise concurrently and fall at different timings, it is not limited to the above-described embodiments. In other words, the present invention makes it possible to extend a line time without lowering of the resolution by allowing the gate driving signals to fall concurrently and then to rise at different timings depending on characteristics of the used LCD panel, thus driving plural gate lines concurrently while transferring video signals to the gate lines at different rising timings.

[0036] As described above, using embodiments of a gate line driving method of the present invention, it becomes possible to increase a line time without lowering the resolution and possible to sufficiently charge/discharge the pixel electrode by making different a falling time of scan signals while concurrently driving plural gate lines.

[0037] Further, the gate driving signal applied to the odd gate line may have the same falling condition as the gate signal applied to the even gate line, thereby preventing degradation in picture quality.

[0038] The foregoing embodiments are merely exemplary and are not to be construed as limiting the present invention. The present teachings can be readily applied to other types of apparatus, especially other apparatus using liquid crystals. The description of the present invention is intended to be illustrative, and not to limit the scope of the claims. Many alternatives, modifications, and variations will be apparent to those skilled in the art.

Claims

1. A method for driving gate lines of a liquid crystal display, in which scan signals which rise concurrently are applied to at least two gate lines while rendering said scan signals to fall at different timings such that said gate lines are concurrently driven and video signals are sampled by pixels corresponding to said gate lines at different falling timings.

2. The method of claim 1, wherein said scan signal rises concurrently within an N line time when driving an N number of gate lines concurrently and has different falling time every gate line.

3. The method of claim 1 or 2, wherein said scan signal comprises a first scan signal which is applied to an even gate line and a second scan signal which is applied to an odd gate line, wherein the first scan signal falls faster than the second scan signal and rises when the second scan signal falls, to render a falling condition of the odd gate line and the even gate line equal.

4. A method for driving gate lines of a liquid crystal display, in which scan signals which fall concurrently are applied to at least two gate lines while rendering said scan signals to rise at different timings such that said gate lines are concurrently driven and video signals are sampled by pixels corresponding to said gate lines at different rising timings.

5. A method for operating a pixellated liquid crystal display device, the device having a plurality of data lines and a plurality of scan lines; the method comprising providing scan signals having substantially concurrent first level transitions and second level transitions opposite to said first transitions which occur at mutually different times; and
applying said scan signals to at least two scan lines, whereby said scan lines are concurrently driven and data signals on the data lines are sampled by pixels corresponding to said scan lines at different times corresponding to the second transitions.

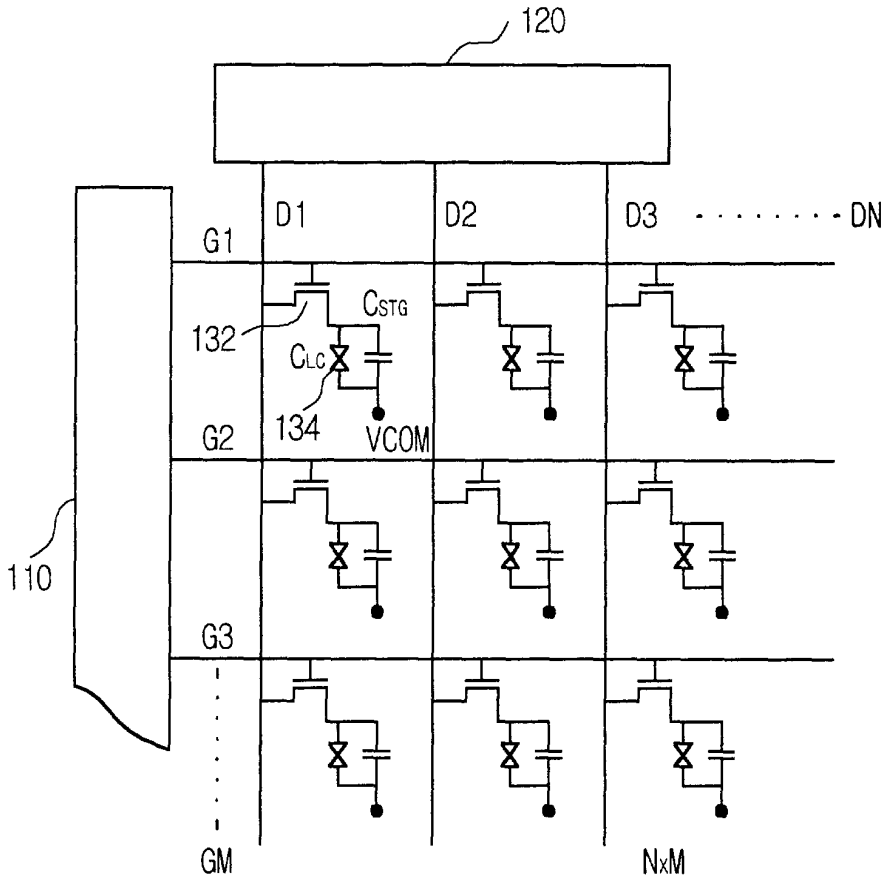

Figure 1

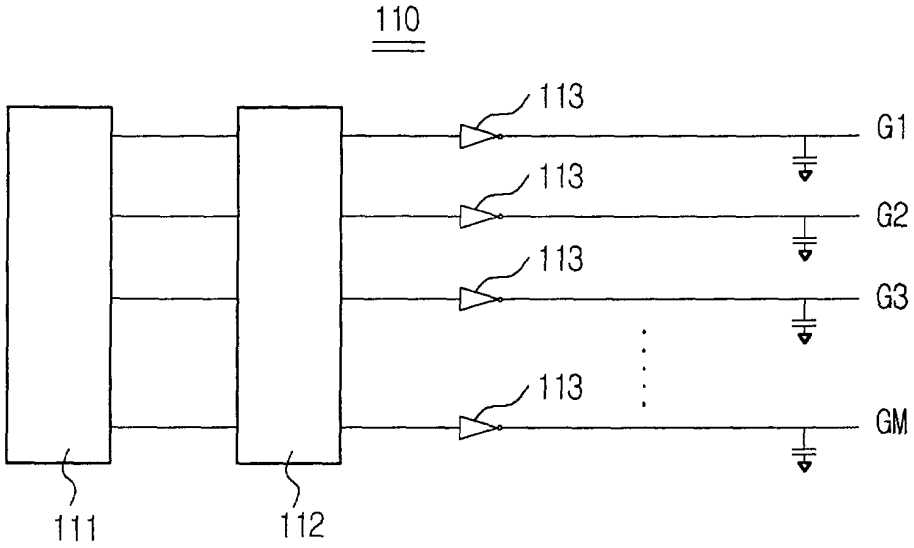

Figure 2

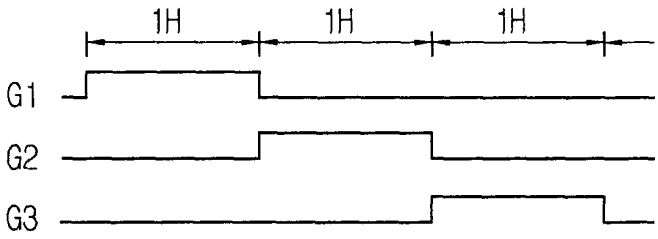

Figure 3

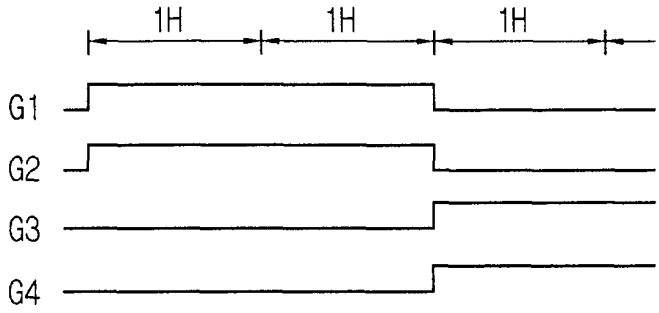

Figure 4

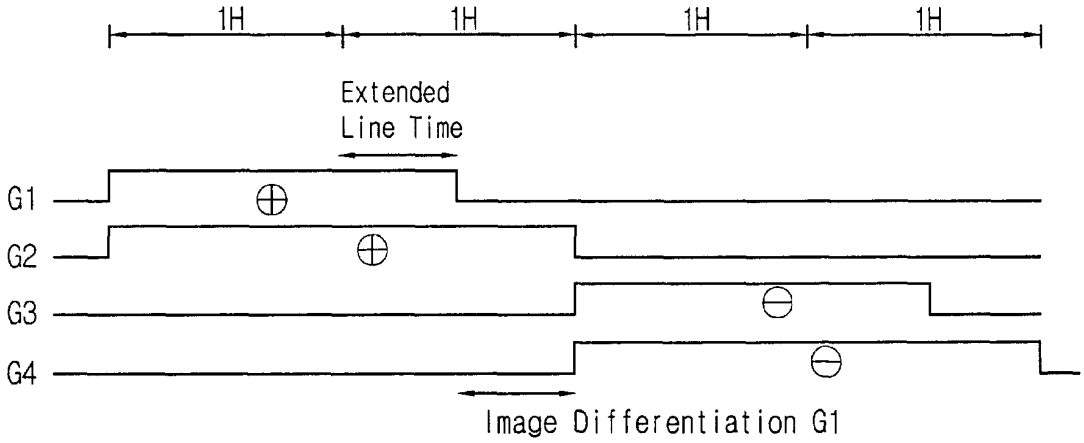

Figure 5

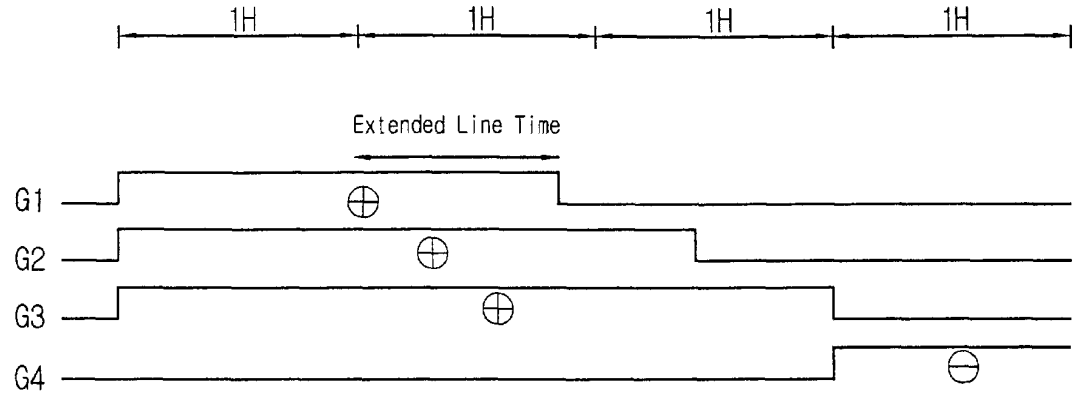

Figure 6

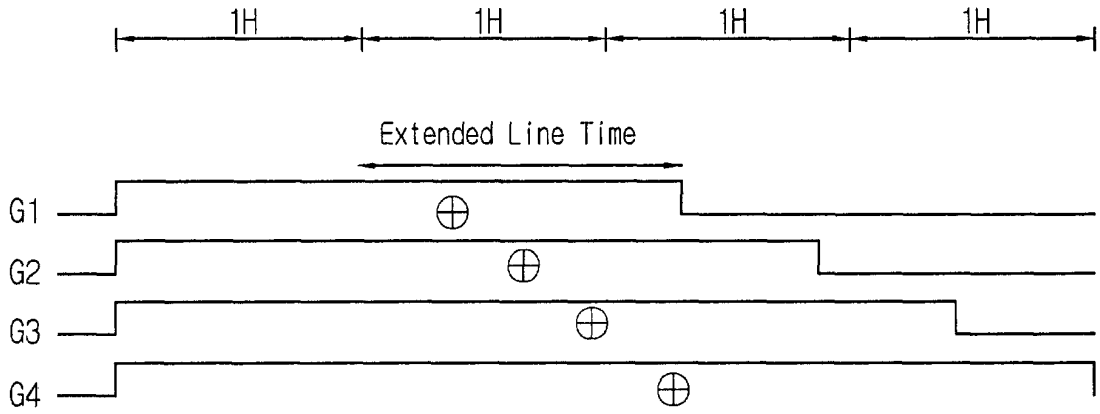

Figure 7

(N)th Frame

−	+	−	+	−	+
−	+	−	+	−	+
+	−	+	−	+	−
+	−	+	−	+	−

(N+1)th Frame

+	−	+	−	+	−
+	−	+	−	+	−
−	+	−	+	−	+
−	+	−	+	−	+

Figure 8

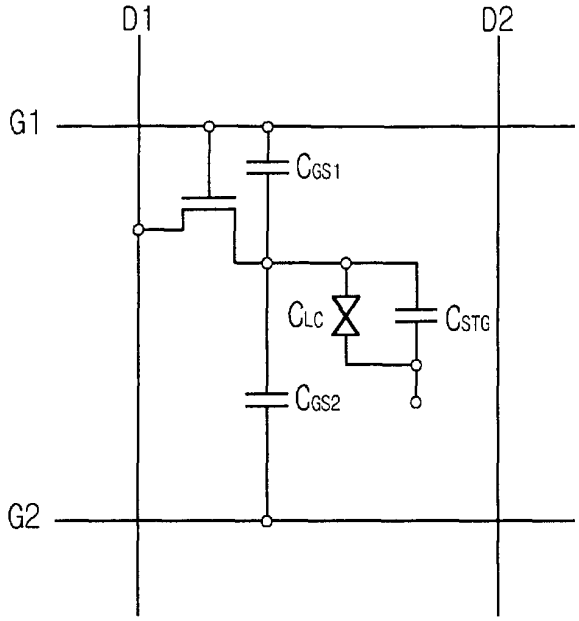

Figure 9

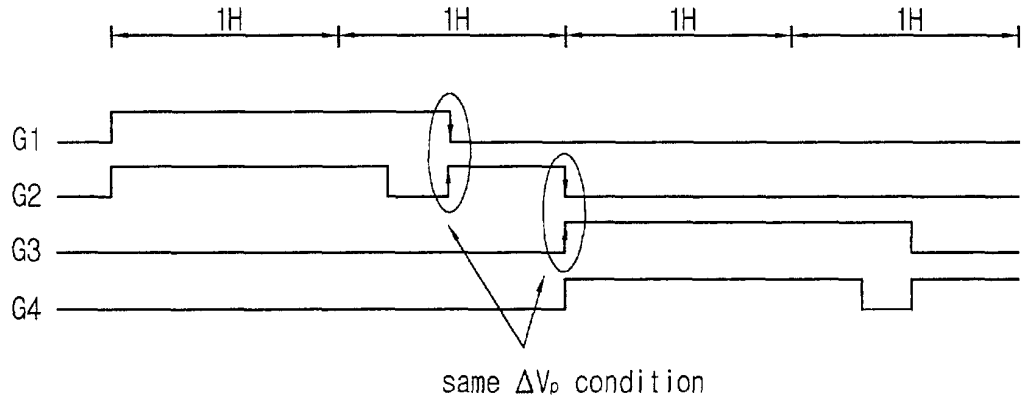

Figure 10

专利名称(译)	液晶显示装置的栅极的驱动方法		
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申请号	JP2001270725	申请日	2001-09-06
[标]申请(专利权)人(译)	権 五敬		
申请(专利权)人(译)	権 五敬		
[标]发明人	権五敬		
发明人	権 五敬		
IPC分类号	G09G3/36 G02F1/133 G09G3/20		
CPC分类号	G09G2320/0219 G09G3/3614 G09G2310/0205 G09G2320/0223 G09G3/3648		
FI分类号	G09G3/36 G02F1/133.550 G09G3/20.621.A G09G3/20.622.Q G09G3/20.624.B		
F-TERM分类号	2H093/NC09 2H093/ND33 2H093/ND36 5C006/AC22 5C006/BB16 5C006/BC03 5C006/FA15 5C080/AA10 5C080/BB05 5C080/DD07 5C080/DD08 5C080/FF11 5C080/FF12 5C080/JJ02 5C080/JJ03 5C080/JJ04		
优先权	1020000053555 2000-09-08 KR		
其他公开文献	JP4776830B2 JP2003084716A		

摘要(译)

一种通过同时驱动多条栅极线并使扫描信号的下降时间不同的方法来驱动液晶显示装置的栅极的方法，该方法能够延长线时间而不降低分辨率。 要做。 根据本发明的一个方面，在液晶显示装置中，多条栅极线同时被施加有上升的扫描信号，并且扫描信号的下降时间彼此不同，从而多条栅极线被分开。 在同时驱动栅极线的同时，图像信号可以在不同的下降时间被相应栅极线的像素采样。 此外，本发明的方法是驱动液晶显示装置的栅极线的方法，其中至少两个或更多栅极线同时被施加下降扫描信号，并且扫描信号的上升时间彼此不同。 通过这样做，在同时驱动多条栅极线的同时，可以在不同的上升时间通过对应的栅极线的像素采样图像信号，并且可以延长线时间。 [选择图]图10