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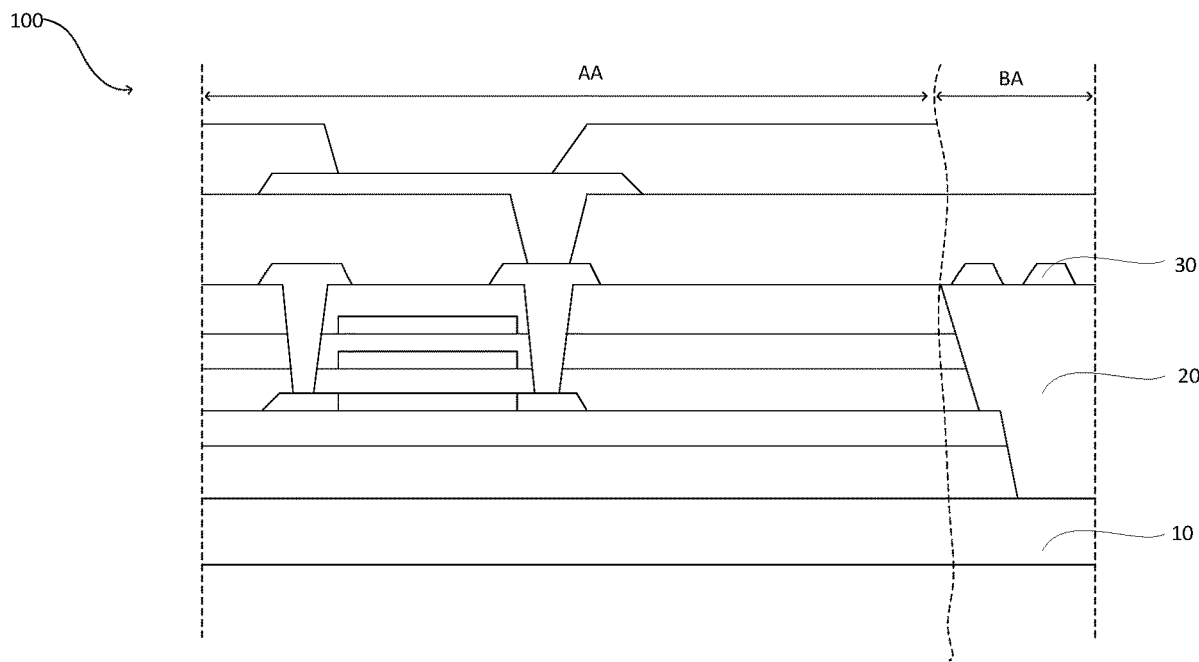
(57) **ABSTRACT**

Array substrate, an organic light emitting diode (OLED) display panel and a display device are provided with a flexible substrate, an water- and oxygen-resistant layer, a signal line layer and a flattening layer that are laminated in a bending region of the array substrate. signal transmission lines formed by patterning the signal line layer are formed on the water- and oxygen-resistant layer. By manufacturing the signal line layer of the bending region on the water- and oxygen-resistant layer and filling with the flattening layer, the problem of electrical performance of signal lines, caused by water and oxygen permeating the signal line layer through organic photoresist, is alleviated.

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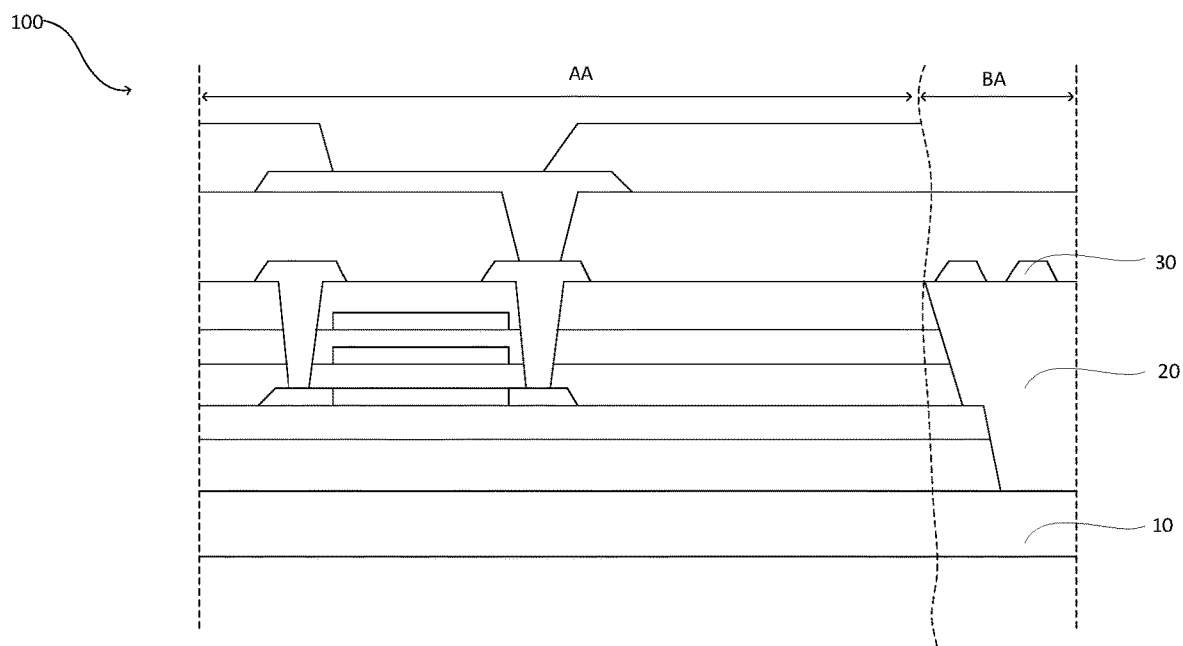


FIG. 1

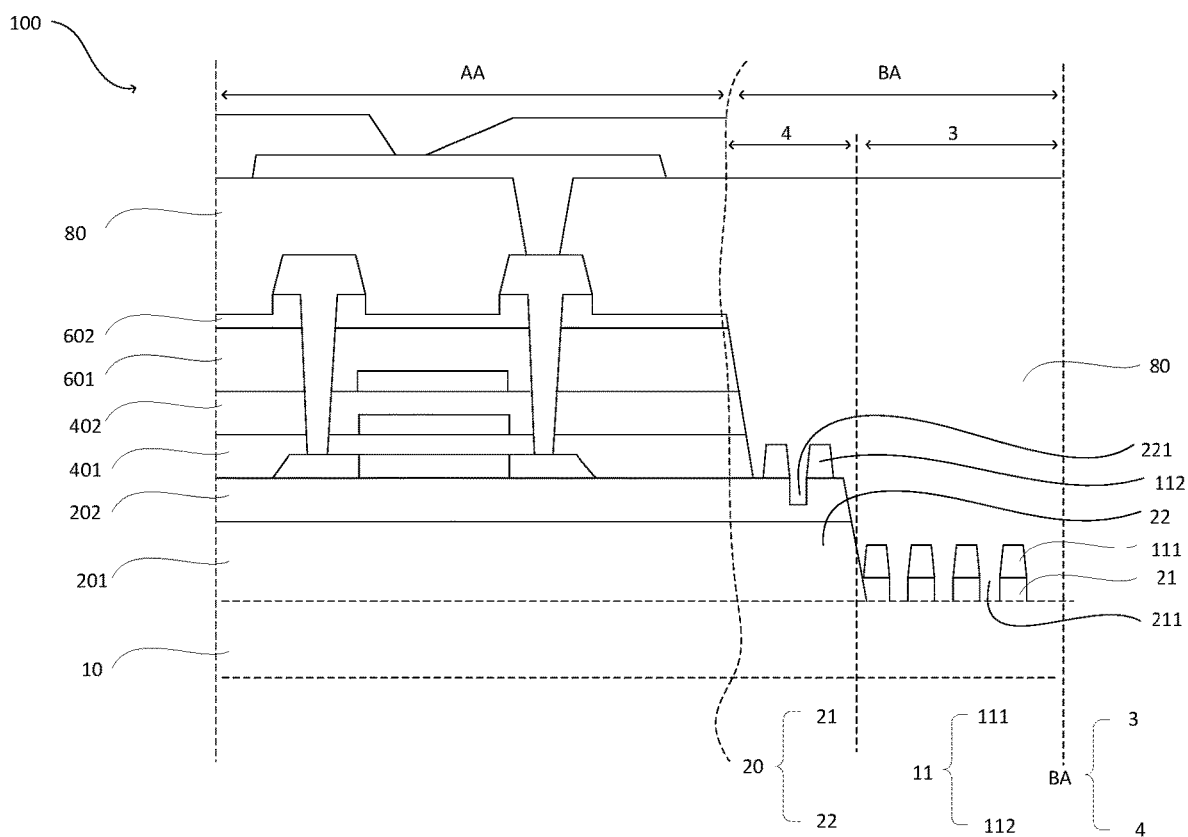


FIG. 2

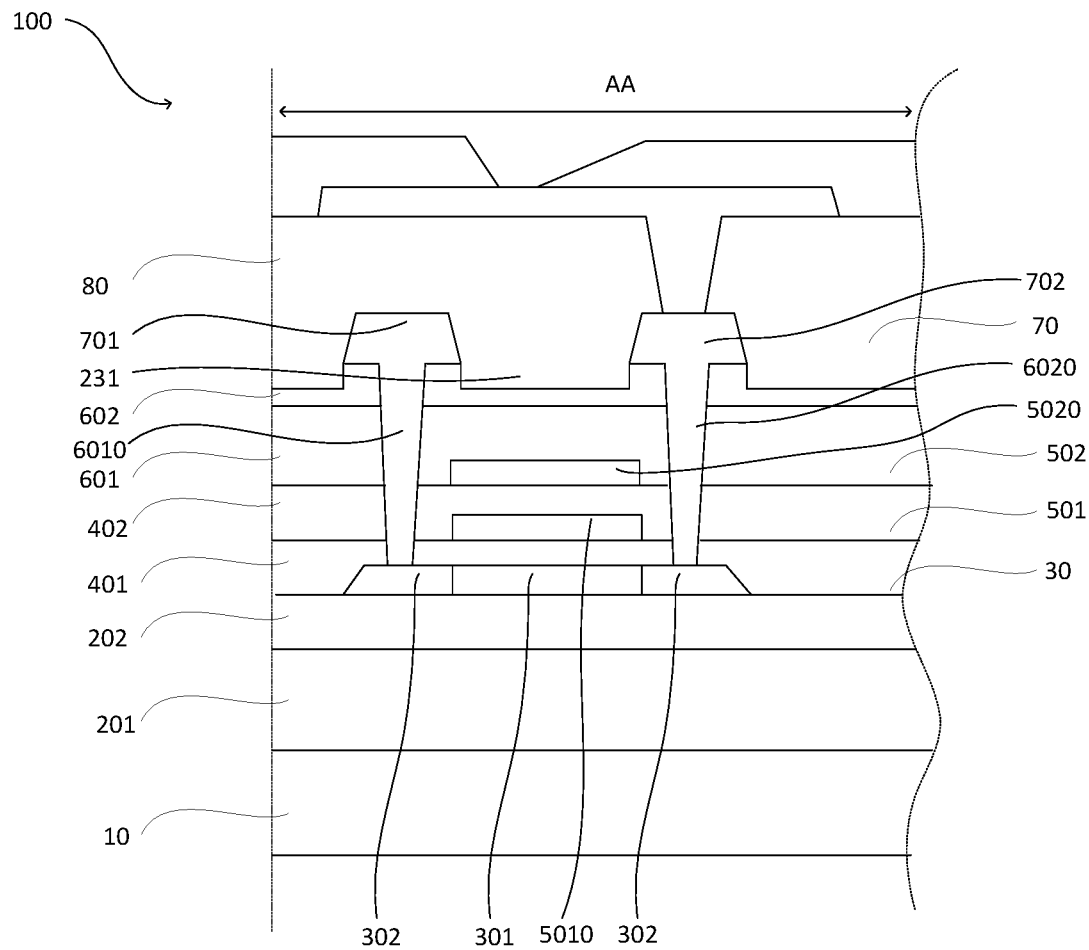


FIG. 3

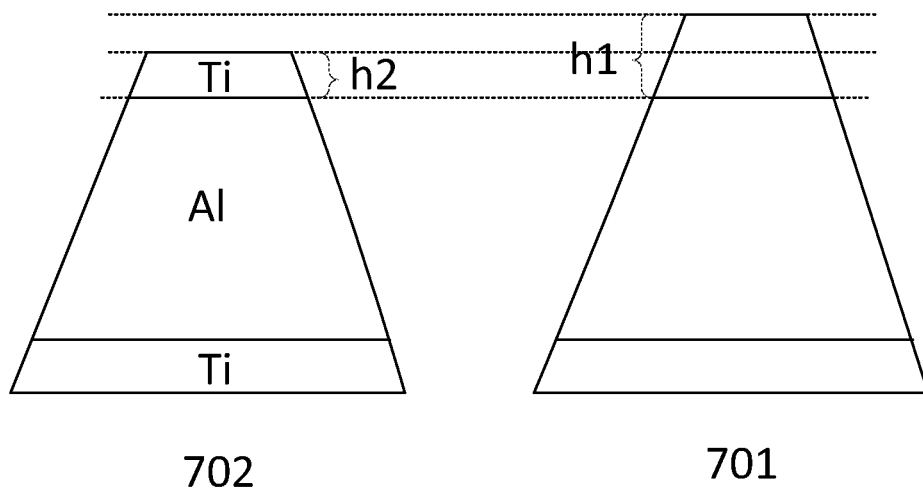


FIG. 4

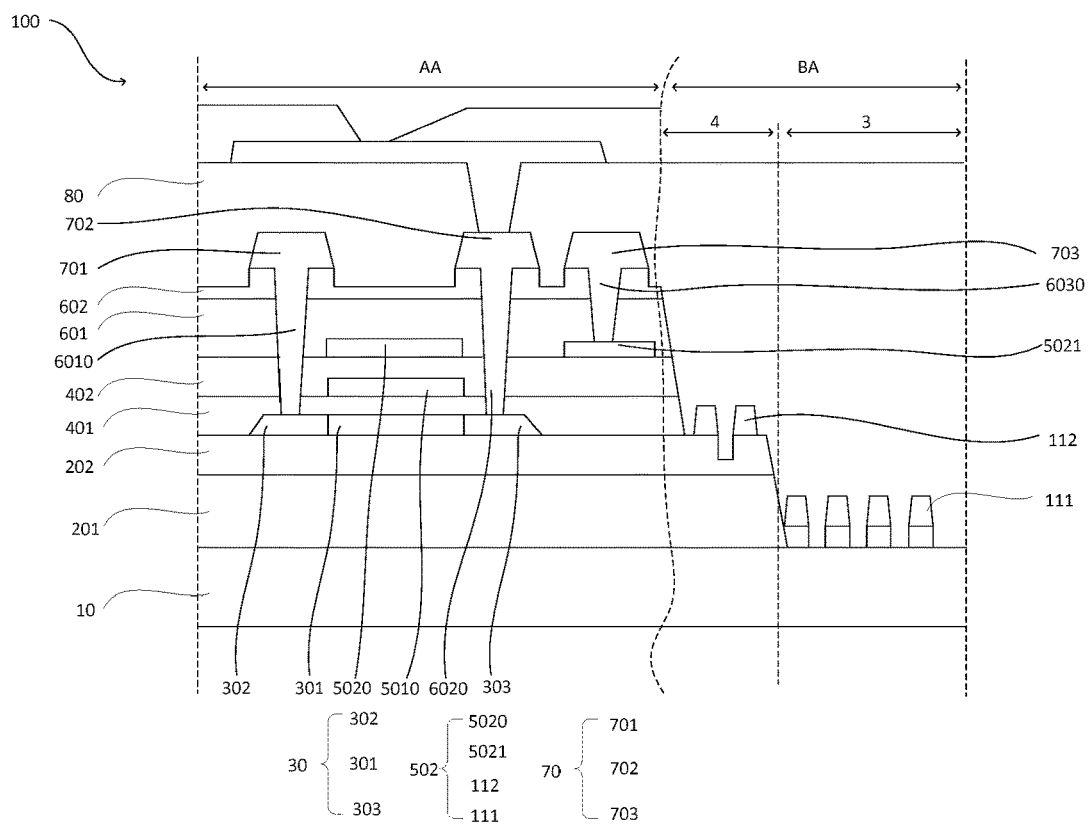


FIG. 5

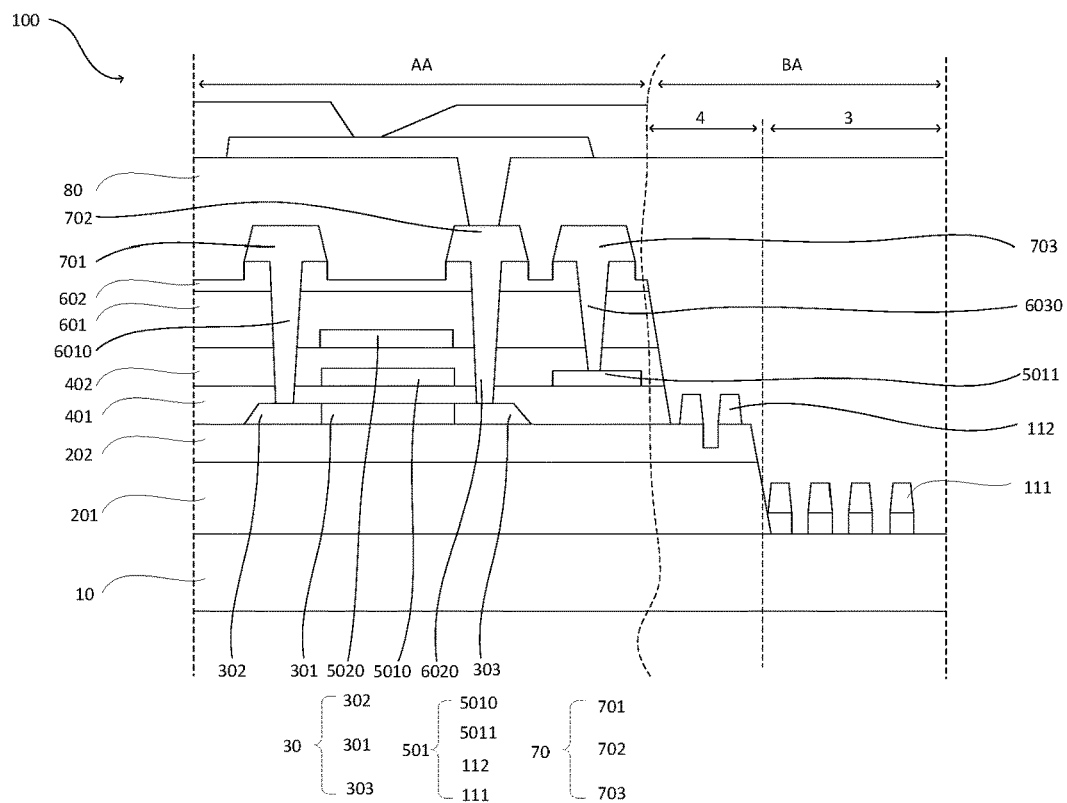


FIG. 6

## ARRAY SUBSTRATE, OLED DISPLAY PANEL AND DISPLAY DEVICE

### FIELD OF THE DISCLOSURE

[0001] The present application relates to display technologies, and more particularly to an array substrate, an organic light emitting diode (OLED) display panel and a display device.

### DESCRIPTION OF RELATED ARTS

[0002] In existing display devices, in order to improve a screen ratio, a bending region is generally formed outside a display region and is bent toward a rear face of a panel at a stage of cell process. To increase bending durability, inorganic layers in the bending region are generally removed entirely to form openings which are filled by organic photoresist. After that, signal lines are deposited above the organic photoresist and are patterned, and then a flattening layer is deposited above the signal lines. As shown in FIG. 1, in this design, a signal line layer 30 in a bending region BA directly contacts an organic photoresist layer 20 which directly contacts a flexible substrate 10. This causes water and oxygen contained in the flexible substrate 10 to permeate the signal line layer 30 through the organic photoresist layer 20, thereby affecting electrical performance of the signal lines.

[0003] Accordingly, there is a need to solve the problems in the existing display devices.

### SUMMARY

[0004] The present application provides an array substrate, an OLED display panel and a display device, for alleviating the technical problem of electrical performance of signal lines, caused by water and oxygen permeating a signal line layer through organic photoresist in existing display devices.

[0005] To solve above problems, the technical solutions provide in the present application are described below.

[0006] Embodiments of the present application provide an array substrate, including the following elements in a bending region:

[0007] a flexible substrate

[0008] a water- and oxygen-resistant layer, formed on the flexible substrate;

[0009] a signal line layer, formed on the water- and oxygen-resistant layer and patterned to form signal transmission lines;

[0010] a flattening layer, formed on the signal line layer and the water- and oxygen-resistant layer.

[0011] In the array substrate provided in the embodiments of the present application, the bending region includes a first bending region and a second bending region;

[0012] wherein in the display region, the array substrate includes a barrier layer formed on the flexible substrate; and

[0013] wherein the barrier layer extends to the first bending region to form the water- and oxygen-resistant layer.

[0014] In the array substrate provided in the embodiments of the present application, in the first bending region, film layer thickness of the water- and oxygen-resistant layer is less than film layer thickness of the barrier layer.

[0015] In the array substrate provided in the embodiments of the present application, the water- and oxygen-resistant layer is formed with a plurality of first slots in corresponding

regions of the patterned signal line layer not forming the signal transmission lines, and the flattening layer fills the first slots.

[0016] In the array substrate provided in the embodiments of the present application, a part of or all of the first slots penetrate the barrier layer.

[0017] In the array substrate provided in the embodiments of the present application, the array substrate further includes a buffer layer formed on the barrier layer in the display region,

[0018] wherein the barrier layer and the buffer layer extend to the second bending region to form the water- and oxygen-resistant layer.

[0019] In the array substrate provided in the embodiments of the present application, film layer thickness of the water- and oxygen-resistant layer in the second bending region is equal to a sum of film layer thickness of the barrier layer and film layer thickness of the buffer layer.

[0020] In the array substrate provided in the embodiments of the present application, the water- and oxygen-resistant layer is formed with a plurality of second slots in corresponding regions of the patterned signal line layer not forming the signal transmission lines, and the flattening layer fills the second slots.

[0021] In the array substrate provided in the embodiments of the present application, the depth of the second slots is less than film layer thickness of the buffer layer.

[0022] Embodiments of the present application further provide an OLED display panel, including:

[0023] an array substrate;

[0024] a light emitting functional layer, formed on the array substrate; and

[0025] an encapsulating layer, formed on the light emitting functional layer.

[0026] In the OLED display panel provided in the embodiments of the present application, the array substrate includes the following elements in a bending region:

[0027] a flexible substrate

[0028] a water- and oxygen-resistant layer, formed on the flexible substrate;

[0029] a signal line layer, formed on the water- and oxygen-resistant layer and patterned to form signal transmission lines;

[0030] a flattening layer, formed on the signal line layer and the water- and oxygen-resistant layer.

[0031] In the OLED display panel provided in the embodiments of the present application, the bending region includes a first bending region and a second bending region;

[0032] wherein in the display region, the array substrate includes a barrier layer formed on the flexible substrate; and

[0033] wherein the barrier layer extends to the first bending region to form the water- and oxygen-resistant layer.

[0034] In the OLED display panel provided in the embodiments of the present application, in the first bending region, film layer thickness of the water- and oxygen-resistant layer is less than film layer thickness of the barrier layer.

[0035] In the OLED display panel provided in the embodiments of the present application, the water- and oxygen-resistant layer is formed with a plurality of first slots in corresponding regions of the patterned signal line layer not forming the signal transmission lines, and the flattening layer fills the first slots.

[0036] In the OLED display panel provided in the embodiments of the present application, a part of or all of the first slots penetrate the barrier layer.

[0037] In the OLED display panel provided in the embodiments of the present application, the array substrate further includes a buffer layer formed on the barrier layer in the display region,

[0038] wherein the barrier layer and the buffer layer extend to the second bending region to form the water- and oxygen-resistant layer.

[0039] In the OLED display panel provided in the embodiments of the present application, film layer thickness of the water- and oxygen-resistant layer in the second bending region is equal to a sum of film layer thickness of the barrier layer and film layer thickness of the buffer layer.

[0040] In the OLED display panel provided in the embodiments of the present application, the water- and oxygen-resistant layer is formed with a plurality of second slots in corresponding regions of the patterned signal line layer not forming the signal transmission lines, and the flattening layer fills the second slots.

[0041] In the OLED display panel provided in the embodiments of the present application, the depth of the second slots is less than film layer thickness of the buffer layer.

[0042] Embodiments of the present application further provide a display device including the OLED display panel provided in embodiments of the present application.

[0043] Beneficial effects of the present application are described below. The present application provides an array substrate, an OLED display panel and a display device. In the bending region, the array substrate includes the flexible substrate, the water- and oxygen-resistant layer, the signal line layer and the flattening layer that are laminated. The signal transmission lines formed by patterning the signal line layer is formed on the water- and oxygen-resistant layer. The bending region includes a first bending region and a second bending region. The water- and oxygen-resistant layer forms first slots in the first bending region and forms second slots in the second bending region. The flattening layer fills the first slots and the second slots. By manufacturing the signal line layer of the bending region on the water- and oxygen-resistant layer and filling with the flattening layer, the present application alleviates the problem of electrical performance of signal lines, caused by water and oxygen permeating the signal line layer through organic photoresist.

#### DESCRIPTION OF DRAWINGS

[0044] For explaining the technical solutions used in the existing arts or the embodiments more clearly, the appended figures to be used in describing the existing arts or the embodiments will be briefly introduced in the following. Obviously, the appended figures described below are only some of the embodiments of the invention, and those of ordinary skill in the art can further obtain other figures according to these figures without making any inventive effort.

[0045] FIG. 1 is a schematic diagram showing a film layer structure of an array substrate in an existing art.

[0046] FIG. 2 is a schematic diagram illustrating a film layer structure according to a first embodiment provided in embodiments of the present application.

[0047] FIG. 3 is a schematic diagram illustrating a film layer structure in a display region provided in embodiments of the present application.

[0048] FIG. 4 is a contrast structural diagram of a source electrode and a drain electrode according to embodiments of the present application.

[0049] FIG. 5 is a schematic diagram illustrating a film layer structure according to a second embodiment provided in embodiments of the present application.

[0050] FIG. 6 is a schematic diagram illustrating a film layer structure according to a third embodiment provided in embodiments of the present application.

#### DETAILED DESCRIPTION

[0051] The following descriptions for the respective embodiments are specific embodiments capable of being implemented for illustrations of the present application with referring to the appended figures. In describing the present application, spatially relative terms such as “upper”, “lower”, “front”, “back”, “left”, “right”, “inner”, “outer”, “lateral”, and the like, may be used herein for ease of description as illustrated in the figures. Therefore, the spatially relative terms used herein are intended to illustrate the present application for ease of understanding, but are not intended to limit the present application. In the appended figures, units with similar structures are indicated by same reference numbers.

[0052] Embodiments of the present application can alleviate the technical problem of electrical performance of signal lines, caused by water and oxygen permeating the signal lines through organic photoresist in the existing art.

[0053] As shown in FIG. 2, in an bending region BA of an array substrate 100, the array substrate 100 provided in the present embodiment includes:

[0054] a flexible substrate 10;

[0055] a water- and oxygen-resistant layer 20, formed on the flexible substrate 10;

[0056] a signal line layer 11, formed on the water- and oxygen-resistant layer 20 and patterned to form signal transmission lines 111 and 112;

[0057] a flattening layer 80, formed on the signal line layer 11 and the water- and oxygen-resistant layer 20.

[0058] The present embodiment provides the array substrate which includes the flexible substrate, the water- and oxygen-resistant layer, the signal line layer and the flattening layer that are laminated in the bending region. The signal transmission line formed by patterning the signal line layer is formed on the water- and oxygen-resistant layer. The bending region includes a first bending region and a second bending region. The water- and oxygen-resistant layer has a plurality of first slots formed in the first bending region and a plurality of second slots formed in the second bending region. The flattening layer fills the first slots and the second slots. In the present application, the signal line layer of the bending region is fabricated on the water- and oxygen-resistant layer and is filled with the flattening layer. This alleviates the problem of signal line performance, caused by water and oxygen permeating the signal line layer through organic photoresist.

[0059] In an embodiment, as shown in FIG. 2, in the bending region BA, the array substrate 100 includes:

[0060] a flexible substrate 10;

[0061] a water- and oxygen-resistant layer 20 formed on the flexible substrate 10;

[0062] a signal line layer 11 formed on the water- and oxygen-resistant layer 20, the signal line layer 11 patterned to form signal transmission lines 111 and 112;

[0063] a flattening layer 80 formed on the signal line layer 11 and the water- and oxygen-resistant layer 20.

[0064] In an embodiment, the material of the flexible substrate 10 can be a flexible polymer such as polyimide.

[0065] In an embodiment, the bending region BA includes a first bending region 3 and a second bending region 4. A plurality of signal transmission lines 112 are disposed in the second bending region 4, distributed as a fan, and configured to connect traces in a display area to a driving circuit located in a peripheral area. Likewise, signal transmission lines 111 are disposed in the first bending region 3 and configured to connect a peripheral driving chip.

[0066] In an embodiment, in a display region AA, the array substrate 100 includes a barrier layer 201 formed on the flexible substrate 10 and a buffer layer 202 formed on the barrier layer 201.

[0067] In an embodiment, the material of the barrier layer 201 may include silicon oxide, which is primarily configured to prevent impurities in the flexible substrate 10 from spreading out and prevent invasion of outer water and oxygen.

[0068] In an embodiment, the material of the buffer layer 202 may include any one of silicon nitride and silicon oxide or their composition, which is primarily configured to buffer the pressure between film layer structures and may have a certain degree of ability to block water and oxygen.

[0069] In an embodiment, the barrier layer 201 in the display region AA extends to the first bending region 3 to form the water- and oxygen-resistant layer 21.

[0070] In an embodiment, film layer thickness of the water- and oxygen-resistant layer 21 is less than film layer thickness of the barrier layer 201.

[0071] In an embodiment, the water- and oxygen-resistant layer 21 may also be disposed individually without a need to extend the barrier layer 201 to the first bending region 3.

[0072] In an embodiment, in the first bending region 3, the water- and oxygen-resistant layer 21 is formed with a plurality of first slots 211 in corresponding regions of the patterned signal line layer 11 not forming the signal transmission lines 111. The flattening layer 80 fills the first slots 211.

[0073] In an embodiment, a part of or all of the first slots 211 penetrates the water- and oxygen-resistant layer 21 such that a part of the flattening layer 80 directly contacts the flexible substrate 10, thereby improving bending performance of the array substrate.

[0074] In an embodiment, the signal transmission lines 111 disposed on the water- and oxygen-resistant layer 21 are primarily configured to connect source signal lines, gate scan lines and power lines in the display region AA to an external driving chip.

[0075] In an embodiment, the barrier layer 201 and the buffer layer 202 in the display region AA extend to the second bending region 4 to form the water- and oxygen-resistant layer 22.

[0076] In an embodiment, film layer thickness of the water- and oxygen-resistant layer 22 is equal to a sum of film layer thickness of the barrier layer 201 and film layer thickness of the buffer layer 202.

[0077] In an embodiment, film layer thickness of the water- and oxygen-resistant layer 22 may also be less than a sum of film layer thickness of the barrier layer 201 and film layer thickness of the buffer layer 202.

[0078] In an embodiment, the water- and oxygen-resistant layer 22 may also be disposed individually without a need to extend the barrier layer 201 and the buffer layer 202 to the first bending region 3.

[0079] In an embodiment, the water- and oxygen-resistant layer 22 and the water- and oxygen-resistant layer 21 have different layer profiles. This is primarily for reducing a stage difference.

[0080] In an embodiment, in the second bending region 4, the water- and oxygen-resistant layer 22 is formed with a plurality of second slots 221 in corresponding regions of the patterned signal line layer 11 not forming the signal transmission lines 112. The flattening layer 80 fills the second slots 221.

[0081] In an embodiment, the depth of the second slots 221 is less than film layer thickness of the buffer layer 202. The second slots 221 are primarily configured to enhance bending performance of the array substrate.

[0082] In an embodiment, the depth of the second slots 221 may also be equal to film layer thickness of the buffer layer 202.

[0083] In an embodiment, the depth of the second slots 221 may also be greater than film layer thickness of the buffer layer 202.

[0084] In an embodiment, the signal transmission lines 112 disposed on the water- and oxygen-resistant layer 22 are primarily connected to the source signal lines, the gate scan lines and the power lines in the display region.

[0085] In an embodiment, as shown in FIG. 3, the display region AA further includes an active layer 20, a first gate insulating layer 401, a first gate electrode layer 501, a second gate insulating layer 402, a second gate electrode layer 502, a first insulating interlayer 601, a second insulating interlayer 602, a source drain electrode layer 70 and the flattening layer 80 that are laminated.

[0086] In an embodiment, the first gate electrode layer 501 and the second gate electrode layer 502 are patterned to form a first electrode plate 5010 and a second electrode plate 5020, respectively, which form a storage capacitor.

[0087] In an embodiment, the material of the gate electrode layer 40 may generally be any one of molybdenum, aluminum, aluminum-nickel alloy, molybdenum-tungsten alloy, chromium and copper, or a composition of several metal materials described above.

[0088] In an embodiment, the active layer 30 is patterned to form a channel region 301 and doped regions 302 and 303 located at two sides of the channel region 301. The doped regions 302 and 303 may be formed by ion doping at two sides of the channel region 301 with the first electrode plate 5010, formed by patterning the first gate electrode layer 501, that shields the channel region 301.

[0089] In an embodiment, the insulating interlayer 60 consists of two layers, in which the first insulating interlayer 601 provides the needed thickness of dielectric layer in general process and the second insulating interlayer 602 is an anti-etching layer that needs to be added. The contact interface materials of the two layers may be the same or different.

[0090] In an embodiment, the material of the insulating interlayer may be silicon nitride or silicon oxide, or their combination.

[0091] In an embodiment, as shown in FIGS. 2 and 3, the insulating interlayer 60 is patterned to form vias 6010 and 6020 in the display region and form openings (not shown) in the bending region.

[0092] In an embodiment, openings are formed in the bending region (not shown). The openings penetrate from the insulating interlayer 60 to the buffer layer 202 and the barrier layer 201.

[0093] In an embodiment, the source drain electrode layer 70 is patterned to form a source electrode 701 and a drain electrode 702 in the display region AA and form the signal transmission lines 111/112 in the bending region BA. The source electrode 701 is connected to the doped region 302 through the via 6010 and the source electrode 702 is connected to the doped region 303 through the via 6020.

[0094] In an embodiment, the source drain electrode layer 70 is further patterned to form slots including the first slots 211 and the second slots 221 formed in the bending region BA and a third slots 231 formed in the display region.

[0095] In an embodiment, the depth of the third slot 231 may be less than or greater than film layer thickness of the second insulating interlayer 602.

[0096] In an embodiment, the third slot 231 plays a role in reducing the thickness of film layers of the array substrate.

[0097] In an embodiment, as shown in FIG. 4, the source drain electrode layer 70 is a sandwich structure made by Ti/Al/Ti, in which the initial thickness of a third film layer Ti is h1. The thickness of the third film layer Ti of the source electrode 701 is h1 and the thickness of the third film layer Ti of the drain electrode 702 is h2, where h1 is greater than h2. As to the signal transmission lines in the bending region BA, the thickness of the third film layer Ti is equal to the initial thickness h1.

[0098] In an embodiment, as shown in FIG. 5, the array substrate 100 includes a display region AA and a bending region BA. The display region AA includes a flexible substrate 10, a barrier layer 201, a buffer layer 202, an active layer 30, a first gate insulating layer 401, a first gate electrode layer 501, a second gate insulating layer 402, a second gate electrode layer 502, a first insulating interlayer 601, a second insulating interlayer 602, a source drain electrode layer 70 and the flattening layer 80 that are laminated.

[0099] In an embodiment, the first gate electrode layer 501 is patterned to form a first electrode plate 5010 and the second gate electrode layer 502 is patterned to form a second electrode plate 5020. A storage capacitor is formed between the first electrode plate 5010 and the second electrode plate 5020.

[0100] In an embodiment, the second gate electrode layer 502 is patterned to form signal transmission lines 5021 in the display region AA and form signal transmission lines 111 and 112 in the bending region BA.

[0101] In an embodiment, the active layer 30 is patterned to form a channel region 301 and doped regions 302 and 303 located at two sides of the channel region. The doped regions 302 and 303 may be formed by ion doping at two sides of the channel region 301 with the first electrode plate 5010, formed by patterning the first gate electrode layer 501, that shields the channel region 301.

[0102] In an embodiment, the insulating interlayer 60 consists of two layers, in which the first insulating interlayer 601 provides the needed thickness of dielectric layer in general process and the second insulating interlayer 602 is

an anti-etching layer that needs to be added. The contact interface materials of the two layers may be the same or different.

[0103] In an embodiment, the insulating interlayer is patterned to form a first via 6010, a second via 6020 and a third via 6030.

[0104] In an embodiment, the material of the insulating interlayer may be silicon nitride or silicon oxide, or their combination.

[0105] In an embodiment, the source drain electrode layer 70 is patterned to form a source electrode 701, a drain electrode 702 and a data line 703.

[0106] In an embodiment, the source electrode 701 is connected to the doped region 302 through the first via 6010, the drain electrode 702 is connected to the doped region 303 through the second via 6020 and the data line 703 is connected to the signal transmission line 5021 through the third via 6030.

[0107] In an embodiment, as shown in FIG. 6, the array substrate 100 includes a display region AA and a bending region BA. The display region AA includes a flexible substrate 10, a barrier layer 201, a buffer layer 202, an active layer 30, a first gate insulating layer 401, a first gate electrode layer 501, a second gate insulating layer 402, a second gate electrode layer 502, a first insulating interlayer 601, a second insulating interlayer 602, a source drain electrode layer 70 and the flattening layer 80 that are laminated.

[0108] In an embodiment, the first gate electrode layer 501 is patterned to form a first electrode plate 5010 and the second gate electrode layer 502 is patterned to form a second electrode plate 5020. A storage capacitor is formed between the first electrode plate 5010 and the second electrode plate 5020.

[0109] In an embodiment, the first gate electrode layer 501 is patterned to form signal transmission lines 5011 in the display region AA and form signal transmission lines 111 and 112 in the bending region BA.

[0110] In an embodiment, the active layer 30 is patterned to form a channel region 301 and doped regions 302 and 303 located at two sides of the channel region. The doped regions 302 and 303 may be formed by ion doping at two sides of the channel region 301 with the first electrode plate 5010, formed by patterning the first gate electrode layer 501, that shields the channel region 301.

[0111] In an embodiment, the insulating interlayer 60 consists of two layers, in which the first insulating interlayer 601 provides the needed thickness of dielectric layer in general process and the second insulating interlayer 602 is an anti-etching layer that needs to be added. The contact interface materials of the two layers may be the same or different.

[0112] In an embodiment, the insulating interlayer is patterned to form a first via 6010, a second via 6020 and a third via 6030.

[0113] In an embodiment, the material of the insulating interlayer may be silicon nitride or silicon oxide, or their combination.

[0114] In an embodiment, the source drain electrode layer 70 is patterned to form a source electrode 701, a drain electrode 702 and a data line 703.

[0115] In an embodiment, the source electrode 701 is connected to the doped region 302 through the first via 6010, the drain electrode 702 is connected to the doped region 303

through the second via 6020 and the data line 703 is connected to the signal transmission line 5011 through the third via 6030.

[0116] In order to manufacture the array substrate shown in FIG. 2, the embodiments of the present application further provide a method for manufacturing an array substrate, which includes steps of:

[0117] S1: providing a flexible substrate and sequentially depositing a barrier layer and a buffer layer on the flexible substrate;

[0118] S2: depositing an active layer on the buffer layer, wherein the active layer is patterned to form doped regions and a channel region;

[0119] S3: forming a first gate insulating layer on the active layer, forming a first gate electrode layer on the first gate insulating layer and patterning the first gate electrode layer, forming the doped regions by ion doping for other regions except for the channel region by use of the patterned first gate electrode layer;

[0120] S4: forming a second gate insulating layer on the first gate electrode layer and the first gate insulating layer, wherein a second gate electrode layer is formed on the second gate insulating layer and is patterned;

[0121] S5: sequentially depositing a first insulating interlayer and a second insulating interlayer on the second gate electrode layer and the second gate insulating layer and patterning the first insulating interlayer and the second insulating interlayer to form vias used to connect to the doped regions in the display region and form a first opening and a second opening in the bending region, wherein the first opening penetrates toward the buffer layer to form a water- and oxygen-resistant layer of a second bending region and the second opening penetrates from the buffer layer to the barrier layer to form a water- and oxygen-resistant layer of a first bending region;

[0122] S6: depositing a source drain electrode layer consisting of three layers (Ti—Al—Ti) on the insulating interlayer and patterning the source drain electrode layer to form a source electrode and a drain electrode that connect to the doped regions in the display region, and form signal transmission lines in the bending region, wherein the thickness of a third film layer Ti of the signal transmission lines in the bending region is equal to the thickness of a third film layer Ti of the source electrode in the display region;

[0123] S7: in a case that photoresist is not removed after the source drain electrode layer is patterned, forming a first slot in the display region with a depth less than or greater than film layer thickness of the second insulating interlayer, forming second slots and third slots in the bending region, wherein the second slots are located in the second bending region and the depth of the second slots is less than film layer thickness of the water- and oxygen-resistant layer, wherein the third slots are located in the first bending region, and a part of or all of the third slots penetrate the water- and oxygen-resistant layer;

[0124] S8: depositing a flattening layer, wherein the flattening layer in the display region is formed on the source drain electrode layer and the insulating interlayer and is patterned to form a via for connecting to the drain electrode, wherein the flattening layer in the bending region is manufactured on the signal transmission lines and the water- and oxygen-resistant layer and fills the slots of the water- and oxygen-resistant layer.

[0125] The embodiments of the present application further provide an organic light emitting diode (OLED) display panel. The OLED display panel includes an array substrate, a light emitting functional layer manufactured on the array substrate and an encapsulating layer manufactured on the functional layer.

[0126] In an embodiment, in a bending region, the array substrate includes:

[0127] a flexible substrate

[0128] a water- and oxygen-resistant layer, formed on the flexible substrate;

[0129] a signal line layer, formed on the water- and oxygen-resistant layer and patterned to form signal transmission lines;

[0130] a flattening layer, formed on the signal line layer and the water- and oxygen-resistant layer.

[0131] In an embodiment, the bending region includes a first bending region and a second bending region. In a display region, the array substrate includes a barrier layer formed on the flexible substrate. The barrier layer extends to a part of the first bending region to form the water- and oxygen-resistant layer.

[0132] In an embodiment, in the first bending region, film layer thickness of the water- and oxygen-resistant layer is less than film layer thickness of the barrier layer.

[0133] In an embodiment, the water- and oxygen-resistant layer is formed with a plurality of first slots in corresponding regions of the patterned signal line layer not forming the signal transmission lines. The flattening layer fills the first slots.

[0134] In an embodiment, a part of or all of the first slots penetrate the barrier layer.

[0135] In an embodiment, in the display region, the array substrate further includes a buffer layer formed on the barrier layer.

[0136] wherein the barrier layer and the buffer layer extend to the second bending region to form the water- and oxygen-resistant layer.

[0137] In an embodiment, film layer thickness of the water- and oxygen-resistant layer in the second bending region is equal to a sum of film layer thickness of the barrier layer and film layer thickness of the buffer layer.

[0138] In an embodiment, the water- and oxygen-resistant layer is formed with second slots in corresponding regions of the patterned signal line layer not forming the signal transmission lines. The flattening layer fills the second slots.

[0139] In an embodiment, the depth of the second slots is less than film layer thickness of the buffer layer.

[0140] In an embodiment, the light emitting functional layer includes a pixel electrode layer, pixel definition layer, a luminescent material layer and a common electrode layer.

[0141] In an embodiment, the common electrode layer is a transparent conductive metal layer.

[0142] Embodiments of the present application further provide a display device including the OLED display panel according to above embodiments.

[0143] It can be known from above embodiments that:

[0144] The present application provides an array substrate and a manufacturing method thereof, an OLED display panel and a display device. In the bending region, the array substrate includes the flexible substrate, the water- and oxygen-resistant layer, the signal line layer and the flattening layer that are laminated. The signal transmission lines formed by patterning the signal line layer is formed on the

water- and oxygen-resistant layer. The bending region includes a first bending region and a second bending region. The water- and oxygen-resistant layer forms first slots in the first bending region and forms second slots in the second bending region. The flattening layer fills the first slots and the second slots. By manufacturing the signal line layer of the bending region on the water- and oxygen-resistant layer and filling with the flattening layer, the present application alleviates the problem of electrical performance of signal lines, caused by water and oxygen permeating the signal line layer through organic photoresist.

[0145] While the preferred embodiments of the present application have been illustrated and described in detail, various modifications and alterations can be made by persons skilled in this art. The embodiment of the present application is therefore described in an illustrative but not restrictive sense. It is intended that the present application should not be limited to the particular forms as illustrated, and that all modifications and alterations which maintain the spirit and realm of the present application are within the scope as defined in the appended claims.

1. An array substrate, comprising the following elements in a bending region:

- a flexible substrate
- a water- and oxygen-resistant layer, formed on the flexible substrate;
- a signal line layer, formed on the water- and oxygen-resistant layer and patterned to form signal transmission lines;
- a flattening layer, formed on the signal line layer and the water- and oxygen-resistant layer.

2. The array substrate according to claim 1, wherein the bending region comprises a first bending region and a second bending region;

wherein in the display region, the array substrate comprises a barrier layer formed on the flexible substrate; and

wherein the barrier layer extends to the first bending region to form the water- and oxygen-resistant layer.

3. The array substrate according to claim 2, wherein in the first bending region, film layer thickness of the water- and oxygen-resistant layer is less than film layer thickness of the barrier layer.

4. The array substrate according to claim 3, wherein the water- and oxygen-resistant layer is formed with a plurality of first slots in corresponding regions of the patterned signal line layer not forming the signal transmission lines, and the flattening layer fills the first slots.

5. The array substrate according to claim 4, wherein a part of or all of the first slots penetrate the barrier layer.

6. The array substrate according to claim 2, further comprising a buffer layer formed on the barrier layer in the display region,

wherein the barrier layer and the buffer layer extend to the second bending region to form the water- and oxygen-resistant layer.

7. The array substrate according to claim 6, wherein film layer thickness of the water- and oxygen-resistant layer in the second bending region is equal to a sum of film layer thickness of the barrier layer and film layer thickness of the buffer layer.

8. The array substrate according to claim 7, wherein the water- and oxygen-resistant layer is formed with a plurality of second slots in corresponding regions of the patterned

signal line layer not forming the signal transmission lines, and the flattening layer fills the second slots.

9. The array substrate according to claim 8, wherein the depth of the second slots is less than film layer thickness of the buffer layer.

10. An organic light emitting diode (OLED) display panel, comprising:

- an array substrate;
- a light emitting functional layer, formed on the array substrate; and
- an encapsulating layer, formed on the light emitting functional layer.

11. The OLED display panel according to claim 10, wherein the array substrate comprises the following elements in a bending region:

- a flexible substrate
- a water- and oxygen-resistant layer, formed on the flexible substrate;
- a signal line layer, formed on the water- and oxygen-resistant layer and patterned to form signal transmission lines;
- a flattening layer, formed on the signal line layer and the water- and oxygen-resistant layer.

12. The OLED display panel according to claim 11, wherein the bending region comprises a first bending region and a second bending region;

wherein in the display region, the array substrate comprises a barrier layer formed on the flexible substrate; and

wherein the barrier layer extends to the first bending region to form the water- and oxygen-resistant layer.

13. The OLED display panel according to claim 12, wherein in the first bending region, film layer thickness of the water- and oxygen-resistant layer is less than film layer thickness of the barrier layer.

14. The OLED display panel according to claim 13, wherein the water- and oxygen-resistant layer is formed with a plurality of first slots in corresponding regions of the patterned signal line layer not forming the signal transmission lines, and the flattening layer fills the first slots.

15. The OLED display panel according to claim 14, wherein a part of or all of the first slots penetrate the barrier layer.

16. The OLED display panel according to claim 12, wherein the array substrate further comprises a buffer layer formed on the barrier layer in the display region,

wherein the barrier layer and the buffer layer extend to the second bending region to form the water- and oxygen-resistant layer.

17. The OLED display panel according to claim 16, wherein film layer thickness of the water- and oxygen-resistant layer in the second bending region is equal to a sum of film layer thickness of the barrier layer and film layer thickness of the buffer layer.

18. The OLED display panel according to claim 17, wherein the water- and oxygen-resistant layer is formed with a plurality of second slots in corresponding regions of the patterned signal line layer not forming the signal transmission lines, and the flattening layer fills the second slots.

**19.** The OLED display panel according to claim **18**, wherein the depth of the second slots is less than film layer thickness of the buffer layer.

**20.** A display device, comprising the OLED display panel according to claim **10**.

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