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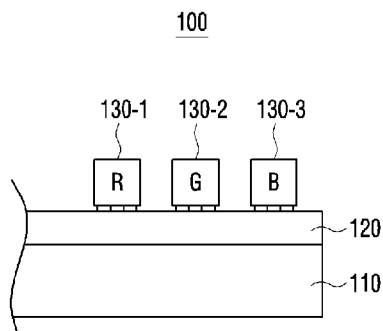
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(54) Title: LED DISPLAY PANEL AND REPAIRING METHOD



(57) **Abstract:** A display panel is provided. The display panel may include a glass, a driver formed on a first surface of the glass, and a circuit layer formed on a second surface of the glass. The circuit layer may include a plurality of pixel circuits configured to drive a plurality of micro light emitting diodes (LEDs) forming a plurality of pixels of the display panel; a plurality of driving circuits connected to the driver via wiring formed over a side surface of the glass, and configured to supply driving signals to the plurality of pixel circuits based on signals received from the driver; and a plurality of redundancy driving circuits connected to the plurality of respective driving circuits in parallel, the plurality of redundancy driving circuits having a same circuit structure as the plurality of respective driving circuits.

Description

Title of Invention: LED DISPLAY PANEL AND REPAIRING METHOD

Technical Field

- [1] The disclosure relates to a light emitting diode (LED) display panel, and more particularly, to a structure of an LED display panel in which driving circuits for driving micro LEDs can be easily repaired and a repairing method thereof.

Background Art

- [2] By using one or more LED display panels with no bezel, a plurality of modular display panels may be used in various ways, for example, to provide one large screen or to be separated from each other.

Disclosure of Invention

Technical Problem

- [3] The disclosure provides a display panel of which a damaged part can be easily restored, when the display panel is at least partially damaged due to an electrostatic discharge (ESD) or the like that may occur in the process of manufacturing a chip-on-glass (COG)-type modular display panel.

Solution to Problem

- [4] In accordance with an aspect of the disclosure, there is provided a display panel including a glass, a driver formed on a first surface of the glass, and a circuit layer formed on a second surface of the glass. The circuit layer may include a plurality of pixel circuits configured to drive a plurality of micro light emitting diodes (LEDs) forming a plurality of pixels of the display panel; a plurality of driving circuits connected to the driver via wiring formed over a side surface of the glass, and configured to supply driving signals to the plurality of pixel circuits based on signals received from the driver; and a plurality of redundancy driving circuits connected to the plurality of respective driving circuits in parallel, the plurality of redundancy driving circuits having a same circuit structure as the plurality of respective driving circuits.
- [5] The plurality of redundancy driving circuits are connected, via additional wiring, to the driver and to the respective plurality of pixel circuits that are connected to the plurality of driving circuits. The plurality of pixel circuits are configured to be driven based on driving signals received from the plurality of driving circuits and the plurality of redundancy driving circuits.
- [6] Based on a connection between a first driving circuit of the plurality of driving circuits and a first pixel circuit of the plurality of pixel circuits being opened, the first

pixel circuit is configured to be driven by a driving signal received from a first redundancy driving circuit among the plurality of redundancy driving circuits corresponding to the first driving circuit.

- [7] Based on a connection between a first redundancy driving circuit of the plurality of redundancy driving circuits and a first pixel circuit of the plurality of pixel circuits being opened, the first pixel circuit is configured to be driven based on a driving signal received from a first driving circuit among the plurality of driving circuits corresponding to the first redundancy driving circuit.
- [8] The plurality of redundancy driving circuits are connected, in an insulated welding form, to the driver and to the plurality of pixel circuits.
- [9] The plurality of micro LEDs form the plurality of pixels arranged in a matrix on the display panel, and the plurality of driving circuits are grouped into a first group of the plurality of driving circuits for driving corresponding pixel circuits for each row of the matrix and a second group of the plurality of driving circuits for driving corresponding pixel circuits for each column of the matrix.
- [10] The first group of the plurality of driving circuits are configured to sequentially supply driving signals for driving the pixel circuits for each row of the matrix based on a clock signal received from the driver, and the second group of the plurality of driving circuits are configured to sequentially select respective pixel circuits corresponding to red (R), green (G) and blue (B) sub-pixels that form each pixel included in a row to which driving signals are supplied from the first group based on the clock signal received from the driver, and sequentially supply data signals received from the driver to the selected pixel circuits.
- [11] The circuit layer may further include an electrostatic discharge (ESD) circuit configured to prevent static electricity of the display panel and a redundancy ESD circuit corresponding to the ESD circuit.
- [12] In accordance with an aspect of the disclosure, there is provided a method of manufacturing a display panel. The method may include forming a circuit layer on a first surface of a glass, the circuit layer including a plurality of pixel circuits, a plurality of driving circuits configured to drive the plurality of pixel circuits, and a plurality of redundancy driving circuits connected in parallel to the plurality of driving circuits with a same circuit structure; forming wiring lines connected from the plurality of driving circuits on the first surface of the glass through a side surface of the glass to a second surface of the glass; forming a plurality of micro light emitting diodes (LEDs) on the circuit layer to be driven by the plurality of pixel circuits; and forming a driver on the second surface of the glass to be electrically connected to the wiring lines connected to the plurality of driving circuits.
- [13] The method may further include, based on an abnormality occurring in a first driving

circuit of the plurality of driving circuits, opening a connection between the first driving circuit and a first pixel circuit among the plurality of pixel circuits connected to the first driving circuit, and the first pixel circuit may be configured to be driven based on a driving signal received from a first redundancy driving circuit among the plurality of redundancy driving circuits corresponding to the first driving circuit.

- [14] The method may further include, based on an abnormality occurring in a first redundancy driving circuit of the plurality of redundancy driving circuits, opening a connection between the first redundancy driving circuit and a first pixel circuit among the plurality of pixel circuits connected to the first redundancy driving circuit, and the first pixel circuit is configured to be driven based on a driving signal received from a first driving circuit among the plurality of driving circuits corresponding to the first abnormal redundancy driving circuit.
- [15] The plurality of micro LEDs form the plurality of pixels arranged in a matrix on the display panel, and the forming of the circuit layer may further include forming a first group of the plurality of driving circuits configured to drive corresponding pixel circuits for each row of the matrix and a second group of the plurality of driving circuits configured to drive corresponding pixel circuits for each column of the matrix.
- [16] The forming of the circuit layer may further include forming the first group of the plurality of driving circuits to sequentially supply driving signals for driving the pixel circuits for each row of the matrix based on a clock signal received from the driver, and forming the second group of the plurality of driving circuits to sequentially select respective pixel circuits corresponding to red (R), green (G) and blue (B) sub-pixels that form each pixel included in a row to which driving signals are supplied from the first group of the plurality of driving circuits based on the clock signal received from the driver, and to sequentially supply data signals received from the driver to the selected pixel circuits.
- [17] The forming of the circuit layer may further include forming an electrostatic discharge (ESD) circuit configured to prevent static electricity of the display panel and a redundancy ESD circuit for the corresponding ESD circuit.

Advantageous Effects of Invention

- [18] The chip-on-glass (COG) type display panel according to the disclosure is advantageous in that even when a gate driver or a MUX circuit provided in a thin film transistor (TFT) layer on the glass is damaged due to an electrostatic discharge (ESD) in a manufacturing process thereof, redundancy circuits that have already been additionally provided in the TFT layer enable restoration in a simple way

Brief Description of Drawings

- [19] The above and other aspects, features and advantages of certain embodiments of the

disclosure will become more apparent from the following description, taken in conjunction with reference to the accompanying drawings, in which:

- [20] FIG. 1a is a diagram illustrating an example of a chip-on-glass (COG)-type display panel to which side wiring is applied according to an embodiment;
- [21] FIG. 1b is a block diagram schematically illustrating an active area of the COG-type display panel to which the side wiring is applied according to an embodiment;
- [22] FIG. 2a is a block diagram illustrating a structure of a display panel according to an embodiment;
- [23] FIG. 2b is a block diagram illustrating a structure of a display panel according to an embodiment;
- [24] FIG. 3 is a diagram illustrating an example in which a display panel that includes a plurality of redundancy multiplexer (MUX) circuits for a plurality of MUX circuits according to an embodiment;
- [25] FIG. 4 is a graph illustrating a voltage applied to a pixel circuit when both specific MUX circuit and redundant MUX circuit operate or when only one of them operates according to an embodiment;
- [26] FIG. 5 is a diagram illustrating an example in which a display panel according to an embodiment of the disclosure includes a plurality of redundancy gate drivers for a plurality of gate drivers;
- [27] FIG. 6 is a diagram illustrating an example in which redundancy MUX circuits are connected to MUX circuits in an insulated welding form according to an embodiment;
- [28] FIG. 7a is a diagram illustrating an example in which redundancy gate drivers are connected to gate drivers in an insulated welding form according to an embodiment;
- [29] FIG. 7b is a diagram illustrating operations of the redundancy gate drivers when specific gate drivers are damaged in FIG. 7a according to an embodiment;
- [30] FIG. 8 is a diagram illustrating a circuit structure in which each redundancy gate driver may replace a respective gate driver according to an embodiment; and
- [31] FIG. 9 is a flowchart illustrating a manufacturing method of a display panel according to an embodiment.

Mode for the Invention

- [32] In the disclosure, when it is determined that the detailed description of the related well-known technology may unnecessarily obscure the gist of the disclosure, the detailed description thereof will be omitted. Also, an overlapping description of the same configuration will be omitted.
- [33] The suffixes "-or", "-er" and "unit" used for elements described herein may be assigned to facilitate understanding of the disclosure, and should not be construed as having distinct meanings or roles.

- [34] Terms used in the disclosure are used to describe embodiments, and are not intended to restrict and/or limit the disclosure. Singular forms are intended to include plural forms unless the context clearly indicates otherwise.
- [35] It is to be understood that term "include", "have" or the like used in the disclosure specifies the presence of features, numerals, steps, operations, elements, parts mentioned in the disclosure, or combinations thereof, but do not preclude the presence or addition of one or more other features, numerals, steps, operations, elements, parts, or combinations thereof.
- [36] The terms "first", "second", and the like used in the disclosure may modify various elements irrespective of sequence and/or importance, not limiting the elements. These expressions may be used to distinguish one element from another element.
- [37] It should further be understood that when an element (e.g. a first element) is referred to as being "(operatively or communicatively) coupled with/to" or "connected to" another element (e.g. a second element), it means that an element is coupled with/to or connected to another element directly or via an intervening element (e.g. a third element). On the other hand, it should be understood that when an element (e.g. a first element) is referred to as being "directly coupled with/to" or "directly connected to" another element (e.g. a second element), it means that there is no intervening element (e.g. a third element) between an element and another element.
- [38] Unless otherwise defined, the terms used for describing the embodiments of the disclosure have the same meanings as commonly understood by those skilled in the art.
- [39] The display panel of the disclosure may be installed and applied in a single unit to a wearable device, a portable device, a hand-held device, or any of various electronic products or electronics requiring a display, or may be applied in a plural number through assembling arrangement thereof in a matrix type to a display device such as a monitor for a personal computer (PC), a high-resolution TV, signage or an electronic display.
- [40] Hereinafter, a display panel according to various embodiments of the disclosure will be described in detail with reference to the accompanying drawings.
- [41] FIG. 1a is a side view illustrating an example of a COG-type display panel to which side wiring is applied according to an embodiment.
- [42] Referring to FIG. 1a, pixel circuits 10 for applying a voltage/current to light emitting diodes and driving circuits 20 for driving the pixel circuits 10 formed on a glass 5 may be connected to each other. In this case, the pixel circuits 10 and the driving circuits 20 may be included in the same circuit layer.
- [43] The light emitting diodes may be formed on the circuit layer including the pixel circuits 10 and the driving circuits 20.
- [44] In addition, the driving circuits 20 may be connected to a driver 30 on a rear surface

of the glass 5 via side wiring 40. Specifically, the side wiring 40 may be connected to each of the driving circuits 20 and the driver 30 through side wiring pads 45 and a rear pad 46.

[45] In FIG. 1a, the driving circuits 20 may be configured to collectively drive the pixel circuits 10 on a column or row basis, and the driver 30 may be configured to control operations of the driving circuits 20 based on image data and clock signals or the like.

[46] In FIG. 1a, an area corresponding to the circuit layer including the pixel circuits 10 and the driving circuits 20 may be collectively referred to as an active area.

[47] FIG. 1b is a block diagram illustrating a partial area of an active area according to an embodiment of the disclosure.

[48] Referring to FIG. 1b, driving circuits, such as gate drivers 20-1, 20-2, 20-3 and 20-4, for driving the pixel circuits, which are connected to the light emitting diodes arranged in a matrix form, for each row may be included in the active area. The driving circuits may further include circuits, such as multiplexer (MUX) circuits, for driving the pixel circuits for each column of corresponding light emitting diodes.

[49] Referring to FIG. 1b, an electrostatic discharge (ESD) circuit 50 for preventing static electricity of the display panel may be further included in the active area.

[50] Referring to FIG. 1b, the gate drivers 20-1, 20-2, 20-3 and 20-4 may receive a start signal "Start" and/or a clock signal "CLK" through the side wiring from the driver 30 disposed on the rear surface of the glass 5 to drive the plurality of pixel circuits.

[51] The display panel as in FIGS. 1a and/or 1b may be manufactured/implemented by forming the active area in which the pixel circuits 10 and the driving circuits 20 are included. For example, on the glass 5, the side wiring 40, the side wiring pads 45 and the rear pad 46 may be disposed, and then the plurality of light emitting diodes on a higher layer than that of the active area may be transferred. Thereafter, the driver 30 on the rear surface of the glass 5 may be connected to the rear pad 46 and the wiring 40.

[52] However, before the driver 30 is connected, there is possibility that an ESD may occur and enter the active area through the side wiring pads 45, the rear pad 46, or the like. Even though the ESD circuit 50 is provided on the active area as shown in FIG. 1b, at least some of the driving circuits may be damaged as a result of not coping with more powerful ESD. This is because, unlike the driver 30 that is capable of having a relatively high-performance ESD circuit, the active area, which corresponds to a relatively thin circuit layer, has a small space so that the ESD circuit 50 provided therein has limitations in its performance.

[53] This may result in poor image quality such as bright lines/dark lines for at least a portion of the display panel.

[54] Hereinafter, various embodiments of a display panel derived to solve the above-described problem will be described.

- [55] FIGS. 2a and 2b are block diagrams illustrating a structure of a display panel according to an embodiment of the disclosure. FIGS. 2a and 2b schematically illustrate a side view of a portion of the display panel according to an embodiment.
- [56] Referring to FIG. 2a, a display panel 100 may include a glass 110 made of a light transmissive material and a circuit layer 120 formed on one surface of the glass 110.
- [57] The circuit layer 120 may include a plurality of pixel circuits for driving a plurality of micro light emitting diodes (micro LEDs) 130-1, 130-2 and 130-3 included in each of a plurality of pixels of the display panel 100.
- [58] The plurality of pixel circuits may be electrically connected to of the plurality of respective micro LEDs. Each of the plurality of pixel circuits may include a pulse amplitude modulation (PAM) circuit, a pulse width modulation (PWM) circuit, a current source, a transistor, and the like.
- [59] Referring to FIG. 2a, the micro LEDs 130-1, 130-2 and 130-3 may be formed on one of the surfaces of the circuit layer 120 that is opposite to the surface contacting the glass 110. Each of the micro LEDs may be any one of red (R), green (G) and blue (B) sub-pixels, and the R, G and B sub-pixels may be combined to form one pixel.
- [60] The micro LEDs formed on the circuit layer 120 may be any of flip-chip type micro LEDs, lateral type micro LEDs, and vertical type micro LEDs.
- [61] The circuit layer 120 may also include driving circuits that supply driving signals for driving the plurality of pixel circuits based on signals received from a driver.
- [62] For example, the driving circuits may be connected to the driver formed on the other surface of the glass 110 via wiring formed over a side surface of the glass 110 to receive signals and generate driving signals based on the received signals. Specifically, the driving circuits may be respectively connected to data terminals of the driver through wiring lines formed on the side surface.
- [63] The circuit layer 120 may be formed as a thin film transistor (TFT) layer by implementing the plurality of pixel circuits and driving circuits as TFT.
- [64] The plurality of pixels configuring the display panel 100 may be arranged in a matrix form on the display panel 100. In addition, the driving circuits in the circuit layer 120 may include first driving circuits for driving corresponding pixel circuits for each row of the matrix and second driving circuits for driving corresponding pixel circuits for each column of the matrix.
- [65] Specifically, the first driving circuits may be gate drivers sequentially supplying driving signals for driving the plurality of pixel circuits for each row of the matrix based on one or more clock signals received from the driver. Here, the gate drivers may be arranged in a gate-in-panel form in which they are included in the circuit layer 120 within the panel.
- [66] The second driving circuits may be multiplexer (MUX) circuits configured to se-

quentially select respective pixel circuits corresponding to red (R), green (G) and blue (B) sub-pixels that constitute each pixel included in a row to which driving signals are supplied from the first driving circuits based on one or more clock signals received from the driver. The second driving circuits may sequentially supply data signals received from the driver to the selected pixel circuits.

[67] For example, the clock signals supplied from the driver to the first driving circuits and the clock signals supplied from the driver to the second driving circuits may be different from each other, and the data signals supplied to the second driving circuits may be data of one or more images to be displayed through the display panel 100.

[68] In addition, to solve the above-described problem, the circuit layer 120 may further include redundancy driving circuits connected to the respective driving circuits in parallel, and having the same circuit structure as the respective driving circuits.

[69] Specifically, the redundancy driving circuits may be connected via additional wiring lines through which the driving circuits receive signals from the driver and lines through which the driving circuits supply driving signals to the plurality of pixel circuits, and may have the same circuit structure as the driving circuits.

[70] The redundancy driving circuits will be described in more detail with respect to FIG. 2b.

[71] In FIG. 2b, a display panel 100' may include a side wiring 140 and a driver 150 in addition to the glass 110 and the circuit layer 120 described above with regard to the display panel 100 of FIG. 2a.

[72] Here, the driver 150 may be formed on the other surface of the glass 110, that is, on a surface opposite to the surface that is in contact with the circuit layer 120, while being connected to the circuit layer 120, via the side wiring 140.

[73] The driver 150 may include a clock supply circuit for supplying clock signals to the driving circuits in the circuit layer 120, a data driver (or a source driver) for supplying information on a data voltage (e.g., an amplitude setting voltage or a pulse width setting voltage) for each pixel or each sub-pixel of the display panel 100, or the like.

[74] In addition, the driver 150 may include a circuit structure for supplying, to the driving circuits, signals required for the driving circuits to drive the plurality of pixel circuits.

[75] The plurality of pixel circuits included in the circuit layer 120 may be driven basically based on driving signals received from the driving circuits and the redundancy driving circuits.

[76] When an abnormality occurs in any one of a driving circuit for driving specific pixel circuits and a redundancy driving circuit, it may be required that the pixel circuits be driven only through one of the operating driving circuits.

[77] The abnormality in any one of the driving circuits (or the redundancy driving

circuits) means that any two lines among lines connected to the driving circuits for signals or driving signals are short-circuited with respect to each other or one or more lines are opened. In addition, the abnormality may include a case where a connection between a source and a drain of a transistor included in the relevant driving circuit is opened. For example, there may be a case where the source and a gate are short-circuited or a case where the drain and the gate are short-circuited, or the like. However, the abnormality is not limited to the above-described examples, and may include various phenomena and events where the driving circuit does not operate normally.

- [78] When an abnormality occurs in any one of the driving circuits, it may be required that the abnormal driving circuit be stopped from operating, and the relevant pixel circuits be driven only through a redundancy driving circuit corresponding to the abnormal driving circuit. It is thus necessary to open all of the lines that are connected to the abnormal drive circuit for signals or driving signals.
- [79] As a result, when a connection between a driving circuit and a pixel circuit is opened, the pixel circuit may be driven based on a driving signal received from a redundancy driving circuit corresponding to the driving circuit to which the connection is opened.
- [80] Conversely, when an abnormality occurs in one of the redundancy driving circuits, and as a result a connection between the redundancy driving circuit and a pixel circuit is opened, the pixel circuit may be driven based on a driving signal received from one of the driving circuits corresponding to the redundancy driving circuit to which the connection is opened.
- [81] More specific examples will be described with reference to FIGS. 3, 4, and 5.
- [82] FIG. 3 is a diagram illustrating an example in which the display panel 100 according to an embodiment of the disclosure includes a plurality of redundancy MUX circuits for a plurality of MUX circuits. In FIG. 3, it may be assumed that the number of pixel columns of the display panel 100 is 480.
- [83] Referring to FIG. 3, the circuit layer 120 may include pixel circuit areas in which pixel circuits corresponding to pixels for each row are included, and may include a plurality of MUX circuits 121-1, 121-2, ..., and 121-480 for driving pixel circuits corresponding to pixels of each column.
- [84] Here, the MUX circuits 121-1, 121-2, ..., and 121-480 may receive respective data signals DATA 1, 2, 3, ..., and 480 from the driver 150. The data signals DATA 1, 2, 3, ..., and 480 may be data including information on images to be displayed.
- [85] In addition, the MUX circuits 121-1, 121-2, ..., and 121-480 may apply the data signals DATA 1, 2, 3, ..., and 480 to the plurality of pixel circuits according to clock signals MUX R, MUX G and MUX B for controlling respective driving timings of R, G and B sub-pixels.

- [86] However, FIG. 3 merely illustrates an example of signals for operating the MUX circuits, and is not intended to limit the type and the number of signals that the MUX circuits receive from the driver 30.
- [87] Referring to FIG. 3, the circuit layer 120 may further include redundancy MUX circuits 122-1, 122-2, ..., and 122-480 having not only the same input and output, but also the same circuit structure as the MUX circuits 121-1, 121-2, ..., and 121-480, respectively.
- [88] In this case, before the driver 30 is formed on the rear surface of the glass 110, even if any one of a specific MUX circuit and a redundancy MUX circuit is damaged, pixel circuits in the corresponding column may be controlled through the other one, thereby enabling an easy repair.
- [89] For example, as illustrated in FIG. 3, when there is no abnormality in any of the MUX circuit 121-1 and the redundancy MUX circuit 122-1, pixel circuits corresponding to pixels in a first column of the matrix may be driven by both the MUX circuit 121-1 and the redundancy MUX circuit 122-1 that are connected to each other in parallel.
- [90] On the other hand, referring to FIG. 3, when the MUX circuit 121-2 is damaged, a connection thereto may be opened so that the driver 30 and the pixel circuits are not connected to the damaged MUX circuit 121-2 during a process. As a result, pixel circuits corresponding to a second column may be driven through the redundancy MUX circuit 122-2. Accordingly, the problem may be solved by simply opening a connection to a relevant part without having to specifically repair the MUX circuit 121-2 itself.
- [91] In addition, if a redundancy MUX circuit is damaged rather than a MUX circuit, it is only required to open a connection to the damaged redundancy MUX circuit in a similar manner as described above. Referring to FIG. 3, when a redundancy MUX circuit 122-3 is damaged, it is still possible to drive pixel circuits corresponding to a third column through a MUX circuit 121-3 by opening a connection to the redundancy MUX circuit 122-3.
- [92] In FIG. 3, it may be required that a difference between magnitudes of voltages applied to pixel circuits in different columns should be minimized when the pixel circuits are driven through both the MUX circuit and the redundancy MUX circuit and when the pixel circuits are driven by only one of the MUX circuit and the redundancy MUX circuit.
- [93] In this regard, FIG. 4 is a graph illustrating voltages applied to pixel circuits when both a specific MUX circuit and a corresponding redundant MUX circuit included in the circuit layer 120 operate or when only one of them operates.
- [94] Referring to FIG. 4, it may be seen that the maximum magnitude of the voltage V_{data}

applied to the pixel circuits is substantially the same between when both the MUX circuit and the corresponding redundant MUX circuit operate and when only one of them operates.

[95] In addition, referring to FIG. 4, it may be seen that when both the MUX circuit and the redundant MUX circuit operate, it takes shorter time for V_{data} to reach the maximum/minimum value.

[96] FIG. 5 is a diagram illustrating an example in which the display panel 100 according to an embodiment of the disclosure includes a plurality of redundancy gate drivers for a plurality of gate drivers. In FIG. 5, it is assumed that the number of pixel rows of the display panel 100 is 270.

[97] Referring to FIG. 5, the circuit layer 120 includes pixel circuit areas in which pixel circuits corresponding to pixels for each column are included, and includes gate drivers 123-1, 123-2, ..., and 123-270 for driving pixel circuits corresponding to pixels for each column.

[98] Referring to FIG. 5, the gate drivers 123-1, 123-2, ..., and 123-270 may generate respective waveforms corresponding to timings for the gate drivers 123-1, 123-2, ..., and 123-270 to drive the pixel circuits, according to clock signals CLK 1, CLK2 and CLK 3, which the three gate drivers 123-1, 123-2 and 123-3 receive from the driver 30 respectively, and VGH (a direct current high voltage signal) and VGL (a direct current low voltage signal), which all of the gate drivers 123-1, 123-2, ..., and 123-270 receive from the driver 30.

[99] In this case, once the first gate driver 123-1 receives a start signal VST supplied from the driver 30, the gate drivers 123-1, 123-2, ..., and 123-270 may drive pixel circuits corresponding to the respective columns while sequentially transmitting signals from the first gate driver 123-1 until reaching the last gate driver 123-270.

[100] Meanwhile, FIG. 5 merely illustrates an example of signals for operating the gate drivers, and is not intended to limit the type and the number of signals that the gate drivers receive from the driver 30.

[101] Referring to FIG. 5, the circuit layer 120 may further include redundancy gate drivers 124-1, 124-2, ..., and 124-270 having not only the same input and output, but also the same circuit structure as the gate drivers 123-1, 123-2, ..., and 123-270, respectively.

[102] In this case, before the driver 30 is formed on the rear surface of the glass 110, even if any one of a specific gate driver or a corresponding redundancy gate driver is damaged, pixel circuits in the relevant row may be controlled through the other one, thereby enabling an easy repair.

[103] For example, as illustrated in FIG. 5, when none of the gate driver 123-1 and the redundancy gate driver 124-1 is damaged, pixel circuits corresponding to pixels in a first row of the matrix may be driven by both the gate driver 123-1 and the redundancy gate

driver 124-1 that are connected to each other in parallel.

[104] On the other hand, referring to FIG. 5, when the gate driver 123-270 is damaged, a connection thereto may be opened so that the driver 30 and the pixel circuits are not connected to the damaged gate driver 123-270 during a process. As a result, pixel circuits corresponding to a 270th row may be driven through the redundancy gate driver 124-270. That is, the problem may be solved by simply opening a connection to a relevant part without having to specifically repair the damaged gate driver 123-270 itself.

[105] However, if a redundancy gate driver is damaged rather than a gate driver, it is merely required to open a connection to the damaged redundancy gate driver likewise. For example, when the redundancy gate driver 124-3 is damaged, it is possible to drive pixel circuits corresponding to a third row through the gate driver 123-3 by opening a connection to the redundancy gate driver 124-3.

[106] Here, the arrangement of the driving circuits (gate drivers, redundancy gate drivers, MUX circuits and redundancy MUX circuits) and pixel circuits (within the pixel circuit areas) in the circuit layer 120 as illustrated in FIGS. 3 and 5 are merely an example, and are not limited thereto. The pixel circuits and the driving circuits may be arranged at various positions and in various manners in the circuit layer 120.

[107] In addition, the respective redundancy driving circuits for the driving circuits may be included in the same number as the driving circuits, and there is no requirement that the redundancy driving circuits for all of the driving circuits be included in the circuit layer 120. If the redundancy driving circuits for at least some of the driving circuits are included in the circuit layer 120, this may be considered as falling within the spirit of the disclosure.

[108] In addition, unlike the embodiments described with reference to FIGS. 3 to 5, the redundancy driving circuits may be connected, in an insulated welding form, to lines through which the driving circuits receive signals from the driver 150 and to lines through which the driving circuits supply driving signals to the plurality of pixel circuits.

[109] That is, metals for the lines described above may be welded to metals for the lines connected to the redundancy driving circuits with insulators interposed therebetween. If there is no abnormality in the driving circuits, the redundancy driving circuits do not operate and only the driving circuits operate, as long as there is no particular measure (e.g. removing the insulators in welded portions using a laser or the like).

[110] Hereinafter, it will be described in detail with reference to FIGS. 6, 7a, 7b and 8.

[111] FIG. 6 is a diagram illustrating an example in which the redundancy MUX circuits are connected to the MUX circuits in an insulated welding form. Although it is schematically illustrated in FIG. 6 that only one clock signal CLK is connected to the

circuit layer 120, a plurality of clock signals may be connected thereto.

- [112] Referring to FIG. 6, the circuit layer 120 includes n MUX circuits 121-1, ..., and 121-n and n redundancy MUX circuits 122-1, ..., and 122-n. In addition, it may be seen that each of the redundancy MUX circuits 122-1, ..., and 122-n is connected, in an insulated welding form, to a line for receiving a CLK signal from the driver 150 and to lines for the MUX circuits to supply driving signals to the plurality of pixel circuits.
- [113] If a MUX circuit 121-1 of the MUX circuits 121-1, ..., and 121-n is damaged before the driver 150 is connected, a connection to the damaged MUX circuit 121-1 may be opened, while removing an insulating layer of the welded portion where the corresponding redundancy MUX circuit 122-1 is connected.
- [114] As a result, pixel circuits corresponding to pixels in a first column may be driven using the redundancy MUX circuit 122-1 instead of the damaged MUX circuit 121-1.
- [115] FIG. 7a is a diagram illustrating an example in which the redundancy gate drivers are connected to the gate drivers in an insulated welding form. Unlike FIG. 6, FIG. 7a illustrates an embodiment in which there are two redundancy driving circuits for two driving circuits, rather than a redundancy driving circuit for each of the driving circuits.
- [116] Referring to FIG. 7a, the circuit layer 120 may include redundancy gate drivers 124-1 and 124-2 for specific gate drivers 123-1 and 123-2 among the gate drivers 123-1, 123-2, 123-3 and 123-4.
- [117] In this case, the gate drivers 123-1, 123-2, 123-3 and 123-4 may drive the plurality of pixel circuits using a start signal Start and a clock signal CLK (which may be a plurality of signals) received from the driver 150.
- [118] In contrast, the redundancy gate drivers 124-1 and 124-2 may be connected in an insulated welding form to lines for signals received from the driver 150. Thus, the redundancy gate drivers 124-1 and 124-2 do not operate unless insulators in their welded portions are removed.
- [119] Referring to FIG. 7a, it may be seen that the redundancy gate drivers 124-1 and 124-2 are connected to replace the entirety of the gate drivers 123-1 and 123-2 with the redundancy gate drivers 124-1 and 124-2, rather than replacing the gate drivers 123-1 and 123-2 individually.
- [120] FIG. 7b is a diagram illustrating operations of the redundancy gate drivers when the specific gate drivers are damaged in FIG. 7a.
- [121] Referring to FIG. 7b, when at least one of the gate drivers 123-1 and 123-2 is damaged and a connection thereto is opened, pixel circuits corresponding to first and second rows of the matrix may be driven through the redundancy gate drivers 124-1 and 124-2 by removing the insulators in the welded portions thereof for the lines that are connected to the redundancy gate drivers 124-1 and 124-2.

- [122] Referring to FIG. 8, unlike in FIG. 7a, each of the redundancy gate drivers 124-1 and 124-2 may be connected to replace each of the gate driver 123-1 or 123-2.
- [123] Unlike FIG. 7a, FIG. 8 is a diagram illustrates a circuit structure in which each redundancy gate driver may replace each gate driver.
- [124] In FIG. 8, a line 810 is added so that even though only one of the gate drivers 123-1 and 123-2 is damaged, it is required to replace both the gate drivers 123-1 and 123-2 with the redundancy gate drivers 124-1 and 124-2. However, FIG. 7a is advantageous in that a circuit structure thereof is simpler than that of FIG. 8.
- [125] Although FIG. 8 only shows one line 810 being added, this is only for explaining a schematic structure. The number of added lines may vary depending on the number of lines (signals) connected from the driver 150 to the redundancy gate drivers 124-1 and 124-2.
- [126] Meanwhile, with regard to all the above-described embodiments in which the circuit layer 120 includes one or more redundancy driving circuits, the circuit layer 120 may include one or more electrostatic discharge (ESD) circuits for preventing occurrence of static electricity in the display panel 100 and redundancy ESD circuits thereof.
- [127] The ESD circuit may be implemented as a diode, a zener diode, a ground-gate N-channel MOSFET (GGNMOS), or the like.
- [128] The ESD circuit may be connected to at least one of the lines through which the driver circuits receive signals from the driver 150 to protect the driver circuits.
- [129] In addition, the redundancy ESD circuits may be connected to the respective ESD circuits in parallel to replace an ESD circuit as the ESD circuit is damaged. In this case, the ESD circuits and the redundancy ESD circuits may be connected in an insulated welding form.
- [130] Examples thereof are ESD circuits 125-1 and 125-2 and redundancy ESD circuits 126-1 and 126-2 in FIG. 6, and ESD circuits 125'-1 and 125''-2 and redundancy ESD circuits 126'-1 and 126'-2 in FIG. 7a.
- [131] Meanwhile, it is supposed in the above-described embodiments that the driving circuits are gate drivers or MUX circuits, but at least one of the gate drivers and the MUX circuits may be included in the driver 150 to be connected directly to a pixel circuit through the side wiring 140. Alternatively, it may also be supposed that at least one of the clock supply circuit and the data driver, which are described as being included in the driver 150, is one of the driving circuits included in the circuit layer 120.
- [132] Hereinafter, a manufacturing method of a display panel according to the disclosure will be described with reference to FIG. 9. FIG. 9 is a flowchart illustrating a manufacturing method of a display panel according to an embodiment of the disclosure.
- [133] Referring to FIG. 9, in the manufacturing method, a circuit layer may be formed on

one surface of a glass. The circuit layer may include a plurality of pixel circuits and driving circuits supplying driving signals for driving the plurality of pixel circuits to the plurality of pixel circuits based on signals received from a driver (S910). The plurality of pixel circuits are circuits connected to respective micro LEDs, which constitute pixels of the display panel, to apply a current/voltage to the micro LEDs.

[134] In this case, the circuit layer may be formed to further include redundancy driving circuits having the same circuit structure as the driving circuits. However, there is no requirement that redundancy driving circuits be included for all of the driving circuits, and redundancy driving circuits may be provided for only some of the driving circuits.

[135] In this case, the redundancy driving circuits may be connected via additional wiring to lines through which the driving circuits receive signals from the driver and to lines through which the driving circuits supply driving signals to the plurality of pixel circuits.

[136] Meanwhile, the plurality of pixels of the display panel may be arranged in a matrix form. In this case, first driving circuits for driving corresponding pixel circuits for each row of the matrix and second driving circuits for driving corresponding pixel circuits for each column of the matrix may be formed in the circuit layer.

[137] Specifically, the first driving circuits may be formed as gate drivers for sequentially supplying driving signals for driving the plurality of pixel circuits for each row of the matrix based on a clock signal received from the driver.

[138] In addition, the second driving circuits may be formed as MUX circuits for sequentially selecting respective pixel circuits corresponding to red (R), green (G) and blue (B) sub-pixels that form pixels included in a row to which driving signals are supplied from the first driving circuits based on a clock signal received from the driver, and sequentially supplying data signals received from the driver to the selected pixel circuits.

[139] In addition, an electrostatic discharge (ESD) circuit for preventing static electricity of the display panel and a redundant ESD circuit for the ESD circuit may further be formed.

[140] Here, the redundancy driving circuits and the redundancy ESD circuit may be designed to be connected in an insulated welding form to other lines on the circuit layer.

[141] Then, lines connected from the driving circuits on one surface of the glass through a side surface of the glass to the other surface of the glass may be wired (S920).

[142] Thereafter, each of a plurality of pixels of the display panel may be disposed on the circuit layer, and a plurality of micro LEDs driven by the plurality of pixel circuits may be formed therein (S930). Specifically, the plurality of micro LEDs may be attached onto the circuit layer by applying a uniform pressure such that the plurality of micro

LEDs may be transferred evenly onto the circuit layer.

[143] In this case, the plurality of pixels may be arranged in a matrix form on the display panel.

[144] In addition, a driver may be formed on the other surface of the glass to be electrically connected to the wired lines (S940).

[145] When an abnormality occurs in one of the driving circuits before operation S940, a connection between the driving circuit and a pixel circuit connected to the driving circuit may be opened.

[146] As such, the relevant pixel circuit may be driven based on a driving signal received from a redundancy driving circuit corresponding to the abnormal driving circuit among the redundancy driving circuits.

[147] Alternatively, when an abnormality occurs in one of the redundancy driving circuits before operation S940, a connection between the redundancy driving circuit and a pixel circuit connected to the redundancy driving circuit may be opened.

[148] In this case, the corresponding pixel circuit may be driven based on a driving signal received from a driving circuit corresponding to the abnormal redundancy driving circuit among the driving circuits.

[149] In operation S910, if the redundancy driving circuits are connected in the insulated welding form to other lines on the circuit layer, there may be a slight offset. As such, when an abnormality occurs in one of the driving circuits before operation S940, insulators of welded portions, in which the redundancy driving circuit for the abnormal driving circuit is connected, may be removed, in addition to the opening of the connection between the driving circuit and the pixel circuit connected to the driving circuit.

[150] In this case, the relevant pixel circuit may be connected to the redundancy driving circuit corresponding to the abnormal driving circuit to be driven by the redundancy driving circuit.

[151] According to the various embodiments, each of the elements may be implemented as a single entity or a plurality of entities. The above-described sub elements may be partially omitted, or other sub elements may be further included in the various embodiments. Alternatively or additionally, after being integrated into a single entity, some of the elements may identically or similarly perform the respective functions as performed by the relevant elements before integration.

[152] According to the various embodiments, operations performed by modules, programs, or other elements may be executed sequentially, in parallel, repeatedly, or heuristically, or at least some of the operations may be executed in a different order or omitted, or other operations may be added.

[153] While embodiments of the disclosure have been illustratively described hereinabove,

various changes and modifications may be made by one having ordinary skill in the art without departing from the essential characteristics of the disclosure. Also, the embodiments of the disclosure are not intended to limit the spirit of the disclosure, but are to describe the spirit of the disclosure, and the spirit and the scope of the disclosure are not limited by the embodiments. Accordingly, the scope of the disclosure should be construed based on the following claims, and it is to be construed that all equivalents thereto fall within the scope of the disclosure.

Claims

- [Claim 1] A display panel comprising:
a glass;
a driver formed on a first surface of the glass; and
a circuit layer formed on a second surface of the glass, the circuit layer comprising:
a plurality of pixel circuits configured to drive a plurality of micro light emitting diodes (LEDs) forming a plurality of pixels of the display panel;
a plurality of driving circuits which are respectively connected to the driver via wiring formed over at least one side surface of the glass, and configured to supply driving signals to the plurality of pixel circuits based on signals received from the driver; and
a plurality of redundancy driving circuits connected to the plurality of respective driving circuits in parallel, the plurality of redundancy driving circuits having a same circuit structure as the plurality of respective driving circuits.
- [Claim 2] The display panel according to claim 1, wherein the plurality of redundancy driving circuits are connected, via additional wiring, to the driver and to the respective plurality of pixel circuits that are connected to the plurality of driving circuits, and
wherein the plurality of pixel circuits are configured to be driven based on driving signals received from the plurality of driving circuits and the plurality of redundancy driving circuits.
- [Claim 3] The display panel according to claim 1, wherein, based on a connection between a first driving circuit of the plurality of driving circuits and a first pixel circuit of the plurality of pixel circuits being opened, the first pixel circuit is configured to be driven by a driving signal received from a first redundancy driving circuit, among the plurality of redundancy driving circuits, corresponding to the first driving circuit.
- [Claim 4] The display panel according to claim 1, wherein, based on a connection between a first redundancy driving circuit of the plurality of redundancy driving circuits and a first pixel circuit of the plurality of pixel circuits being opened, the first pixel circuit is configured to be driven based on a driving signal received from a first driving circuit, among the plurality of driving circuits, corresponding to the first redundancy driving circuit.

- [Claim 5] The display panel according to claim 1, wherein the plurality of redundancy driving circuits are connected, in an insulated welding form, to the driver and to the plurality of pixel circuits.
- [Claim 6] The display panel according to claim 1, wherein the plurality of micro LEDs form the plurality of pixels arranged in a matrix on the display panel, and
wherein the plurality of driving circuits are grouped into a first group of the plurality of driving circuits for driving corresponding pixel circuits for each row of the matrix and a second group of the plurality of driving circuits for driving corresponding pixel circuits for each column of the matrix.
- [Claim 7] The display panel according to claim 6, wherein the first group of the plurality of driving circuits are configured to sequentially supply driving signals for driving the pixel circuits for each row of the matrix based on a clock signal received from the driver, and
wherein the second group of the plurality of driving circuits are configured to sequentially select respective pixel circuits corresponding to red (R), green (G) and blue (B) sub-pixels that form each pixel included in a row to which driving signals are supplied from the first group based on the clock signal received from the driver, and sequentially supply data signals received from the driver to the selected pixel circuits.
- [Claim 8] The display panel according to claim 1, wherein the circuit layer further comprises an electrostatic discharge (ESD) circuit configured to prevent static electricity of the display panel and a redundancy ESD circuit corresponding to the ESD circuit.
- [Claim 9] A method of manufacturing a display panel, the method comprising:
forming a circuit layer on a first surface of a glass, the circuit layer including a plurality of pixel circuits, a plurality of driving circuits configured to drive the plurality of pixel circuits, and a plurality of redundancy driving circuits connected in parallel to the plurality of driving circuits with a same circuit structure;
forming wiring lines connected from the plurality of driving circuits on the first surface of the glass through at least one side surface of the glass to a second surface of the glass, respectively;
forming a plurality of micro light emitting diodes (LEDs) on the circuit layer to be driven by the plurality of pixel circuits; and
forming a driver on the second surface of the glass to be electrically

connected to the wiring lines connected to the plurality of driving circuits.

[Claim 10]

The method according to claim 9, further comprising, based on an abnormality occurring in a first driving circuit of the plurality of driving circuits, opening a connection between the first driving circuit and a first pixel circuit among the plurality of pixel circuits connected to the first driving circuit,

wherein the first pixel circuit is configured to be driven based on a driving signal received from a first redundancy driving circuit among the plurality of redundancy driving circuits corresponding to the first driving circuit.

[Claim 11]

The method according to claim 9, further comprising, based on an abnormality occurring in a first redundancy driving circuit of the plurality of redundancy driving circuits, opening a connection between the first redundancy driving circuit and a first pixel circuit among the plurality of pixel circuits connected to the first redundancy driving circuit, wherein the first pixel circuit is configured to be driven based on a driving signal received from a first driving circuit among the plurality of driving circuits corresponding to the first abnormal redundancy driving circuit.

[Claim 12]

The method according to claim 9, wherein the plurality of micro LEDs form the plurality of pixels arranged in a matrix on the display panel, and

wherein the forming of the circuit layer further comprises forming a first group of the plurality of driving circuits configured to drive corresponding pixel circuits for each row of the matrix and a second group of the plurality of driving circuits configured to drive corresponding pixel circuits for each column of the matrix.

[Claim 13]

The method according to claim 12, wherein the forming of the circuit layer further comprises:

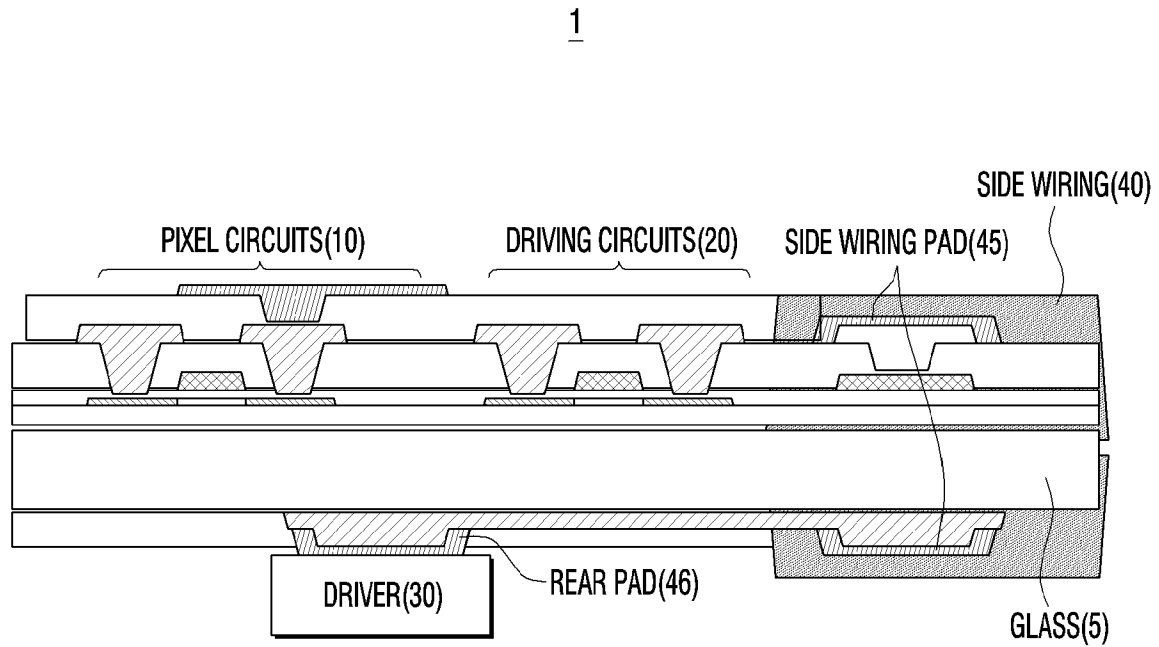
forming the first group of the plurality of driving circuits to sequentially supply driving signals for driving the pixel circuits for each row of the matrix based on a clock signal received from the driver, and forming the second group of the plurality of driving circuits to sequentially select respective pixel circuits corresponding to red (R), green (G) and blue (B) sub-pixels that form each pixel included in a row to which driving signals are supplied from the first group of the plurality of driving circuits based on the clock signal received from the

driver, and to sequentially supply data signals received from the driver to the selected pixel circuits.

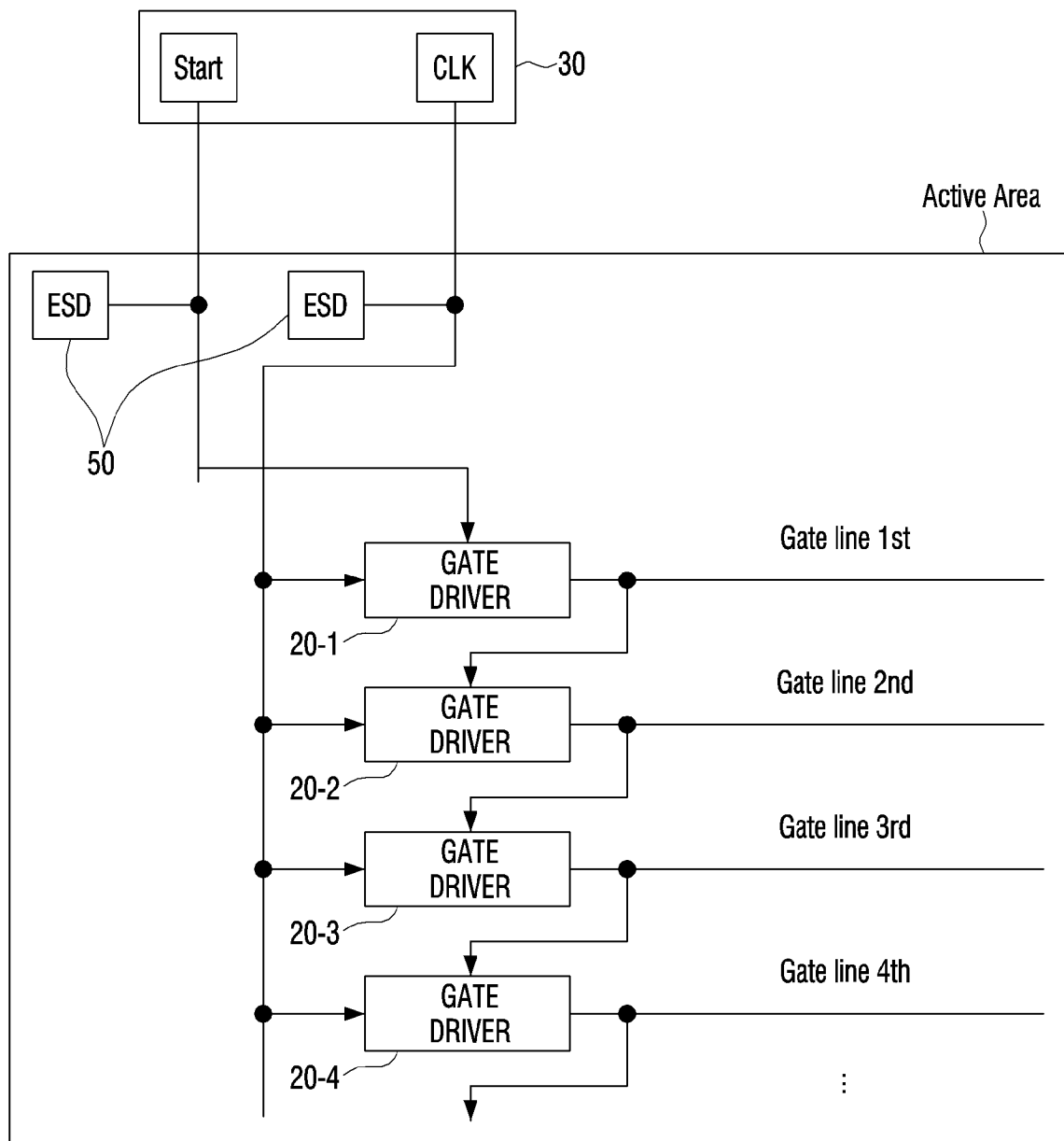
[Claim 14]

The method according to claim 9, wherein the forming of the circuit layer further comprises forming an electrostatic discharge (ESD) circuit configured to prevent static electricity of the display panel and a redundancy ESD circuit for the corresponding ESD circuit.

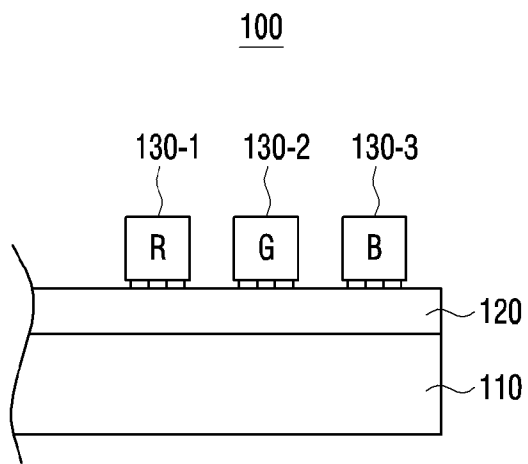
[Fig. 1a]



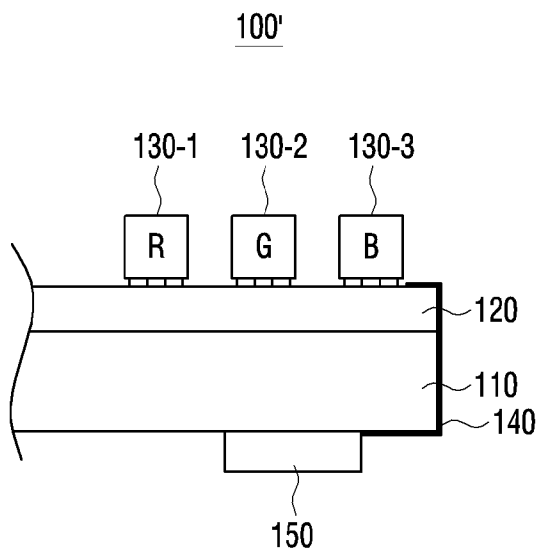
[Fig. 1b]



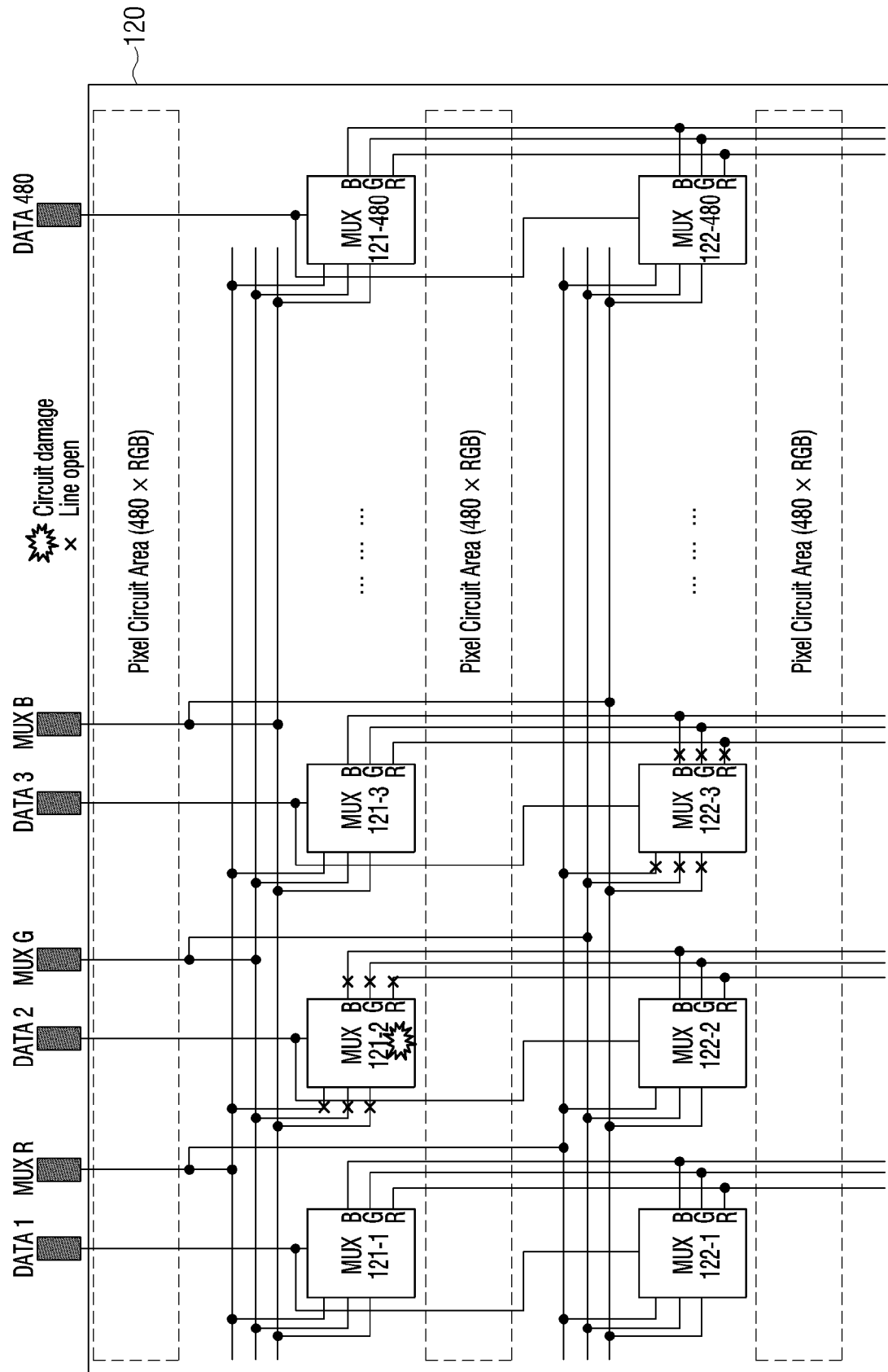
[Fig. 2a]



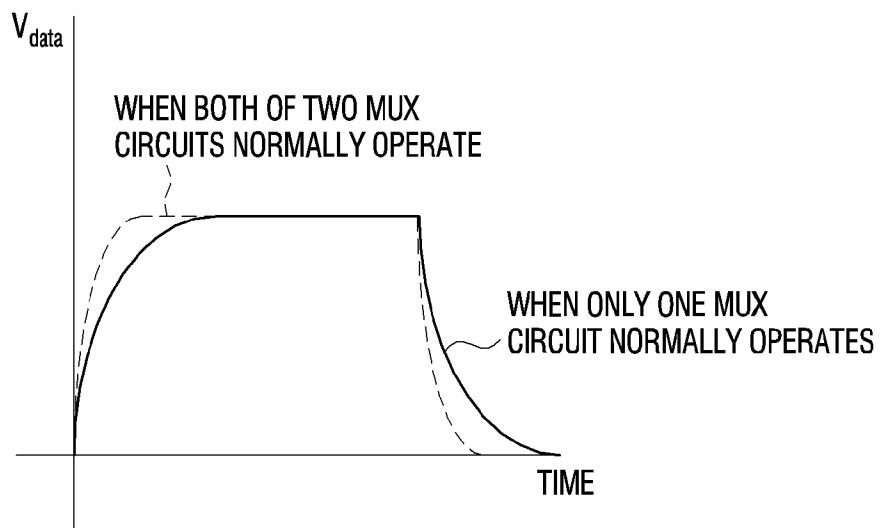
[Fig. 2b]



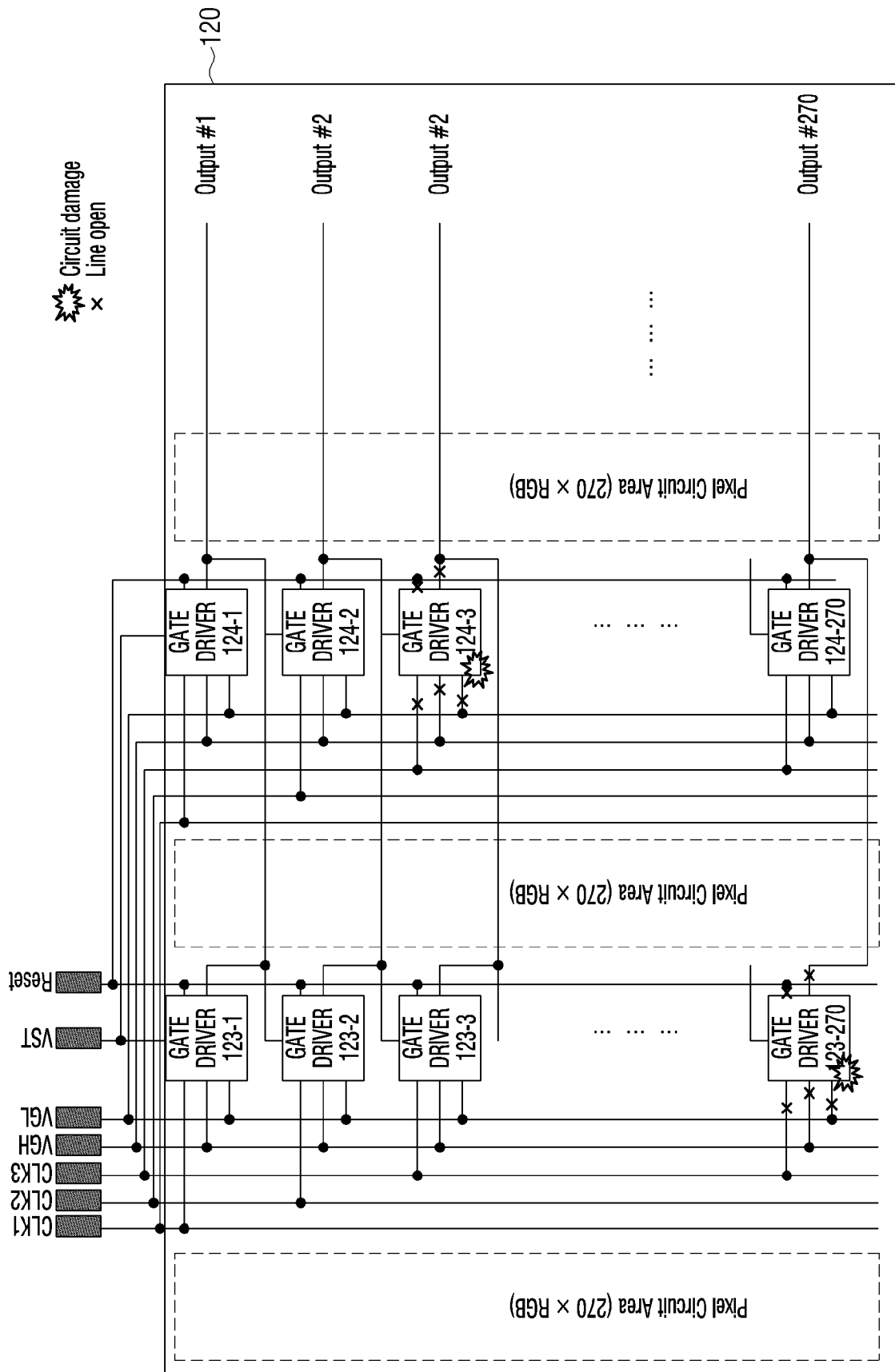
[Fig. 3]



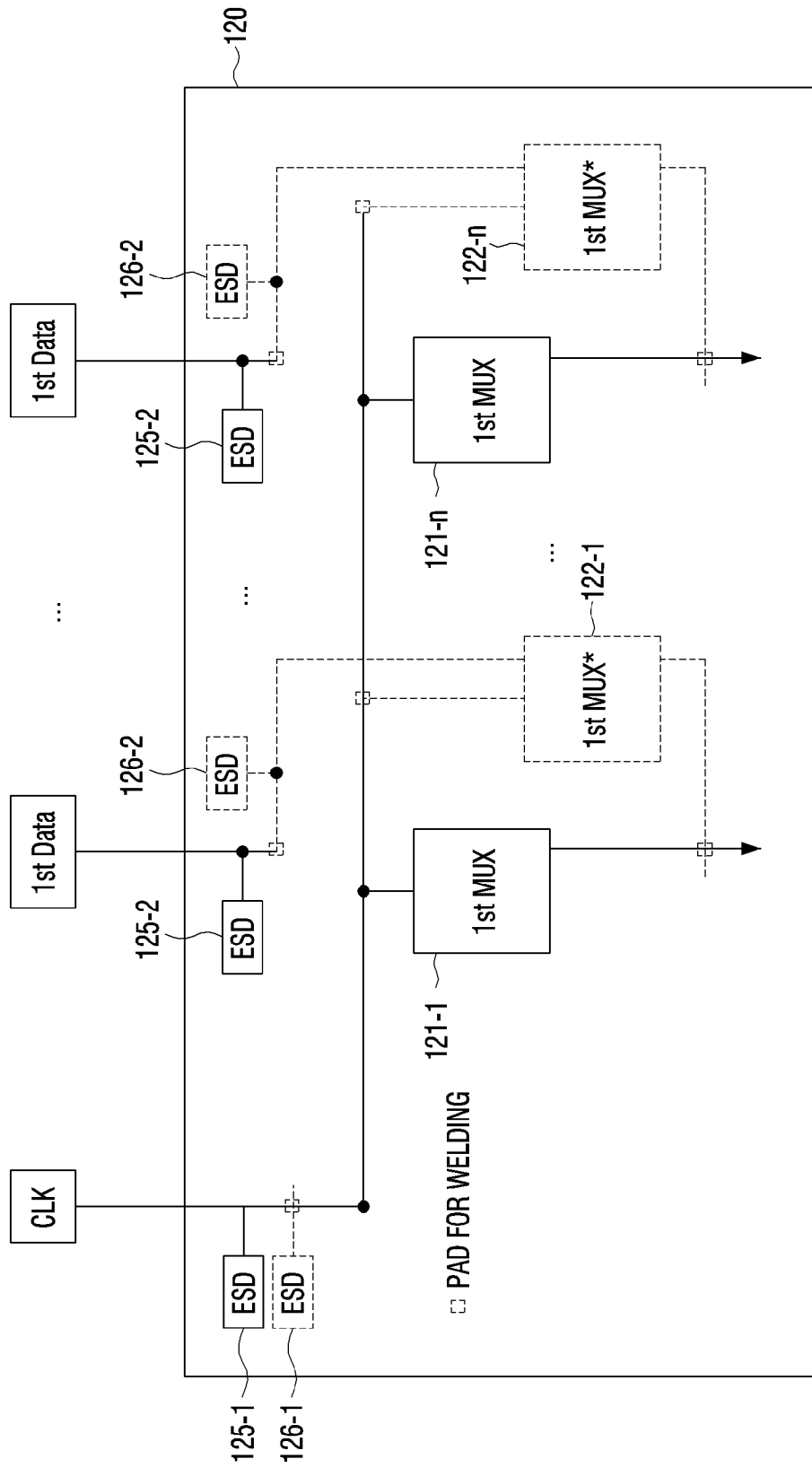
[Fig. 4]



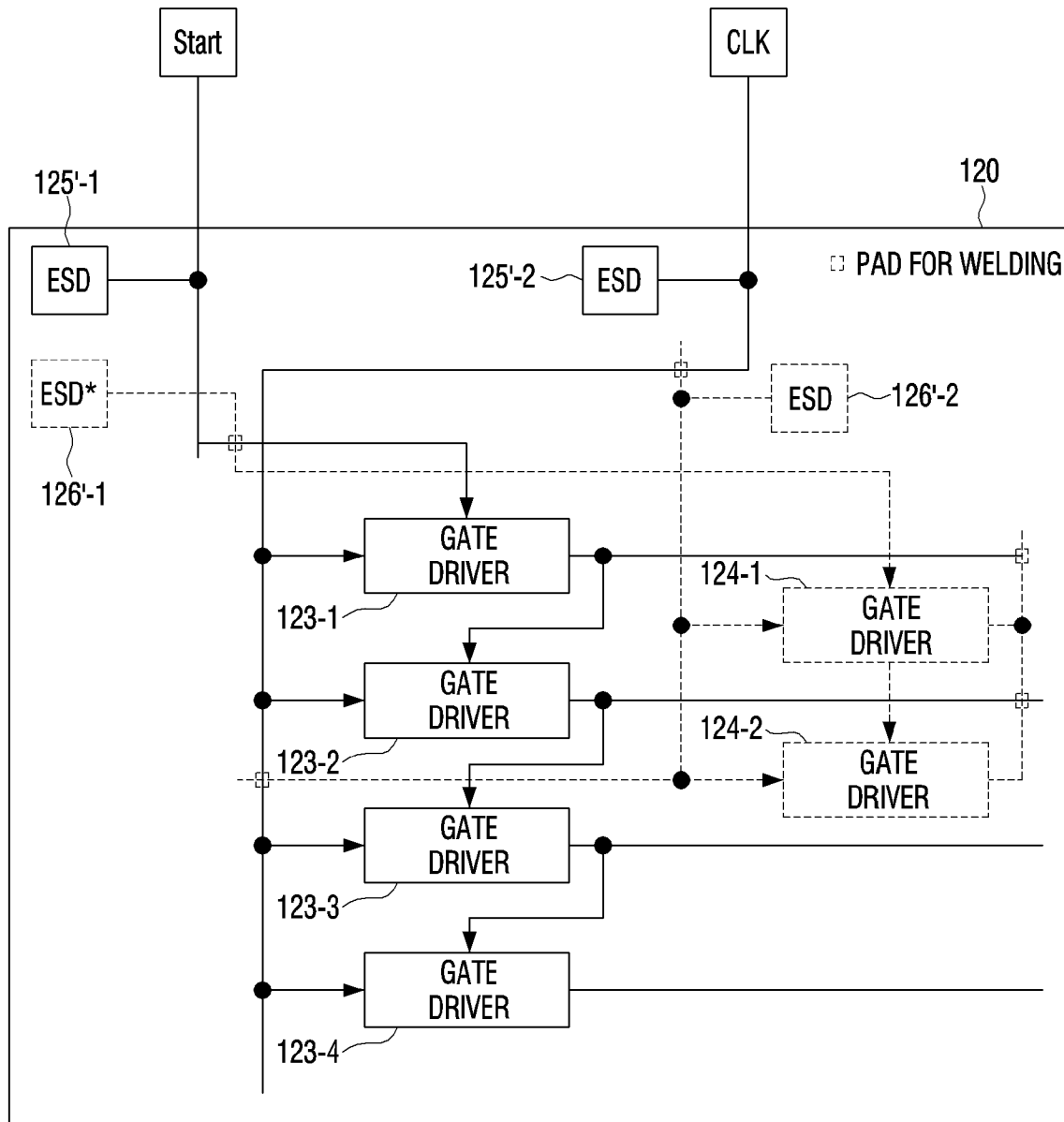
[Fig. 5]



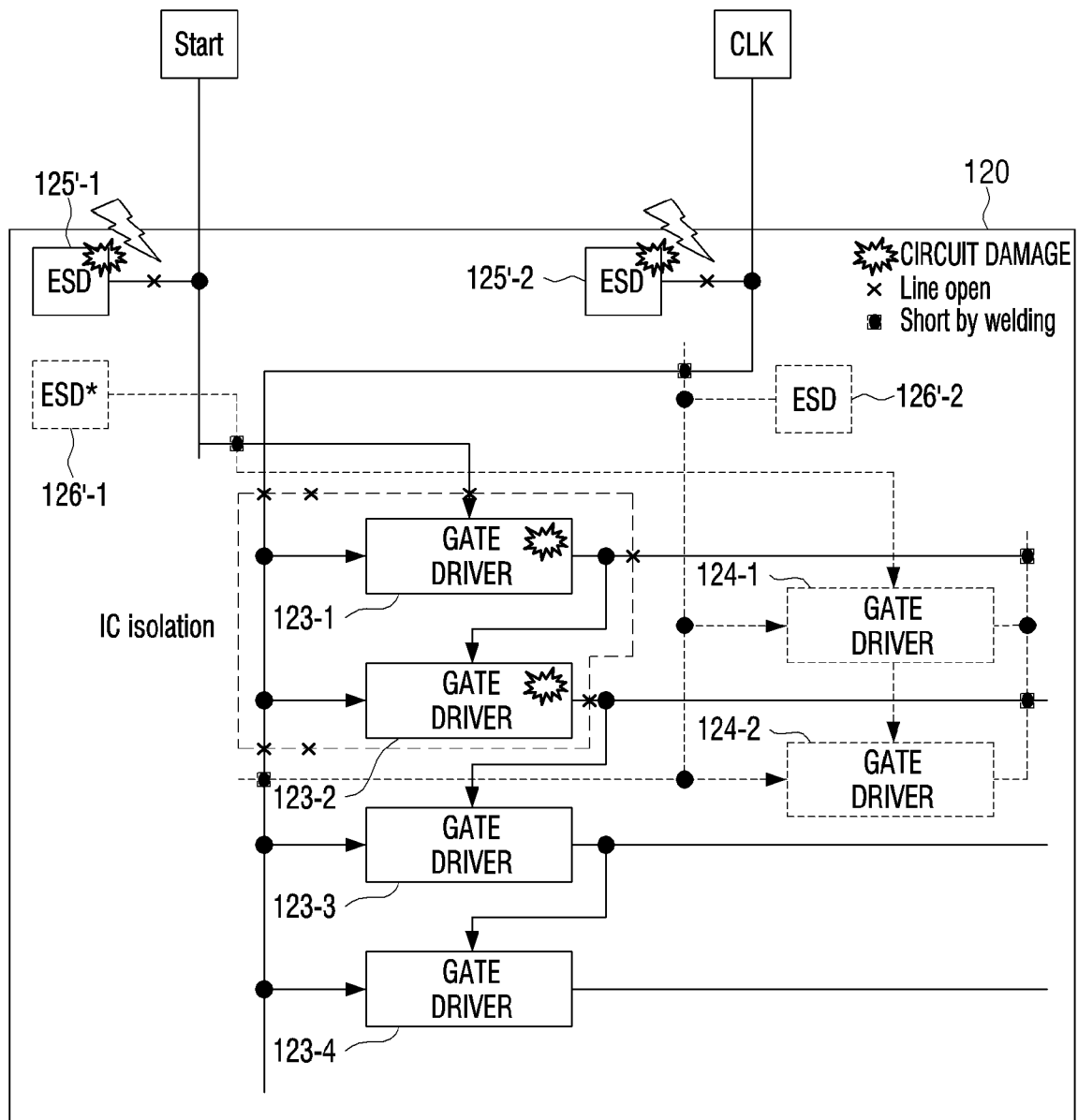
[Fig. 6]



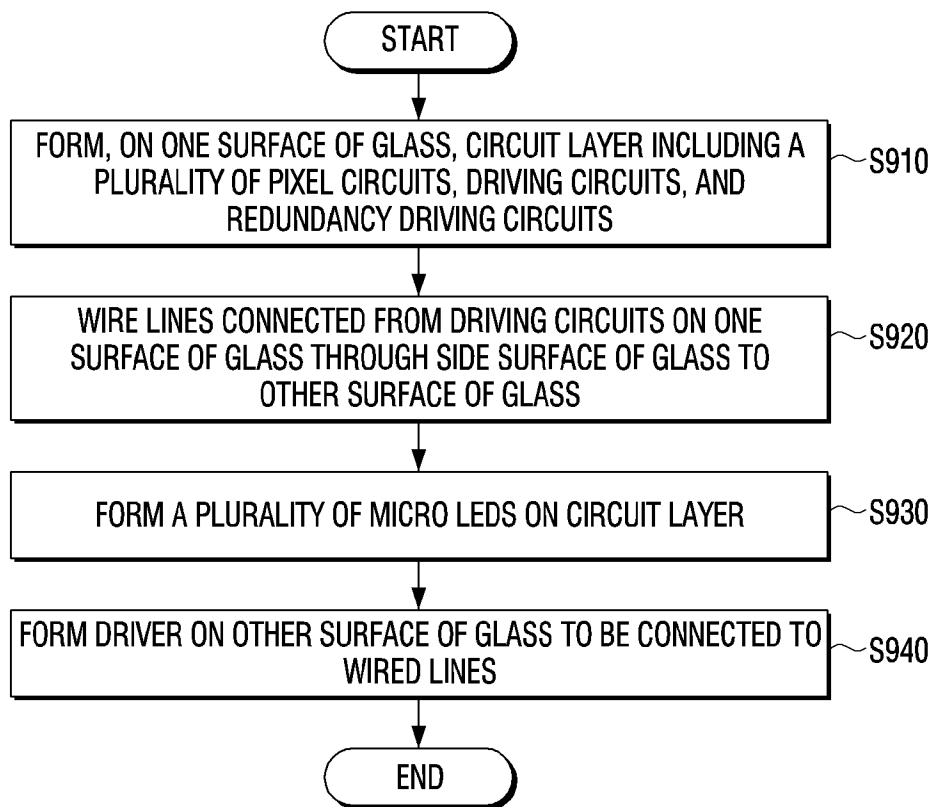
[Fig. 7a]



[Fig. 7b]



[Fig. 9]



A. CLASSIFICATION OF SUBJECT MATTER**G09G 3/32(2006.01)i, G09G 3/00(2006.01)i, H01L 27/15(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G09G 3/32; G09F 9/30; G09G 3/20; G09G 3/30; G09G 3/36; H01L 27/12; H01L 27/32; H01L 51/50; G09G 3/00; H01L 27/15

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & keywords: display panel, LED, pixel circuit, driving circuit, redundancy driving circuit

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2019-0005870 A1 (LG DISPLAY CO., LTD.) 03 January 2019 paragraphs [0020]-[0021], [0025], [0041]-[0042], [0050]; and figures 1-2	1-14
Y	US 2008-0036717 A1 (SEUNG-HWAN MOON) 14 February 2008 paragraphs [0131]-[0137]; and figure 20	1-14
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A	KR 10-2015-0063748 A (LG DISPLAY CO., LTD.) 10 June 2015 claims 1-4; and figures 2-4	1-14



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"D" document cited by the applicant in the international application

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

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Date of mailing of the international search report

13 July 2020 (13.07.2020)

Name and mailing address of the ISA/KR

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

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