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(71) Applicant: **Samsung Display Co., Ltd.**
Gyeonggi-Do (KR)

(72) Inventor: **KWAK, Won Kyu**
Seongnam-si (KR)

(74) Representative: **Shearman, James Ward**
Marks & Clerk LLP
15 Fetter Lane
London EC4A 1BW (GB)

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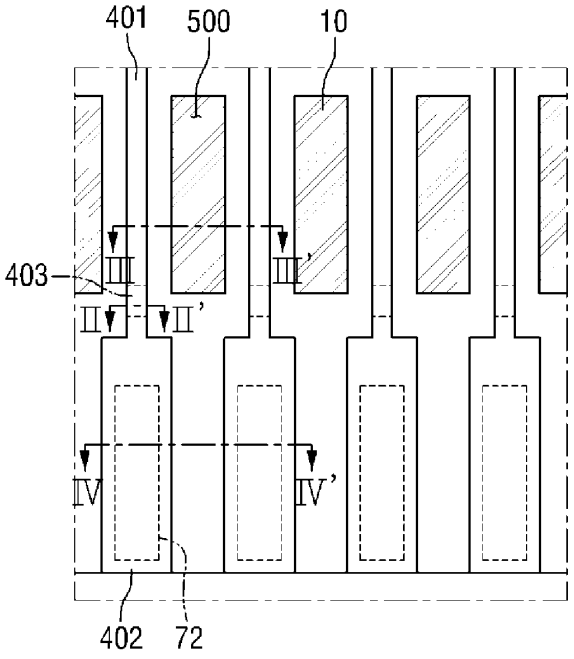
(54) ARRAY SUBSTRATE AND ORGANIC LIGHT-EMITTING DISPLAY INCLUDING THE SAME

(57) An array substrate includes a substrate, a barrier layer disposed on the substrate, a buffer layer disposed on the barrier layer, a first insulating layer disposed on the buffer layer, a second insulating layer disposed on the first insulating layer, a plurality of wiring patterns disposed between the first insulating layer and the second insulating layer and/or on the second insulating layer. In addition, the wiring patterns are separated from each other, and extend toward a side of the substrate. The array substrate further includes a recess pattern disposed adjacent the wiring patterns and recessed from a top surface of the second insulating layer to expose at least part of a top surface of the substrate , and an organic insulating layer disposed on the second insulating layer and exposing at least part of a portion of the top surface of the substrate which is exposed by the recess pattern.

【 Fig. 4】



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Description

BACKGROUND OF THE INVENTION

1. Technical Field

[0001] The present invention relates to an array substrate and a display device including the same, and more particularly, to an array substrate having a display area and a non-display area and a display device including the array substrate.

2. Discussion of the Related Art

[0002] A display device such as a liquid crystal display (LCD) or an organic light-emitting display (OLED) may include an array substrate having a display area and a non-display area located outside the display area. Such a display device may include a plurality of pixels in the display area as basic elements for displaying an image, and each of the pixels may include a switching device to operate independently.

[0003] In LCDs or OLEDs, the array substrate is used as a circuit board for driving each pixel independently. Gate wirings delivering scan signals, data wirings delivering image signals, thin-film transistors (TFTs), and various organic or inorganic insulating layers are disposed on the array substrate. Of these elements, each of the TFTs includes a gate electrode which is a portion of a gate wiring, a semiconductor layer which forms a channel, a source electrode which is a portion of a data wiring, and a drain electrode. Therefore, each of the TFTs may serve as a switching device.

[0004] In the non-display area located outside the display area, a plurality of wirings connected to gate lines or data lines of the display area are disposed. The wirings may extend in various forms and may have respective ends connected to a plurality of pads included in a pad unit in a lower part of the array substrate.

[0005] The array substrate may be exposed to various impacts from its manufacturing process. For example, when the array substrate is transported or when various tests are performed on the array substrate, impacts may be applied to the array substrate. These impacts may create cracks in the substrate. The cracks tend to grow or propagate through inorganic insulating layers disposed on the substrate. That is, when cracks are created in a part of the non-display area, they may propagate to the display area along the inorganic insulating layers, thereby degrading the reliability of the display area. To solve these difficulties, various technical attempts are being made to provide an array substrate structured in such a way to be resistant to impact and suppress the propagation of cracks created in the non-display area.

SUMMARY OF THE INVENTION

[0006] The present invention sets out to provide an array substrate structured to prevent the creation of cracks.

[0007] The present invention also sets out to provide an array substrate structured to suppress the propagation of cracks.

[0008] The present invention also sets out to provide an organic light-emitting display (OLED) structured to prevent the creation of cracks.

[0009] The present invention also sets out to provide an OLED structured to suppress the propagation of cracks.

[0010] However, embodiments of the present invention are not restricted to the effects set forth herein, as would be apparent one of ordinary skill in the art referencing the present disclosure set forth herein.

[0011] According to an embodiment of the present invention, an array substrate is provided. The array substrate includes a substrate, a barrier layer disposed on the substrate, a buffer layer disposed on the barrier layer, a first insulating layer disposed on the buffer layer, a second insulating layer disposed on the first insulating layer, a plurality of wiring patterns disposed between the first insulating layer and the second insulating layer and/or on the second insulating layer. In addition, the wiring patterns are separated from each other, and extend toward a side of the substrate.

[0012] The array substrate further includes a recess pattern disposed adjacent to the wiring patterns and recessed from a top surface of the second insulating layer to expose at least part of the top surface of the substrate, and an organic insulating layer disposed on the second insulating layer and exposing at least part of a portion of the top surface of the substrate which is exposed by the recess pattern.

[0013] According to embodiments of the present invention, there may be provided an array substrate which includes a display area and a non-display area located outside the display area.

[0014] According to an embodiment of the present invention, the non-display area of the array substrate may include a substrate, a barrier layer disposed on the substrate, a buffer layer disposed on the barrier layer, a first insulating layer disposed on the buffer layer, a second insulating layer which is disposed on the first insulating layer, a plurality of wiring patterns disposed between the first insulating layer and the second insulating layer and/or on the second insulating layer. In addition, the wiring patterns may be separated from each other, and extend toward a side of the substrate. The non-display area of the array substrate may further include a recess pattern recessed from a top surface of the second insulating layer to expose at least part of a top surface of the substrate, and an organic insulating layer disposed on the second insulating layer and exposing at least part of a portion of the top surface of the substrate which is exposed by the recess pattern.

[0015] According to an embodiment of the present invention, an OLED may be provided which includes an array substrate and an encapsulation member disposed

on the array substrate. The array substrate may have a display area and a non-display area located outside the display area. The non-display area may include a substrate, a barrier layer which is disposed on the substrate, a buffer layer which is disposed on the barrier layer, a first insulating layer which is disposed on the buffer layer, a second insulating layer which is disposed on the first insulating layer, and a plurality of wiring patterns which are disposed between the first insulating layer and the second insulating layer and/or on the second insulating layer. In addition, the wiring patterns may be separated from each other and extend toward a side of the substrate. The non-display area may further include a recess pattern disposed adjacent to the wiring patterns and which is recessed from a top surface of the second insulating layer to expose at least part of a top surface of the substrate, and an organic insulating layer which is disposed on the second insulating layer and exposes at least part of a portion of the top surface of the substrate which is exposed by the recess pattern.

[0016] According to an embodiment of the present invention, an organic light-emitting display (OLED) may be provided. The OLED may include an array substrate including a display area, and a non-display area disposed outside the display area, and an encapsulation member disposed on the array substrate.

[0017] The display area of the OLED may include a display area substrate, a display area barrier layer disposed on the display area substrate, a display area buffer layer disposed on the display area barrier layer, a semiconductor layer disposed on the display area buffer layer, a gate insulating layer disposed on the semiconductor layer, a gate wiring including a gate line, a gate electrode and a gate pad disposed on the gate insulating layer, an interlayer insulating film covering the gate wiring, a data wiring including a source electrode, a drain electrode, and a data line disposed on the interlayer insulating film, a planarization layer disposed on the data wiring and the interlayer insulating film, a first electrode disposed on the planarization layer and electrically connected to the drain electrode, a pixel defining layer disposed on the first electrode and exposing a portion of the first electrode, an organic layer disposed on the portion of the first electrode exposed by the pixel defining layer, and
a second electrode disposed on the organic layer and the pixel defining layer.

[0018] The non-display area of the OLED may include a non-display area substrate, a non-display area barrier layer disposed on the non-display area substrate, a non-display area buffer layer disposed on the non-display area barrier layer, a first insulating layer disposed on the non-display area buffer layer, a second insulating layer disposed on the first insulating layer, a plurality of wiring patterns disposed between the first insulating layer and the second insulating layer and/or on the second insulating layer. In addition, the wiring patterns may be separated from each other, and extend toward a side of the non-display area substrate.

[0019] In addition, the non-display area of the OLED may further include a recess pattern disposed adjacent to the wiring patterns and recessed from a top surface of the second insulating layer to expose at least part of the top surface of the non-display area substrate, and an organic insulating layer disposed on the second insulating layer and exposing at least part of a portion of the top surface of the non-display area substrate which is exposed by the recess pattern.

[0020] At least some of the above and other features of the invention are set out in the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0021] Embodiments of the present invention can be understood in more detail from the following description taken in conjunction the attached drawings, in which:

FIG. 1 is a plan view of an array substrate according to an embodiment of the present invention;
FIG. 2 is a partial enlarged view of a portion 'A' of FIG. 1;
FIG. 3 is a cross-sectional view taken along the line I-I' of FIG. 2;
FIG. 4 is a partial enlarged view of a portion 'B' of FIG. 1;
FIG. 5 is a cross-sectional view taken along the line II-II' of FIG. 4;
FIG. 6 is a cross-sectional view taken along the line III-III' of FIG. 4;
FIG. 7 is a cross-sectional view taken along the line IV-IV' of FIG. 4;
FIG. 8 is a partial enlarged view of an array substrate according to a modified example of the embodiment of FIG. 4;
FIG. 9 is a partial enlarged view of an array substrate according to a modified example of the modified example of FIG. 8;
FIG. 10 is a partial enlarged view of an array substrate according to a modified example of the embodiment of FIG. 4;
FIG. 11 is a cross-sectional view taken along the line V-V' of FIG. 10;
FIG. 12 is a cross-sectional view taken along the line VI-VI' of FIG. 10;
FIG. 13 is a cross-sectional view of an array substrate according to a modified example of the modified example of FIG. 11;
FIG. 14 is a cross-sectional view of an array substrate according to a modified example of the modified example of FIG. 12;
FIG. 15 is a partial enlarged view of an array substrate according to a modified example of the modified example of FIG. 10;
FIG. 16 is a cross-sectional taken along the line VII-VII' of FIG. 15;
FIG. 17 is a cross-sectional view of an array substrate according to a modified example of the em-

bodiment of FIG. 6;
FIG. 18 is a cross-sectional view of an array substrate according to a modified example of the embodiment of FIG. 7;
FIG. 19 is a partial enlarged view of an array substrate according to an embodiment of the present invention;
FIG. 20 is a cross-sectional view taken along the line VIII-VIII' of FIG. 19;
FIG. 21 is a partial enlarged view of an array substrate according to an embodiment of the present invention;
FIG. 22 is a plan view of an array substrate according to an embodiment of the present invention;
FIG. 23 is a partial enlarged view of a portion 'C' of FIG. 22;
FIG. 24 is a cross-sectional view taken along the line IX-IX' of FIG. 23;
FIG. 25 is a partial enlarged view of a portion 'D' of FIG. 22;
FIG. 26 is a cross-sectional view taken along the line X-X' of FIG. 25;
FIG. 27 is a cross-sectional view of an organic light-emitting display (OLED) according to an embodiment of the present invention; and
FIG. 28 is a cross-sectional view of an OLED according to an embodiment of the present invention.

DETAILED DESCRIPTION

[0022] Embodiments of the present invention and methods for achieving the aspects and features will be apparent after referring to the embodiments described below with reference to the accompanying drawings. However, embodiments of the present invention are not limited to the embodiments disclosed hereinafter, but can be implemented in diverse forms.

[0023] In the entire description of the present invention, the same drawing reference numerals are used for the same elements across various figures.

[0024] In the drawings, the thickness of layers, films, panels, regions, etc., may be exaggerated for clarity. It will be understood that when an element such as a layer, film, region, or substrate is referred to as being "on" another element, it can be directly on the other element or intervening elements may also be present.

[0025] As used herein, the singular forms, "a", "an", and "the" are intended to include plural forms as well, unless the context clearly indicates otherwise.

[0026] Hereinafter, embodiments of the present invention will be described with reference to the attached drawings.

[0027] FIG. 1 is a plan view of an array substrate 100 according to an embodiment of the present invention. FIG. 2 is a partial enlarged view of a portion 'A' of FIG. 1. FIG. 3 is a cross-sectional view taken along the line I-I' of FIG. 2.

[0028] Referring to FIGS. 1 through 3, the array substrate 100 according to the current embodiment includes a display area DA and a non-display area NDA located outside the display area DA.

[0029] The display area DA includes, for example, a plurality of gate lines 50 which extend in a direction and a plurality of data lines 60 which extend in a direction intersecting the gate lines 50. In addition, a plurality of pixel areas surrounded by the gate lines 50 and the data lines 60 are defined. A thin-film transistor (TFT) connected to a gate line 50 and a data line 60 is formed in each of the pixel areas defined by the gate lines 50 and the data lines 60.

[0030] The display area DA will now be described in greater detail with reference to FIGS. 2 and 3.

[0031] A substrate 10 is, for example, a plate-shaped member and may support other elements which will be described later. The substrate 10 may be, for example, an insulating substrate and may be formed of a polymer material including glass, quartz or plastic. In an exemplary embodiment, the substrate 10 may be formed of polyimide (PI). However, the material of the substrate 10 is not limited to polyimide. For example, in an exemplary embodiment, the substrate 10 may include polyethersulfone (PES), polyethylenenaphthalate (PEN), polyethylene (PE), polyvinyl chloride (PVC), polyethylene terephthalate (PET), or combinations thereof.

[0032] The substrate 10 may be a rigid substrate. However, the substrate 10 is not limited to the rigid substrate and may also be a ductile or flexible substrate. That is, in the present specification, the term "substrate" can be understood as a concept that encompasses, for example, a bendable, foldable, and rollable flexible substrate.

[0033] As shown in FIG. 3, the substrate 10 may have a single layer structure. However, the structure of the substrate 10 is not limited to the single layer structure. That is, alternatively, the substrate 10 may have a stacked structure of two or more layers. In other words, the substrate 10 may include, for example, a base layer and a protective layer disposed on the base layer.

[0034] The base layer may be formed of, for example, an insulating material. In an embodiment, the base layer may be formed of, for example, polyimide. However, the material of the base layer is not limited to polyimide. The protective layer may be disposed on the base layer. The protective layer may be formed of, for example, an organic material or an inorganic material. For example, the protective layer may include one or more materials selected from polyethylene terephthalate (PET) and polyethylene naphthalate (PEN). However, the material of the protective layer is not limited to the above examples.

[0035] A barrier layer 11 is disposed on the substrate 10. The barrier layer 11 may prevent penetration of impurity elements from the substrate 10. In an embodiment, the barrier layer 11 may be formed of, for example, one or more materials selected from the group consisting of silicon oxide (SiOx) and silicon nitride (SiNx). However, the material of the barrier layer 11 is not limited to the above examples. The barrier layer 11 may have a single

layer structure or a stacked structure of two or more layers. In an embodiment in which the barrier layer 11 consists of two layers, the two layers may be formed of, for example, different materials. For example, a first layer may be formed of silicon oxide, and a second layer may be formed of silicon nitride. However, the structure of the barrier layer 11 is not limited to the above example.

[0036] Alternatively, in an embodiment, the barrier layer 11 can be omitted depending on the material of the substrate 10 or process conditions.

[0037] A buffer layer 12 is formed on the barrier layer 11 to cover the barrier layer 11. The buffer layer 12 may be, for example, an inorganic layer formed of an inorganic material. In an embodiment, the buffer layer 12 may be formed of, for example, one or more materials selected from the group consisting of silicon oxide (SiOx), silicon nitride (SiNx), aluminum oxide (AlOx), and silicon oxynitride (SiON). However, the material of the buffer layer 12 is not limited to the above examples. In addition, the buffer layer 12 may have a single layer structure or a stacked structure of two or more layers. In an embodiment in which the buffer layer 12 consists of two layers, the two layers may be formed of, for example, different materials. For example, a first layer may be formed of silicon oxide, and a second layer may be formed of silicon nitride. However, the structure of the buffer layer 12 is not limited to the above example.

[0038] A semiconductor layer 40 is formed on the buffer layer 12. The semiconductor layer 40 may be formed of, for example, amorphous silicon or polycrystalline silicon. In an embodiment, the semiconductor layer 40 may be formed by, for example, coating, patterning, and then crystallizing amorphous silicon. However, a method of forming the semiconductor layer 40 is not limited to the above example. In the present specification, the term "semiconductor layer" can be understood as an oxide semiconductor layer.

[0039] A gate insulating layer 20 is formed on the semiconductor layer 40. The gate insulating layer 20 may include, for example, at least one of silicon nitride, silicon oxide, silicon oxynitride (SiOxNy), aluminum oxide (AlOx), yttrium oxide (Y_2O_3), hafnium oxide (HfOx), zirconium oxide (ZrOx), aluminum nitride (A1N), aluminum oxynitride (AlNO), titanium oxide (TiOx), barium titanate (BaTiO3) and lead titanate ($PbTiO_3$), but the material of the gate insulating layer 20 is not limited to the above examples. The gate insulating layer 20 may have a single layer structure. However, the structure of the gate insulating layer 20 is not limited to the single layer structure. The gate insulating layer 20 may also have a multilayer structure which includes two or more insulating layers with different physical properties.

[0040] A gate wiring including a gate line 50, a gate electrode 51 and a gate pad 55 is disposed on the gate insulating layer 20. The gate wiring may be formed of, for example, one or more materials selected from the group consisting of aluminum (Al)-based metal such as aluminum or an aluminum alloy, silver (Ag)-based metal such as silver or a silver alloy, copper (Cu)-based metal such as copper or a copper alloy, molybdenum (Mo)-based metal such as molybdenum or a molybdenum alloy, chromium (Cr), titanium (Ti), and tantalum (Ta). In addition, in an embodiment, the gate wiring may be formed of, for example, at least one material selected from the group consisting of, for example, nickel (Ni), gold (Au), palladium (Pd), platinum (Pt), neodymium (Nd), zinc (Zn), cobalt (Co), silver (Ag), manganese (Mn) or any alloys thereof. However, the material of the gate wiring is not limited to the above examples, and any transparent or semitransparent material having conductivity can be used to form the gate wiring.

[0041] The gate line 50 may be provided in a plurality as described above, and the gate lines 50 may extend, for example, in a direction to be parallel to each other.

[0042] An interlayer insulating film 30 is disposed on the gate wiring to cover the gate wiring. The interlayer insulating film 30 may be, for example, an inorganic layer formed of an inorganic material. In an embodiment, the interlayer insulating film 30 may include, for example, silicon nitride or silicon oxide, but the material of the interlayer insulating film 30 is not limited to the above examples. The interlayer insulating film 30 may have a single layer structure. However, the structure of the interlayer insulating film 30 is not limited to the single layer structure. The interlayer insulating film 30 may also have a multilayer structure which includes two or more insulating layers with, for example, different physical properties. The interlayer insulating film 30 having the multilayer structure will be described later.

[0043] A data wiring including, for example, a source electrode 61, a drain electrode 62 and a data line 60 is disposed on the interlayer insulating film 30. The data wiring may be formed of, for example, molybdenum, chromium, a refractory metal such as tantalum and titanium, or an alloy of these materials. In addition, in an embodiment, the data wiring may be formed of, for example, at least one material selected from the group consisting of, for example, nickel (Ni), gold (Au), palladium (Pd), platinum (Pt), neodymium (Nd), zinc (Zn), cobalt (Co), silver (Ag), manganese (Mn) or any alloys thereof. However, the material of the data wiring is not limited to the above examples, and any transparent or semitransparent material having conductivity can be used to form the data wiring.

[0044] The data line 60 may deliver a data signal and may be placed to intersect the gate line 50. That is, for example, in an embodiment, the gate line 50 may extend in a horizontal direction, and the data line 60 may extend in a vertical direction to intersect the gate line 50.

[0045] In FIG. 2, the data line 60 and the gate line 50 are shaped, for example, like straight lines. In an alternative embodiment, however, the data line 60 and the gate line 60 may also be bent.

[0046] The source electrode 61 is, in this example, a portion of the data line 60 and lies in the same plane with the data line 60. The drain electrode 62 may extend, for

example, parallel to the source electrode 61. In this case, the drain electrode 62 is, parallel to the portion of the data line 60.

[0047] The gate electrode 51, the source electrode 61 and the drain electrode 62 form one TFT, together with the semiconductor layer 40. A channel of the TFT is formed in the semiconductor layer 40 between the source electrode 61 and the drain electrode 62.

[0048] A planarization layer 70 is disposed on the data wiring to cover the data wiring and the interlayer insulating film 30. The planarization layer 70 is relatively thicker than the interlayer insulating film 30. Due to this difference in the thicknesses of the planarization layer 70 and the interlayer insulating film 30, a top surface of the planarization layer 70 may be relatively flatter than a bottom surface thereof which contacts the interlayer insulating film 30 and the source and drain electrodes 61 and 62. To reduce a step difference on the substrate 10, the planarization layer 70 may include, for example, one or more materials selected from the group consisting of acrylic, benzocyclicbutene (BCB), and polyimide. However, the material of the planarization layer 70 is not limited to the above examples. In addition, the planarization layer 70 may be formed of, for example, a photosensitive material.

[0049] A first contact hole 71 is formed in the planarization layer 70 to expose at least part of the drain electrode 62. In this example, the first contact hole 71 penetrates through the planarization layer 70 and partially exposes a top surface of the drain electrode 62.

[0050] A first electrode 80 is disposed on the planarization layer 70 and an exposed portion of the drain electrode 62. That is, the first electrode 80 may cover the planarization layer 70, sidewalls of the first contact hole 71, and the top surface of the drain electrode 62. Accordingly, the first electrode 80 and the drain electrode 62 may be electrically connected to each other. In this particular embodiment, the first electrode 80 is an anode. In other embodiments, it may be a cathode. The first electrode 80 may be formed of, for example, indium tin oxide (ITO), indium zinc oxide (IZO), cadmium tin oxide (CTO), aluminum zinc oxide (AZO), indium tin zinc oxide (ITZO), cadmium oxide (CdO), hafnium oxide (HfO), indium gallium zinc oxide (InGaZnO), indium gallium zinc magnesium oxide (InGaZnMgO), indium gallium magnesium oxide (InGaMgO) or indium gallium aluminum oxide (InGaAlO). However, the material of the first electrode 80 is not limited to the above examples. A pixel defining layer, an organic layer, and a second electrode are disposed on the first electrode 80. These elements will be described in greater detail later.

[0051] The non-display area NDA of the array substrate 100 according to the current embodiment will now be described.

[0052] Referring back to FIG. 1, a scan driver 200, an emission driver 300, and a plurality of wiring patterns which are connected to the scan driver 200, the emission driver 300 or the display area DA are disposed in the non-display area NDA located outside the display area DA. Each of the wiring patterns includes a wiring line 401 and a wiring pad 402.The wiring line 401 extends from the scan driver 200, the emission driver 300 or the display area DA, and the wiring pad 402 is disposed at an end of the wiring line 401 and has an end wider than the wiring line 401. The structure of each of the wiring patterns will be described in greater detail later.

[0053] The non-display area NDA will be described in greater detail with reference to FIGS. 4 through 7.

[0054] FIG. 4 is a partial enlarged view of a portion 'B' of FIG. 1. FIG. 5 is a cross-sectional view taken along the line II-II' of FIG. 4. FIG. 6 is a cross-sectional view taken along the line III-III' of FIG. 4. FIG. 7 is a cross-sectional view taken along the line IV-IV' of FIG. 4.

[0055] Referring to FIGS. 4 through 7, the non-display area NDA of the array substrate 100 according to the current embodiment includes, for example, a substrate 10, a barrier layer 11 which is disposed on the substrate 10, a buffer layer 12 which is disposed on the barrier layer 11, a first insulating layer 25 which is disposed on the buffer layer 12, a second insulating layer 35 which is disposed on the first insulating layer 25, and a plurality of wiring patterns. The wiring patterns are disposed between the first insulating layer 25 and the second insulating layer 35 and on the second insulating layer 35. In addition, the wiring patterns are separated from each other, and extend toward a side of the substrate 10. The non-display area NDA further includes, for example, a recess pattern 500 which is recessed from a top surface of the second insulating layer 35 by a predetermined depth to expose at least part of a top surface of the substrate 10, and an organic insulating layer 75 which is disposed on the second insulating layer 35 and exposes at least part of a portion of the top surface of the substrate 10 which is exposed by the recess pattern 500.

[0056] The substrate 10, the barrier layer 11, and the buffer layer 12 may be substantially identical to those described above with reference to FIGS. 1 through 3, and thus a detailed description thereof will be omitted.

[0057] The first insulating layer 25 is disposed on the buffer layer 12. The first insulating layer 25 may be, for example, an inorganic insulating layer formed of an inorganic material. The first insulating layer 25 may be formed of, e.g., silicon nitride or silicon oxide. However, the material of the first insulating layer 25 is not limited to the above examples.

[0058] In this embodiment, the first insulating layer 25 may be formed of, for example, substantially the same material as the gate insulating layer 20 of the display area DA. In other words, the first insulating layer 25 of the non-display area NDA may be formed at substantially the same time as the gate insulating layer 20 of the display area DA. However, this is merely an example, and embodiments of the present invention are not limited to this example. That is, the first insulating layer 25 of the non-display area NDA and the gate insulating layer 20 of the display area DA may also be formed independently as

separate elements.

[0059] The second insulating layer 35 is disposed on the first insulating layer 25. Like the first insulating layer 25, the second insulating layer 35 may be, for example, an inorganic insulating layer formed of an inorganic material. Like the first insulating layer 25, the second insulating layer 35 may include, for example, silicon nitride or silicon oxide. The first insulating layer 25 and the second insulating layer 35 may be formed of, for example, different materials. However, embodiments of the present invention are not limited thereto, and the first insulting layer 25 and the second insulating layer 35 may also be formed of the same material. In an embodiment of the invention, the second insulating layer 35 may be formed of, for example, substantially the same material as the interlayer insulating film 30 of the display area DA. That is, the second insulating layer 35 may be formed at substantially the same time as the interlayer insulating film 30 of the display area DA. However, this is merely an example, and embodiments of the present invention are not limited to this example. That is, the interlayer insulating film 30 of the display area DA and the second insulating layer 35 of the non-display area NDA may also be formed independently as separate elements.

[0060] The wiring patterns may be disposed on the first insulating layer 25 to be interposed between the first insulating layer 25 and the second insulating layer 35 and/or may be disposed on the second insulating layer 35. For example, a portion of each of the wiring patterns may be formed on the first insulating layer 25, and the remaining portion of each of the wiring patterns may be formed on the second insulating layer 35.

[0061] The wiring patterns are connected to the display area DA, the scan driver 200 or the emission driver 300 so as to transmit or receive signals. To this end, the wiring patterns may be formed of, for example, one or more materials selected from the group consisting of aluminum (Al)-based metal such as aluminum or an aluminum alloy, silver (Ag)-based metal such as silver or a silver alloy, copper (Cu)-based metal such as copper or a copper alloy, molybdenum (Mo)-based metal such as molybdenum or a molybdenum alloy, chrome (Cr), titanium (Ti), and tantalum (Ta). In addition, in an embodiment, the wiring patterns may be formed of, for example, at least one material selected from the group consisting of, for example, nickel (Ni), gold (Au), palladium (Pd), platinum (Pt), neodymium (Nd), zinc (Zn), cobalt (Co), silver (Ag), manganese (Mn) or any alloys thereof. However, the material of the wiring patterns is not limited to the above examples, and a conductor having conductivity can be used to form the wiring patterns.

[0062] In an embodiment of the invention, each of the wiring patterns may include, for example, a wiring line 401, a wiring pad 402, and a wiring connection portion 403.

[0063] The wiring line 401 is electrically connected to the display area DA, the scan driver 200 or the emission driver 300 and extends from the display area DA, the scan driver 200 or the emission driver 300 toward a side of the substrate 10. The wiring line 401 is provided in a plurality, and the wiring lines 401 are separated from each other by a predetermined distance. Each of the wiring lines 401 may extend, for example, in a straight line or may be bent one or more times to extend toward the side of the substrate 10.

[0064] In this embodiment, the wiring lines 401 are disposed on the first insulating layer 25. That is, the wiring lines 401 are interposed between the first insulating layer 25 and the second insulating layer 35. The wiring lines 401 may be formed of, for example, the same material as the gate wiring of the display area DA. In other words, the wiring line 401 may be formed at substantially the same time as the gate wiring of the display area DA. However, embodiments of the present invention are not limited thereto, and the wiring line 401 of the non-display area NDA and the gate wiring of the display area DA may also be formed independently.

[0065] A first end of the wiring line 401 partially overlaps a second end of the wiring pad 402 which will be described later.

[0066] The wiring pad 402 is electrically connected to the first end of the wiring line 401 and extends from the first end of the wiring line 401 toward a side of the substrate 10. The wiring pad 402 is provided in a plurality, and the wiring pads 402 are arranged along the side of the substrate 10. In this embodiment, a first end of the wiring pad 402 contacts the side of the substrate 10, but embodiments of the present invention are not limited thereto. The second end of the wiring pad 402 is relatively wider than the wiring line 401. An external circuit module, such as, for example, a test device for testing the performance of the substrate 10 or a flexible printed circuit board (FPCB) connected to the substrate 10, may be connected to the wiring pad 402. When the wiring pad 402 is wider than the wiring line 401, it can be electrically connected to the circuit module more easily.

[0067] In this embodiment, the wiring pad 402 is disposed on the second insulating layer 35. That is, the wiring pad 402 and the wiring line 401 may be disposed at, for example, different levels. In other words, the wiring pad 402 and the wiring line 401 may be disposed on different layers.

[0068] In an embodiment in which the wiring line 401 is disposed on the first insulating layer 25 and the wiring pad 402 is disposed on the second insulating layer 35, the wiring pad 402 and the wiring line 401 may be electrically connected to each other through the wiring connection portion 403. The wiring connection portion 403 will now be described in greater detail with reference to FIG. 5.

[0069] Referring to FIG. 5, the second insulating layer 35 is disposed on the wiring line 401 to expose at least part of the wiring line 401. The wiring pad 402 is disposed on a portion of the wiring line 401 which is exposed by the second insulating layer 35. Accordingly, the wiring pad 402 and the wiring line 401 are electrically connected

to each other.

[0070] At least one recess pattern 500 is disposed adjacent to the wiring patterns. The recess pattern 500 is recessed from, for example, the top surface of the second insulating layer 35 by a predetermined distance. The recess pattern 500 recessed from the top surface of the second insulating layer 35 by the predetermined distance may expose at least part of the top surface of the substrate 10. In other words, a bottom surface of the recess pattern 500 may include at least part of the top surface of the substrate 10.

[0071] To put it another way, the recess pattern 500 penetrates through the barrier layer 11, the buffer layer 12, the first insulating layer 25, and the second insulating layer 35 to expose at least part of the top surface of the substrate 10. That is, in this embodiment, the bottom surface of the recess pattern 500 consists of the top surface of the substrate 10, and sidewalls of the recess patterns 500 consist of inner side surfaces of the barrier layer 11, the buffer layer 12, the first insulating layer 25 and the second insulating layer 35. However, embodiments of the present invention are not limited thereto. When an intermediate layer is interposed between the second insulating layer 35 and the substrate 10 or when another layer is disposed on the second insulating layer 35, the sidewalls of the recess pattern 500 may further include, for example, inner side surfaces of the intermediate layer and inner side surfaces of the layer disposed on the second insulating layer 35. This will be described in greater detail later.

[0072] In an embodiment of the invention, at least one recess pattern 500 may be disposed adjacent to the wiring lines 401 or disposed between a wiring line 401 and another wiring line 401.

[0073] In FIGS. 4 and 6, the recess pattern 500 is disposed adjacent to the wiring lines 401 but is separated from each of the wiring lines 401 by a predetermined distance. However, embodiments of the present invention are not limited thereto. The recess pattern 500 may also contact at least part of each of the wiring lines 401.

[0074] The recess pattern 500 that penetrates through one or more inorganic insulating layers on the substrate 10 can suppress the propagation of cracks created by impacts applied to the array substrate 100 during processes of manufacturing, testing, and transporting the array substrate 100. That is, cracks created by various impacts tend to grow or propagate through the inorganic insulating layers of the substrate 10. However, if the recess pattern 500 is formed by removing part of the inorganic insulating layers as described above, it can suppress the propagation of the cracks by blocking the propagation path of the cracks. That is, it is possible to hinder cracks created in the non-display area NDA from growing to reach the display area DA. In other words, the recess pattern 500 can serve as a crack stopper.

[0075] The organic insulating layer 75 is disposed on the second insulating layer 35. The organic insulating layer 75 may be formed of an organic material. The organic insulating layer 75 may include, for example, one or more materials selected from the group consisting of acrylic, benzocyclicbutene (BCB), and polyimide. However, the material of the organic insulating layer 75 is not limited to the above examples. In addition, the organic insulating layer 75 may be formed of, for example, a photosensitive material.

[0076] In an area where the wiring lines 401 are formed, the organic insulating layer 75 disposed on the second insulating layer 35 defines at least part of the recess pattern 500 (see FIG. 6). That is, the organic insulating layer 75 exposes at least part of a portion of the top surface of the substrate 10 which is accessed by the recess pattern 500..

[0077] In an area where the wiring pads 402 are disposed, the organic insulating layer 75 partially covers the second insulating layer 35 and the wiring pads 402 disposed on the second insulating layer 35 (see FIG. 7). That is, the organic insulating layer 75 exposes the wiring pads 402. In other words, the organic insulating layer 75 includes, for example, a contact 72 which penetrates through the organic insulating layer 75 to expose at least part of a top surface of each of the wiring pads 402. As described above, various test devices for testing the performance of the substrate 10 or an FPC connected to the substrate 10 may be connected to the wiring pads 402. That is, the contact 72 may expose each of the wiring pads 402, thereby allowing each of the wiring pads 402 to be connected to the above devices.

[0078] The organic insulating layer 75 may be formed of, for example, substantially the same material as the planarization layer 70 of the display area DA. In other words, the organic insulating layer 75 may be formed at the same time as the planarization layer 70 of the display area DA. However, this is merely an example, and embodiments of the present invention are not limited to this example. The planarization layer 70 of the display area DA and the organic insulating layer 75 of the non-display area NDA may also be formed independently as separate elements.

[0079] FIG. 8 is a partial enlarged view of an array substrate according to a modified example of the embodiment of FIG. 4. Referring to FIG. 8, the array substrate according to the current modified example is different from the array substrate 100 according to FIG. 4 in that a plurality of recess patterns 507 are formed between a wiring line 401 and another adjacent wiring line 401.

[0080] In this embodiment recess patterns 507 are disposed between a wiring line 401 and another adjacent wiring line 401. Mor specifically, in FIG. 8, three recess patterns 507 are arranged in a line between a wiring line 401 and another adjacent wiring line 401. However, the number and arrangement of the recess patterns 507 are not limited to the above example. That is one or more patterns 507 may be provided, and if a plurality of the recess patterns 507 are provided, they may be arranged, for example, in a line or in a matrix of columns and rows. This will be described later.

[0081] FIG. 9 is a partial enlarged view of an array substrate according to a modified example of the modified example of FIG. 8. The array substrate according to the current modified example is different from the array substrate according to the modified embodiment of FIG. 8 in that a plurality of recess patterns 508 are arranged in a matrix of columns and rows between a wiring line 401 and another adjacent wiring line 401.

[0082] As described above, a plurality of recess patterns 508 may be disposed between a wiring line 401 and another adjacent wiring line 401. The recess patterns 508 may be arranged, for example, in a line or in a matrix of columns and rows. In FIG. 9, the recess patterns 508 are arranged in a 3 x 2 matrix (having three rows and two columns), but the arrangement of the recess patterns 508 is not limited to this example. That is, the number of rows and the number of columns may be greater than or equal to two. In FIG. 9, the recess patterns 508 are arranged regularly. However, embodiments of the present invention are not limited thereto, and the recess patterns 508 may also be arranged irregularly.

[0083] FIG. 10 is a partial enlarged view of an array substrate according to a modified example of the embodiment of FIG. 4. FIG. 11 is a cross-sectional view taken along the line V-V' of FIG. 10. FIG. 12 is a cross-sectional view taken along the line VI-VI' of FIG. 10.

[0084] Referring to FIGS. 10 through 12, the array substrate according to the current modified example is different from the array substrate 100 according to FIG. 4 in that a recess pattern 501 disposed between wiring lines 401 extends to between wiring pads 402.

[0085] The recess pattern 501 disposed between a wiring line 401 and another wiring line 401 extends to between a wiring pad 402 connected to the former wiring line 401 and another wiring pad 402 connected to the latter wiring line 402. That is, the recess pattern 501 disposed between adjacent wiring lines 401 extends toward a side of a substrate 10. The wiring pads 402 are relatively wider than the wiring lines 401. Accordingly, a width d1 of the recess pattern 501 disposed between the wiring lines 401 is relatively greater than a width d2 of the recess pattern 501 disposed between the wiring pads 402. However, embodiments of the present invention are not limited thereto, and the width d1 of the recess pattern 501 disposed between the wiring lines 401 may be substantially equal to the width d2 of the recess pattern 501 disposed between the wiring pads 402.

[0086] FIG. 13 is a cross-sectional view of an array substrate according to a modified example of the modified example of FIG. 11. FIG. 14 is a cross-sectional view of an array substrate according to a modified example of the modified example of FIG. 12.

[0087] The modified example of FIGS. 13 and 14 is different from the modified example of FIGS. 11 and 12 in that an organic insulating layer 75 disposed on a second insulating layer 35 covers a portion of a substrate 10 which is exposed by a recess pattern 501. As described above, the organic insulating layer 75 is disposed on the second insulating layer 35. In this embodiment, the organic insulating layer 75 completely covers a portion of a top surface of the substrate 10 which is exposed by the recess pattern 501. That is, the organic insulating layer 75 covers the second insulating layer 35, sidewalls of the recess pattern 501, and a bottom surface of the recess pattern 501. In FIGS. 13 and 14, the organic insulating layer 75 completely covers the portion of the top surface of the substrate 10 which is exposed by the recess pattern 501. However, embodiments of the present invention are not limited thereto, and the organic insulating layer 75 may fully or partially expose the portion of the top surface of the substrate 10 which is exposed by the recess pattern 501. A contact 72 which exposes at least part of each wiring pad 402 is formed in the organic insulating layer 75. As the contact 72 is substantially identical to the contact 72 described above with reference to FIG. 7, a detailed description thereof will be omitted.

[0088] FIG. 15 is a partial enlarged view of an array substrate according to a modified example of the modified example of FIG. 10. FIG. 16 is a cross-sectional taken along the line VII-VII' of FIG. 15.

[0089] Referring to FIGS. 15 and 16, the array substrate according to the current modified example is different from the modified example of FIG. 10 in that it further includes recess grooves 502 which are each formed inside a respective wiring pad 402 and penetrates through the wiring pad 402 to expose a top surface of a substrate 10. In this example, each recess groove 502 is disposed inside an outer circumference of a respective wiring pad 402.

[0090] Each recess groove 502 sequentially s through a wiring pad 402, a second insulating layer 35, a first insulating layer 25, a buffer layer 12 and a barrier layer 11 to expose the top surface of the substrate 10. That is a bottom surface of the recess groove 502 includes the top surface of the substrate 10, and sidewalls of the recess groove 502 include inner side surfaces of the wiring pad 402, the second insulating layer 35, the first insulating layer 25, the buffer layer 12 and the barrier layer 11.

[0091] An organic insulating layer 75 is disposed on the second insulating layer 35 and each wiring pad 402. In FIG. 16, the organic insulating layer 75 completely exposes a portion of the top surface of the substrate 10 which is exposed by the second insulating layer 35, each wiring pad 402, and the recess groove 502. However, embodiments of the present invention are not limited thereto, and the organic insulating layer 75 may also cover at least part of the portion of the top surface of the substrate 10 which is exposed by the recess groove 502. If the recess groove 502 penetrating through each wiring pad 402 to expose the top surface of the substrate 10 is formed in each wiring pad 402, cracks created by impacts applied to the wiring pads 402 when a substrate test device or an FPC is connected to or disconnected from the wiring pads 402 can be prevented from propagating to a display area DA through the wiring pads 402 or through inorganic insulating layers disposed under the wiring

pads 402.

[0092] FIG. 17 is a cross-sectional view of an array substrate according to a modified example of the embodiment of FIG. 6. FIG. 18 is a cross-sectional view of an array substrate according to a modified example of the embodiment of FIG. 7.

[0093] The modified example of FIGS. 17 and 18 is different from the array substrate of FIGS. 6 and 7 in that a second insulating layer 35' includes a first sub-insulating layer 31 and a second sub-insulating layer 32.

[0094] As described above, the second insulating layer 35 may have a single layer structure but embodiments of the present invention are not limited thereto. For example, in the present embodiment, the second insulating layer 35' has a multilayer structure including two or more insulating layers. For ease of description, an insulating layer which covers a first insulating layer 25 will be referred to as the first sub-insulating layer 31, and an insulating layer which covers the first sub-insulating layer 31 will be referred to as the second sub-insulating layer 32.

[0095] Each of the first sub-insulating layer 31 and the second sub-insulating layer 32 may be, for example, an inorganic insulating layer formed of an inorganic material. For example, each of the first sub-insulating layer 31 and the second sub-insulating layer 32 may include one or more materials selected from silicon oxide and silicon nitride. However, the material of each of the first sub-insulating layer 31 and the second sub-insulating layer 32 are not limited to the above examples. The first sub-insulating layer 31 and the second sub-insulating layer 32 may be formed of, for example, different materials.

[0096] The second insulating layer 35' may have a multilayer structure due to the structure of a display area DA. For example, although not shown in the drawings, a storage capacitor may be disposed adjacent to a TFT in the display area DA. In an embodiment of the invention, the storage capacitor may include, for example, a first gate metal disposed on a gate insulating layer 20, a first sub-insulating layer 31 disposed on the first gate metal, a second sub-insulating layer 32 disposed on the first sub-insulating layer 31, and a second gate metal disposed on the second sub-insulating layer 32. To correspond to the storage capacitor, source and drain electrodes 61 and 62 of the TFT may be disposed on the second sub-insulating layer 32. However, this is merely an example, and the specific structure of the display area DA is not limited to this example.

[0097] FIG. 19 is a partial enlarged view of an array substrate according to an embodiment of the present invention. FIG. 20 is a cross-sectional view taken along the line VIII-VIII' of FIG. 19.

[0098] Referring to FIGS. 19 and 20, the array substrate according to the current embodiment is different from the array substrate 100 according to FIG. 4 in that each wiring line 411 extends in a zigzag shape toward a side of a substrate 10.

[0099] Each wiring line 411 is bent several times to have, a zigzag shape and extends toward a side of the substrate 10. For ease of description, a direction toward the side of the substrate 10 will be referred to as a first direction, a direction perpendicular to the first direction will be referred to as a second direction, and a direction opposite the second direction will be referred to as a third direction.

[0100] Referring to FIG. 19, each wiring line 411 extending in the first direction also extends a predetermined distance in the second direction, extends a predetermined distance again in the first direction, extends a predetermined distance in the third direction, and then extends again in the first direction. That is, each wiring line 411 extends in the first direction, the second direction, the first direction, the third direction and the first direction, sequentially.

[0101] The distance by which each wiring line 411 extends along the second direction may be, but is not limited to, substantially equal to the distance by which the wiring line 411 extends along the third direction.

[0102] As described above, each wiring line 411 extends in the first direction, the second direction, the first direction, the third direction and the first direction sequentially, and this order may be repeated one or more times.

[0103] When each wiring line 411 extends in the first direction, the second direction, the first direction, the third direction and the first direction sequentially as described above, a space is defined by each portion of the wiring line 411 which extends in the second direction, the first direction and the third direction or in the third direction, the first direction and the second direction. In this embodiment, a recess pattern 503 is disposed in the space defined by each portion of the wiring line 411 which extends in the second direction, the first direction and the third direction or in the third direction, the first direction and the second direction. In other words, each wiring line 411 is disposed adjacent to an outer circumference of a recess pattern 503 and disposed along part of the outer circumference of the recess pattern 503. To put it another way, the recess pattern 503 is disposed between portions of each wiring line 411 which extends in a zigzag shape. At least one recess pattern 503 is disposed between the wiring lines 411.

[0104] From the perspective of the recess pattern 503, a plurality of recess patterns 503 are arranged in a matrix of columns and rows, and each wiring line 411 extends in a zigzag shape between the recess patterns 503 arranged in the matrix of columns and rows. In FIG. 19, a plurality of recess patterns 503 are arranged in a straight line along a row direction and alternately arranged along a column direction. However, the arrangement of the recess patterns 503 is not limited to this example. That is, the recess patterns 503 may also be arranged in a straight line along the row and column directions, may be alternately arranged along the row direction and arranged in a straight line along the column direction, or may be alternately arranged along the column direction and arranged in a straight line along the row direction.

[0105] In addition, each wiring line 411 may be dis-

posed, for example, between the recess patterns 503 arranged in the matrix.

[0106] FIG. 21 is a partial enlarged view of an array substrate according to an embodiment of the present invention. Referring to FIG. 21, the array substrate according to the current embodiment is different from the array substrate 100 according to FIG. 4 in that each wiring line 421 extends in a curved shape having a pitch.

[0107] In the array substrate according to the current embodiment, each wiring line 421 has a winding shape. To put it another way, each wiring line 421 winds in a gentley curved shape.

[0108] When each wiring line 421 extends in a curved shape having a pitch, valleys and ridges are formed on both sides of the wiring line 421. That is, a valley and a ridge are repeated one or more times on each side of each wiring line 421.

[0109] A recess pattern 504 is disposed adjacent to each valley of each wiring line 421. At least one recess pattern 504 is disposed adjacent to each of the valleys formed on each sides of each wiring line 421. In FIG. 21, a recess pattern 504 is adjacent to each valley. However, embodiments of the present invention are not limited thereto, and a recess pattern 504 may partially contact each valley of each wiring line 421.

[0110] For example, from the perspective of the recess pattern 504, a plurality of recess patterns 504 are arranged in a matrix of columns and rows, and each wiring line 421 extends in a curved shape having a pitch between the recess patterns 504 arranged in the matrix of columns and rows.

[0111] In FIG. 21, a plurality of recess patterns 504 are arranged in a straight line along a row direction and alternately arranged along a column direction. However, the arrangement of the recess patterns 504 is not limited to this example. That is, the recess patterns 504 may also be arranged in a straight line along the row and column directions, may be alternately arranged along the row direction and arranged in a straight line along the column direction, or may be alternately arranged along the column direction and arranged in a straight line along the row direction.

[0112] In addition, each wiring line 421 may be disposed, for example, between the recess patterns 504 arranged in the matrix. At least one recess pattern 504 may be disposed, for example, between a wiring line 421 and another wiring line 421.

[0113] FIG. 22 is a plan view of an array substrate according to an embodiment of the present invention. FIG. 23 is a partial enlarged view of a portion 'C' of FIG. 22. FIG. 24 is a cross-sectional view taken along the line IX-IX' of FIG. 23. FIG. 25 is a partial enlarged view of a portion 'D' of FIG. 22. FIG. 26 is a cross-sectional view taken along the line X-X' of FIG. 25.

[0114] Referring to FIGS. 22 through 25, the array substrate according to the current embodiment is different from the array substrate 100 according to FIG. 1 in that a cell ID pattern 45 and/or a cutting line 700 are formed in a non-display area NDA.

[0115] The array substrate 101 according to the current embodiment may include, for example, the cell ID pattern 45 and the cutting line 700.

[0116] The cell ID pattern 45 is disposed, in the non-display area NDA, outside each of outermost wiring lines 401. In this embodiment the cell ID pattern 45 is disposed adjacent to each of the outermost wiring lines 401. A unique number, a figure, an identification code, etc. used to identify the array substrate 101 may be patterned on the cell ID pattern 45. That is, information about the array substrate 101 can be obtained from the unique number, the figure, the identification code, etc. patterned on the cell ID pattern 45.

[0117] The cell ID pattern 45 will now be described in greater detail with reference to FIGS. 23 and 24.

[0118] In FIGS. 23 and 24, the cell ID pattern 45 is shaped like a quadrangle. However, the shape of the cell ID pattern is not limited to the quadrangular shape, and the cell ID pattern 45 may also have a circular shape or a shape that at least partially includes a curve.

[0119] As described above, a unique number, a figure, an identification code, etc. may be patterned on the cell ID pattern 45. In FIG. 23, a cross-shaped figure 46 is patterned on the cell ID pattern 45. However, the shape of the figure formed on the cell ID pattern 45 is not limited to the cross shape.

[0120] In embodiment, the cell ID pattern 45 is disposed on a buffer layer 12. However, this is merely an example, and the position of the cell ID pattern 45 is not limited to this example. The cell ID pattern 45 disposed on the buffer layer 12 may be formed of, for example, substantially the same material as a semiconductor layer 40 of a display area DA. That is, the cell ID pattern 45 of the non-display area NDA may be formed at the same time as the semiconductor layer 40 of the display area DA. However, embodiments of the present invention are not limited thereto, and the cell ID pattern 45 may also be formed independently of the semiconductor layer 40 of the display area DA.

[0121] A recess pattern 505 is disposed along an outer circumference of the cell ID pattern 45. The recess pattern 505 may contact the outer circumference of the cell ID pattern 45 or may be disposed adjacent to the outer circumference of the cell ID pattern 45. In an embodiment such as this, in which the cell ID pattern 45 is shaped like a quadrangle, the recess pattern 505 may be shaped like a quadrangle having a through hole. However, the shape of the cell ID pattern 45 is not limited to the above example, and the recess pattern 505 may have a shape corresponding to the shape of the outer circumference of the cell ID pattern 45. The recess pattern 505 disposed along the outer circumference of the cell ID pattern 45 can prevent cracks created during a process of manufacturing or transporting the array substrate 101 from propagating to the cell ID pattern 45 and thus damaging the cell ID pattern 45.

[0122] The cutting line 700 is formed in the non-display

area NDA of the array substrate according to the current embodiment. A corner of the non-display area NDA of the array substrate 101 may be cut according to the type of product. That is, the corner of the array substrate 101 may be, for example, chamfered. To this end, the cutting line 700 is formed on the array substrate 101. The cutting line 700 may, for example, extend diagonally in both sides of the non-display area NDA of the array substrate. That is, the cutting line 700 may traverse at least part of the array substrate 101.

[0123] The angle formed by the cutting line 700 and a side of the array substrate 101 is not limited to a particular angle. That is, the angle formed by the cutting line 700 and the side of the array substrate 101 may vary according to a product to which the array substrate 101 is applied.

[0124] To prevent the creation of cracks in a cutting process, the cutting line 700 may be, for example, recessed from a top surface of a second insulating layer 35 by a predetermined distance. That is, as shown in the cross-sectional view of FIG. 26, the cutting line 700 may be recessed from the top surface of the second insulating layer 35 to expose a top surface of a substrate 10. In other words, a bottom surface of the cutting line 700 may include, for example, the top surface of the substrate 10, and sidewalls of the cutting line 700 may include inner side surfaces of a barrier layer 11, the buffer layer 12, a first insulating layer 25 and the second insulating layer 35.

[0125] Referring to FIGS. 25 and 26, one or more recess patterns 506 are disposed adjacent to the cutting line 700. In this example, the recess patterns 506 are disposed adjacent to a second side of the cutting line 700. In other words, when the array substrate 101 is cut along the cutting line 700 in a cutting process, a first side of the cutting line 700 may be removed, and the second side of the cutting line 700 may be left unremoved. The recess patterns 506 may be arranged in column and row directions. However, embodiments of the present invention are not limited thereto, and the recess patterns 506 may be arranged regularly or irregularly.

[0126] When the first side of the cutting line 700 is cut in the cutting process, the second side of the cutting line 700 may become vulnerable to impact. In this case, impacts applied to the second side of the cutting line 700 may create cracks, and the cracks may grow and propagate to the display area DA. Here, the recess patterns 506 disposed adjacent to the second side of the cutting line 700 can serve as a crack stopper. That is, the propagation of the cracks can be suppressed by the recess patterns 506.

[0127] FIG. 27 is a cross-sectional view of an organic light-emitting display (OLED) according to an embodiment of the present invention.

[0128] Referring to FIG. 27, the OLED according to the current embodiment includes an array substrate and an encapsulation member. The array substrate has a display area DA and a non-display area NDA located outside the display area DA. The non-display area NDA includes, a substrate 10, a barrier layer 11 which is disposed on the substrate 10, a buffer layer 12 which is disposed on the barrier layer 11, a first insulating layer 25 which is disposed on the buffer layer 12, a second insulating layer 35 which is disposed on the first insulating layer 25, and a plurality of wiring patterns. The wiring patterns are disposed between the first insulating layer 25 and the second insulating layer 35 and on the second insulating layer 35. In addition, the wiring patterns are separated from each other and extend toward a side of the substrate 10. The non-display area NDA further includes a recess pattern which is recessed from a top surface of the second insulating layer 35 by a predetermined depth to expose at least part of a top surface of the substrate 10, and an organic insulating layer 75 which is disposed on the second insulating layer 35 and exposes at least part of a portion of the top surface of the substrate 10 which is exposed by the recess pattern.

[0129] For ease of description, only one unit pixel area is illustrated in FIG. 27. However, the OLED according to the current embodiment is not limited to the one unit pixel area. That is, the OLED according to the current embodiment may include a plurality of unit pixel areas as described above in relation to the array substrates 100 according to FIGS. 1-21 or in relation to the array substrates 101 according to FIGS. 22-26.

[0130] The display area DA of the array substrate in the OLED according to the current embodiment will first be described.

[0131] The substrate 10 is a plate-shaped member and may support other elements which will be described later. The substrate 10 may be, for example, an insulating substrate and may be formed of a polymer material including glass, quartz, or plastic.The substrate 10 may be formed of, for example, polyimide. However, the material of the substrate 10 is not limited to polyimide. For example, the substrate 10 may include polyethersulfone (PES), polyethylenenaphthalate (PEN), polyethylene (PE), polyvinyl chloride (PVC), polyethylene terephthalate (PET), or combinations thereof.

[0132] The substrate 10 may be, a rigid substrate. However, the substrate 10 is not limited to the rigid substrate and may also be a ductile or flexible substrate. That is, in the present specification, the term "substrate" can be understood as a concept that encompasses, for example, a bendable, foldable, and rollable flexible substrate.

[0133] As shown in FIG. 27, the substrate 10 has a single layer structure. However, the structure of the substrate 10 is not limited to the single layer structure. That is, in an alternative embodiment, the substrate 10 may have a stacked structure of two or more layers. In other words, the substrate 10 may include, for example, a base layer and a protective layer disposed on the base layer.

[0134] The base layer may be formed of, an insulating material. In one embodiment, the base layer may be formed of, for example, polyimide. However, the material of the base layer is not limited to polyimide. The protective

layer may be disposed on the base layer. The protective layer may be formed of, for example, an organic material. For example, the protective layer may include one or more materials selected from polyethylene terephthalate and polyethylene naphthalate. However, the material of the protective layer is not limited to the above examples.

[0135] A barrier layer 11 is disposed on the substrate 10. The barrier layer 11 may prevent penetration of impurity elements from the substrate 10 and planarize a surface of the substrate 10. The barrier layer 11 may be formed of, for example, silicon oxide or silicon nitride. However, the material of the barrier layer 11 is not limited to the above examples. Alternatively, the barrier layer 11 can be omitted depending on the material of the substrate 10 or process conditions.

[0136] A buffer layer 12 is formed on the barrier layer 11 to cover the barrier layer 11. The buffer layer 12 may be, for example, an inorganic layer formed of an inorganic material.The buffer layer 12 may be formed of, for example, one or more materials selected from the group consisting of silicon oxide (SiOx), silicon nitride (SiNx), aluminum oxide (AlOx), and silicon oxynitride (SiON). However, the material of the buffer layer 12 is not limited to the above examples. In addition, the buffer layer 12 may have a single layer structure or a stacked structure of two or more layers. In an embodiment in which the buffer layer 12 consists of two layers, the two layers may be formed of different materials. For example, a first layer may be formed of silicon oxide, and a second layer may be formed of silicon nitride. However, the structure of the buffer layer 12 is not limited to the above example.

[0137] A semiconductor layer 40 is formed on the buffer layer 12. The semiconductor layer 40 may be formed of, for example, amorphous silicon or polycrystalline silicon. In this embodiment, the semiconductor layer 40 may be formed by, for example, coating, patterning, and then crystallizing amorphous silicon. However, a method of forming the semiconductor layer 40 is not limited to the above example. In the present specification, the term "semiconductor layer" can be understood as an oxide semiconductor layer, but embodiments of the present invention are not limited thereto.

[0138] A gate insulating layer 20 is formed on the semiconductor layer 40. The gate insulating layer 20 may include, for example, silicon nitride or silicon oxide, but the material of the gate insulating layer 20 is not limited to the above examples. The gate insulating layer 20 may have a single layer structure. However, the structure of the gate insulating layer 20 is not limited to the single layer structure. The gate insulating layer 20 may also have a multilayer structure which includes two or more insulating layers with different physical properties.

[0139] A gate wiring including a gate line 50, a gate electrode 51 and a gate pad is disposed on the gate insulating layer 20. The gate wiring may be formed of, for example, one or more materials selected from the group consisting of aluminum (Al)-based metal such as aluminum or an aluminum alloy, silver (Ag)-based metal such as silver or a silver alloy, copper (Cu)-based metal such as copper or a copper alloy, molybdenum (Mo)-based metal such as molybdenum or a molybdenum alloy, chromium (Cr), titanium (Ti), and tantalum (Ta). In addition, in an embodiment, the gate wiring may be formed of, for example, at least one material selected from the group consisting of, for example, nickel (Ni), gold (Au), palladium (Pd), platinum (Pt), neodymium (Nd), zinc (Zn), cobalt (Co), silver (Ag), manganese (Mn) or any alloys thereof. However, the material of the gate wiring is not limited to the above examples, and any transparent or semitransparent material having conductivity can be used to form the gate wiring.

[0140] The gate line 50 is provided in a plurality as described above, and the gate lines 50 extend in a direction to be parallel to each other.

[0141] An interlayer insulating film 30 is disposed on the gate wiring to cover the gate wiring. The interlayer insulating film 30 may be, for example, an inorganic layer formed of an inorganic material. The interlayer insulating film 30 may include, for example, silicon nitride or silicon oxide, but the material of the interlayer insulating film 30 is not limited to the above examples. The interlayer insulating film 30 may have a single layer structure. However, the structure of the interlayer insulating film 30 is not limited to the single layer structure. The interlayer insulating film 30 may also have a multilayer structure which includes two or more insulating layers with different physical properties. The interlayer insulating film 30 having the multilayer structure will be described later.

[0142] A data wiring including, for example, a source electrode 61, a drain electrode 62 and a data line 60 is disposed on the interlayer insulating film 30. The data wiring may be formed of, for example, molybdenum, chromium, a refractory metal such as tantalum and titanium, or an alloy of these materials. In addition, in an embodiment, the data wiring may be formed of, for example, at least one material selected from the group consisting of, for example, nickel (Ni), gold (Au), palladium (Pd), platinum (Pt), neodymium (Nd), zinc (Zn), cobalt (Co), silver (Ag), manganese (Mn) or any alloys thereof. However, the material of the data wiring is not limited to the above examples, and any transparent or semitransparent material having conductivity can be used to form the data wiring.

[0143] The data line 60 may deliver a data signal and is placed to intersect the gate line 50. That is, the gate line 50 extends in a horizontal direction, and the data line 60 extends in a vertical direction to intersect the gate line 50.

[0144] In this embodiment, the data line 60 and the gate line 50 are bent.

[0145] The source electrode 61 is a portion of the data line 60 and lies in the same plane with the data line 60. The drain electrode 62 extends parallel to the source electrode 61 and is parallel to the portion of the data line 60.

[0146] The gate electrode 51, the source electrode 61

and the drain electrode 62 form one TFT, together with the semiconductor layer 40. A channel of the TFT is formed in the semiconductor layer 40 between the source electrode 61 and the drain electrode 62.

[0147] A planarization layer 70 is disposed on the data wiring to cover the data wiring and the interlayer insulating film 30. The planarization layer 70 is relatively thicker than the interlayer insulating film 30. Due to this difference in the thicknesses of the planarization layer 70 and the interlayer insulating film 30, a top surface of the planarization layer 70 may be relatively flatter than a bottom surface thereof which contacts the interlayer insulating film 30 and the source and drain electrodes 61 and 62.

[0148] A first contact hole is formed in the planarization layer 70 to expose at least part of the drain electrode 62.The first contact hole penetrates through the planarization layer 70 and partially exposes a top surface of the drain electrode 62.

[0149] A first electrode 80 is disposed on the planarization layer 70 and an exposed portion of the drain electrode 62. That is, the first electrode 80 covers the planarization layer 70, sidewalls of the first contact hole, and the top surface of the drain electrode 62. Accordingly, the first electrode 80 and the drain electrode 62 may be electrically connected to each other. The first electrode 80 may be, but is not limited to, an anode. The first electrode 80 may be formed of, for example, indium tin oxide, indium zinc oxide, cadmium tin oxide (CTO), aluminum zinc oxide (AZO), indium tin zinc oxide (ITZO), cadmium oxide (CdO), hafnium oxide (HfO), indium gallium zinc oxide (InGaZnO), indium gallium zinc magnesium oxide (InGaZnMgO), indium gallium magnesium oxide (InGaMgO) or indium gallium aluminum oxide (InGaAlO). However, the material of the first electrode 80 is not limited to the above examples.

[0150] A pixel defining layer 90 is disposed on the first electrode 80. The pixel defining layer 90 exposes at least part of the first electrode 80. The pixel defining layer 90 may be formed of, for example, one or more organic materials selected from benzocyclobutene, polyimide, polyamide (PA), acrylic resin, and phenolic resin. Alternatively, the pixel defining layer 90 may be formed of, for example, an inorganic material such as silicon nitride. The pixel defining layer 90 may also be formed of, for example, a photosensitizer containing black pigments. In this case, the pixel defining layer 90 may serve as a light-blocking member.

[0151] An organic layer 91 is disposed on a portion of the first electrode 80 which is exposed by the pixel defining layer 90. The organic layer 91 may include, for example, organic material layers included in an OLED, that is, an organic light-emitting layer (EML), a hole injection layer (HIL), a hole transport layer (HTL), an electron injection layer (EIL), and an electron transport layer (ETL). The organic layer 91 may have a single layer structure including one of the organic material layers or a multilayer structure including two or more of the organic material layers.

[0152] A second electrode 92 is formed on the organic layer 91. The second electrode 92 covers the pixel defining layer 90 and the organic layer 91.The second electrode 92 is a whole-surface electrode which covers the pixel defining layer 90 and the organic layer 91. The second electrode 92 may be, for example, a cathode.

[0153] The second electrode 92 may be formed of, indium tin oxide, indium zinc oxide, cadmium tin oxide (CTO), aluminum zinc oxide (AZO), indium tin zinc oxide (ITZO), cadmium oxide (CdO), hafnium oxide (HfO), indium gallium zinc oxide (InGaZnO), indium gallium zinc magnesium oxide (InGaZnMgO), indium gallium magnesium oxide (InGaMgO) or indium gallium aluminum oxide (InGaAlO), but the material of the second electrode 92 is not limited to the above examples.

[0154] The non-display area NDA of the array substrate is substantially identical to the non-display area NDA of any one of the array substrates 100 according to FIGS. 1-21 or to any one of the array substrates 101 according to FIGS. 22-26.

[0155] The encapsulation member is disposed on the array substrate. In the present specification, the encapsulation member may be an encapsulation layer 803 or an encapsulation substrate 800. In FIG. 27, a case where the encapsulation member is the encapsulation substrate 800 is illustrated. However, the encapsulation member is not limited to the encapsulation substrate 800. A case where the encapsulation member is the encapsulation layer 803 will be described later with reference to FIG. 28. The encapsulation substrate 800 is attached to the array substrate with, for example, an encapsulant (not shown).

[0156] To attach the encapsulation substrate 800 to the array substrate, the encapsulant may be, for example, at least one of an epoxy adhesive, a UV-curing adhesive, frit, and their equivalents. However, the material of the encapsulant is not limited to the above examples.

[0157] The encapsulation substrate 800 may be attached and coupled to the array substrate with the above-described encapsulant. The encapsulation substrate 800 may be formed of, for example, any one of transparent glass, transparent plastic, transparent polymer, and their equivalents. However, the material of the encapsulation substrate 800 is not limited to the above examples.

[0158] A conductive layer 801 is formed on a surface of the encapsulation substrate 800 which faces the array substrate. The conductive layer 801 may ground external static electricity that is introduced into the OLED through the encapsulation substrate 800.

[0159] FIG. 28 is a cross-sectional view of an OLED according to an embodiment of the present invention.

[0160] Referring to FIG. 28, the OLED according to the current embodiment is different from the OLED according to the embodiment of FIG. 27 in that the encapsulation member is the encapsulation layer 803.

[0161] As described above, in this embodiment, the encapsulation member may be the encapsulation layer

803. The encapsulation layer 803 covers a display area DA and a non-display area NDA. In this embodiment, the encapsulation layer 803 exposes, at least part of a wiring line 401 and/or a wiring pad 402. However, embodiments of the present invention are not limited thereto.

[0162] The encapsulation layer 803 may be formed of, for example, an organic material and/or an inorganic material.

[0163] Examples of the organic material used to form the encapsulation layer 803 may include, but are not limited to, epoxy, acrylate, and urethane acrylate. Examples of the inorganic material used to form the encapsulation layer 803 may include, but are not limited to, aluminum oxide and silicon oxide.

[0164] In FIG. 28, the encapsulation layer 803 has a single layer structure. However, the structure of the encapsulation layer 803 is not limited to the single layer structure. The encapsulation layer 803 may also have a stacked structure of one or more layers. The encapsulation layer 803 may have a structure in which an organic layer and an inorganic layer are alternately stacked at least once. However, this is merely an example, and the structure of the encapsulation layer 803 is not limited to this example.

[0165] Embodiments of the present invention provide at least one of the following benefits.

[0166] That is, it is possible to prevent cracks from being created in an array substrate by external impacts.

[0167] In addition, it is possible to suppress the growth or propagation of cracks created by external impacts.

[0168] However, the effects of embodiments of the present invention are not restricted to the ones set forth herein, as would be apparent one of ordinary skill in the art referencing the present disclosure set forth herein.

[0169] Having described embodiments of the present invention, it is further noted that it is readily apparent to those of ordinary skill in the art that various modifications may be made without departing from the scope of the invention which is defined by the metes and bounds of the appended claims.

[0170] The present invention may be further understood with reference to the following numbered clauses:

1. An array substrate comprising:
a display area (DA) and a non display area (NDA) located outside the display area, wherein the non display area comprises:

a substrate (10);
a buffer layer (12) disposed on the substrate;
a first insulating layer (25) disposed on the buffer layer;
a second insulating layer (35) disposed on the first insulating layer; and
a plurality of wiring patterns disposed on the second insulating layer (35), wherein the wiring patterns are separated from each other and each of the wiring patterns comprises a wiring line (401, 411) extending toward a side of the substrate;
characterised by a recess pattern (500, 501, 503, 504, 507, 508) disposed between adjacent wiring lines (401) .

2. An array substrate according to clause 1, wherein a top surface of the substrate (10) is exposed by the recess pattern (500, 501, 503, 504, 507, 508).

3. An array substrate according to clause 2, wherein a bottom surface of the recess pattern (500, 501, 503, 504, 507, 508) comprises the top surface of the substrate (10), and sidewalls of the recess pattern comprise inner side surfaces of the first insulating layer (25), the second insulating layer (35), and the buffer layer (12).

4. An array substrate according to clause 1, wherein the wiring line (411) comprises at least a curved shape portion.

5. An array substrate according to clause 1, wherein the wiring line (411) extends in a zigzag shape.

6. An array substrate according to clause 1, wherein each of the wiring patterns further comprises a wiring pad (402) which comprises an end wider than the wiring line (401),
wherein the recess pattern (501) is extended to between the adjacent wiring pads (402), and wherein a width of the recess pattern (501) disposed between the wiring lines (401) is greater than a width of the recess pattern (501) disposed between the wiring pads (402).

7. An array substrate according to clause 1, wherein the recess pattern is provided in a plural number and the recess patterns are disposed between the wiring patterns.

8. An array substrate according to clause 1, wherein the recess pattern (503, 504) is arranged in a matrix of a plurality of columns and a plurality of rows.

9. An array substrate according to clause 6, further comprising a recess groove (502) disposed inside the wiring pad (402) and penetrating through the wiring pad (402), the second insulating layer (35), the first insulating layer (25) and the buffer layer (12) to expose a top surface of the substrate (10).

10. An array substrate according to clause 6, wherein the recess pattern is disposed outside an outermost wiring line among the wiring lines.

11. An array substrate according to clause 1, further comprising a cell ID pattern (45) disposed outside

the outermost wiring line among the wiring lines (401), wherein the recess pattern (505) is disposed along an outer circumference of the cell ID pattern.

12. An array substrate according to clause 1, further comprising at least one cutting line (700) which traverses at least part of the substrate and is defined on the substrate, and wherein the recess pattern (506) is disposed adjacent to the cutting line.

13. An array substrate according to any preceding clause, wherein the buffer layer (12) comprises at least one material selected from the group consisting of silicon oxide, silicon nitride, aluminum oxide, and silicon oxynitride.

14. An array substrate according to any preceding clause, wherein the substrate (10) is a flexible substrate.

Claims

1. An organic light-emitting display (OLED) comprising:

an array substrate comprising a display area and a non-display area located outside the display area; and
an encapsulation member disposed on the array substrate,
wherein the non-display area of the array substrate comprises:

a substrate,
a barrier layer disposed on the substrate,
a buffer layer disposed on the barrier layer,
a first insulating layer disposed on the buffer layer,
a second insulating layer disposed on the first insulating layer,
a plurality of wiring patterns disposed between the first insulating layer and the second insulating layer and/or on the second insulating layer, and wherein the wiring patterns are separated from each other, and extend toward a side of the substrate,
a recess pattern disposed adjacent to the wiring patterns and recessed from a top surface of the second insulating layer to expose at least part of the top surface of the substrate, and
an organic insulating layer disposed on the second insulating layer and exposing at least part of a portion of the top surface of the substrate which is exposed by the recess pattern.

2. The OLED of claim 1, wherein the encapsulation member is an encapsulation substrate or an encapsulation layer.

3. The array substrate of claim 2, wherein the organic insulating layer disposed on the second insulating layer covers sidewalls of the recess pattern and a bottom surface of the recess pattern.

4. An organic light-emitting display (OLED) comprising:

an array substrate comprising a display area, and a non-display area disposed outside the display area; and
an encapsulation member disposed on the array substrate,
wherein the display area comprises:

a display area substrate,
a display area barrier layer disposed on the display area substrate,
a display area buffer layer disposed on the display area barrier layer,
a semiconductor layer disposed on the display area buffer layer,
a gate insulating layer disposed on the semiconductor layer,
a gate wiring including a gate line, a gate electrode and a gate pad disposed on the gate insulating layer,
an interlayer insulating film covering the gate wiring,
a data wiring including a source electrode, a drain electrode, and a data line disposed on the interlayer insulating film,
a planarization layer disposed on the data wiring and the interlayer insulating film,
a first electrode disposed on the planarization layer and electrically connected to the drain electrode,
a pixel defining layer disposed on the first electrode and exposing a portion of the first electrode,
an organic layer disposed on the portion of the first electrode exposed by the pixel defining layer, and
a second electrode disposed on the organic layer and the pixel defining layer, and

wherein the non-display area comprises:

a non-display area substrate,
a non-display area barrier layer disposed on the non-display area substrate,
a non-display area buffer layer disposed on the non-display area barrier layer,
a first insulating layer disposed on the non-display area buffer layer,
a second insulating layer disposed on the

first insulating layer,
a plurality of wiring patterns disposed between the first insulating layer and the second insulating layer and/or on the second insulating layer, and wherein the wiring patterns are separated from each other, and extend toward a side of the non-display area substrate;
a recess pattern disposed adjacent to the wiring patterns and recessed from a top surface of the second insulating layer to expose at least part of the top surface of the non-display area substrate, and
an organic insulating layer disposed on the second insulating layer and exposing at least part of a portion of the top surface of the non-display area substrate which is exposed by the recess pattern.

5. An array substrate comprising:

a substrate;
a buffer layer disposed on the substrate;
a first insulating layer disposed on the buffer layer;
a second insulating layer disposed on the first insulating layer;
a plurality of wiring patterns disposed on the second insulating layer, and wherein the wiring patterns are separated from each other; and
a recess pattern disposed adjacent to the wiring patterns.

6. The array substrate of claim 5, wherein the top surface of the substrate is exposed by the recess pattern.

7. The array substrate of claim 5, wherein each of the wiring patterns comprises a wiring line extending toward the side of the substrate,
wherein the recess pattern is disposed between the adjacent wiring lines.

8. The array substrate of claim 7, wherein the wiring line comprises at least a curved shape portion.

9. The array substrate of claim 7, the wiring line is extended in a zigzag shape.

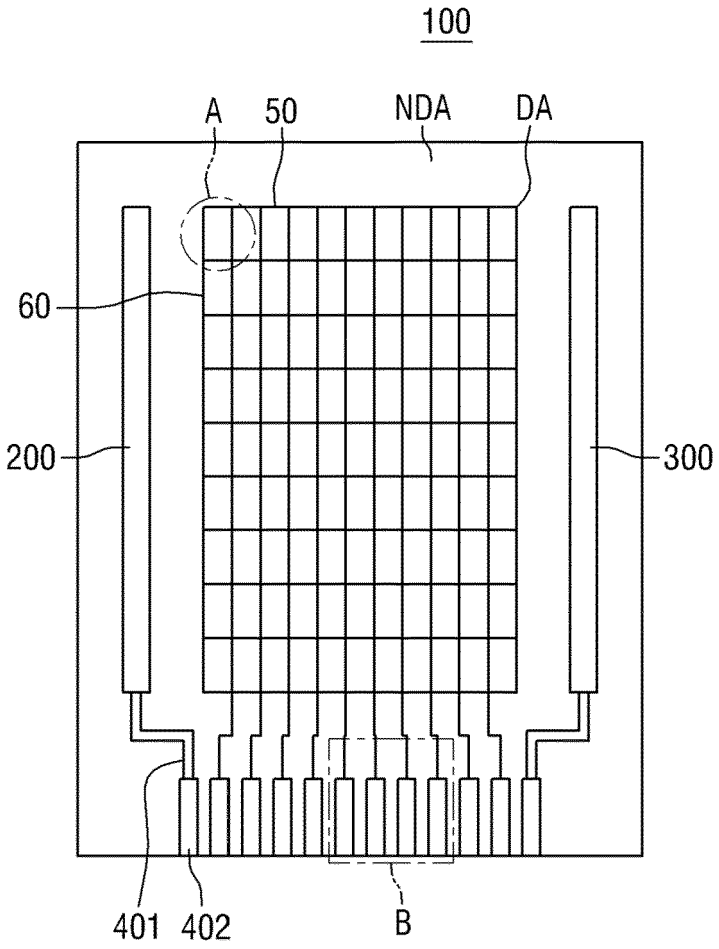
10. The array substrate of claim 7, wherein each of the wiring patterns further comprises a wiring pad which comprises an end wider than the wiring line,
wherein the recess pattern is extended to between the adjacent wiring pads,
and wherein a width of the recess pattern disposed between the wiring lines is greater than a width of the recess pattern disposed between the wiring pads.

11. The array substrate of claim 5, wherein the recess pattern is provided in a plurality, and the plurality of the recess patterns are arranged in a matrix of a plurality of columns and a plurality of rows.

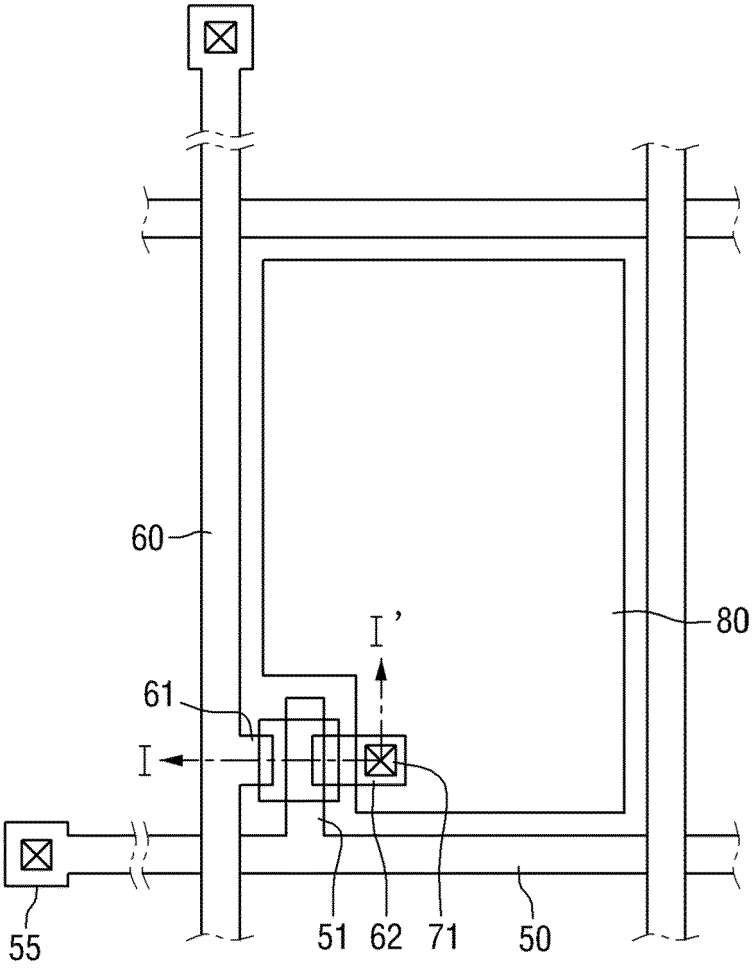
12. The array substrate of claim 5, further comprising a cell ID pattern disposed outside the outermost wiring line among the wiring lines, wherein the recess pattern is disposed along an outer circumference of the cell ID pattern.

13. The array substrate of claim 5, further comprising at least one cutting line which traverses at least part of the substrate and is defined on the substrate, and wherein the recess pattern is disposed adjacent to the cutting line.

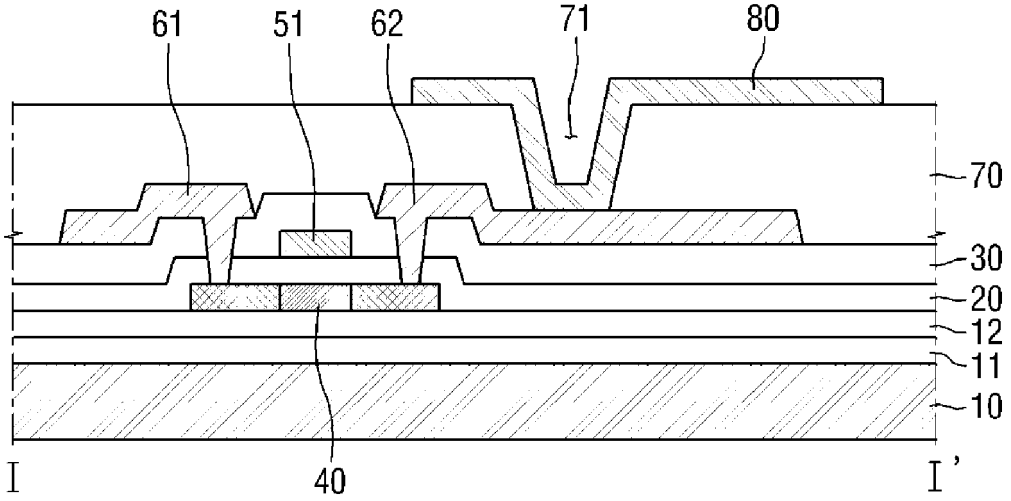
【 Fig. 1】



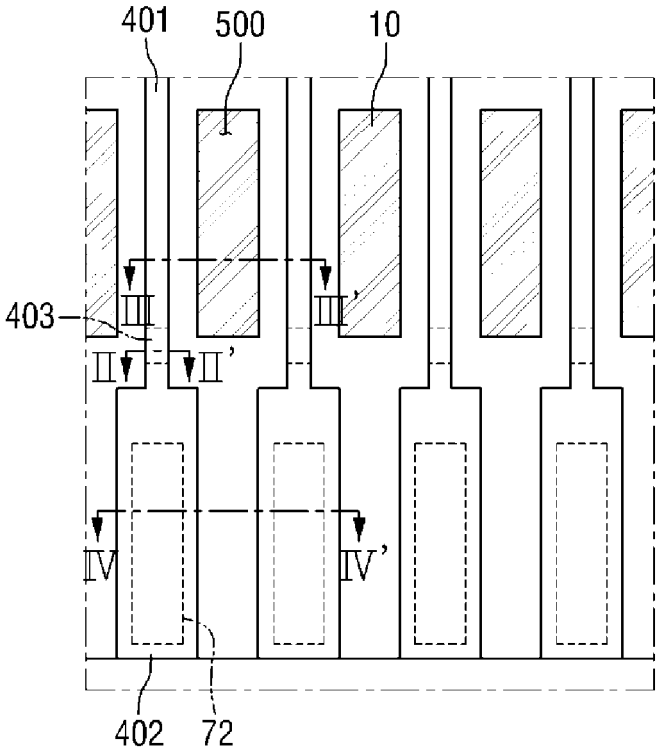
【Fig. 2】



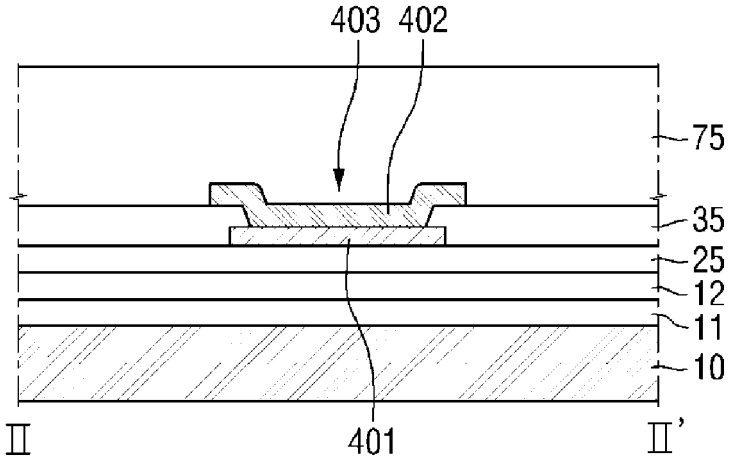
【Fig. 3】



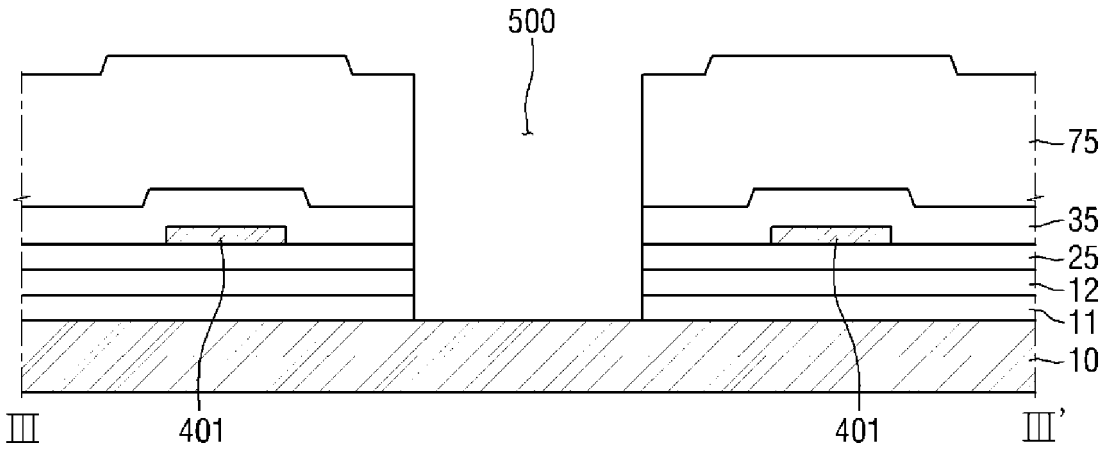
【Fig. 4】


401
500
10
403
III
III'
II
II'
IV
IV'
402
72

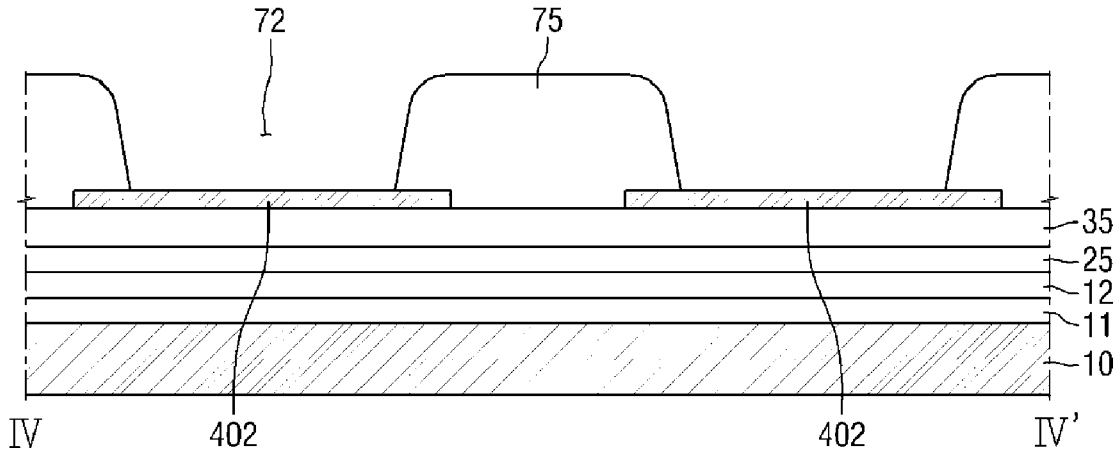
【Fig. 5】


403
402
75
35
25
12
11
10
II
401
II'

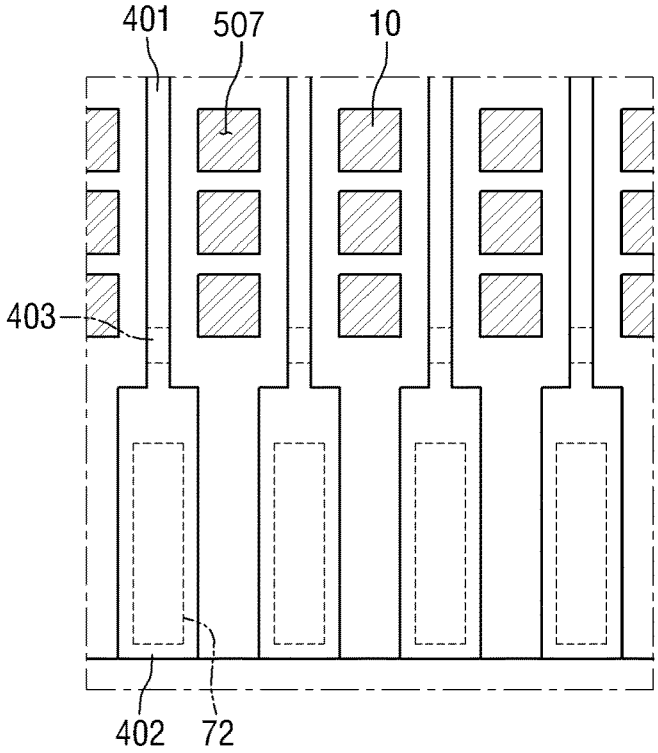
【 Fig. 6】



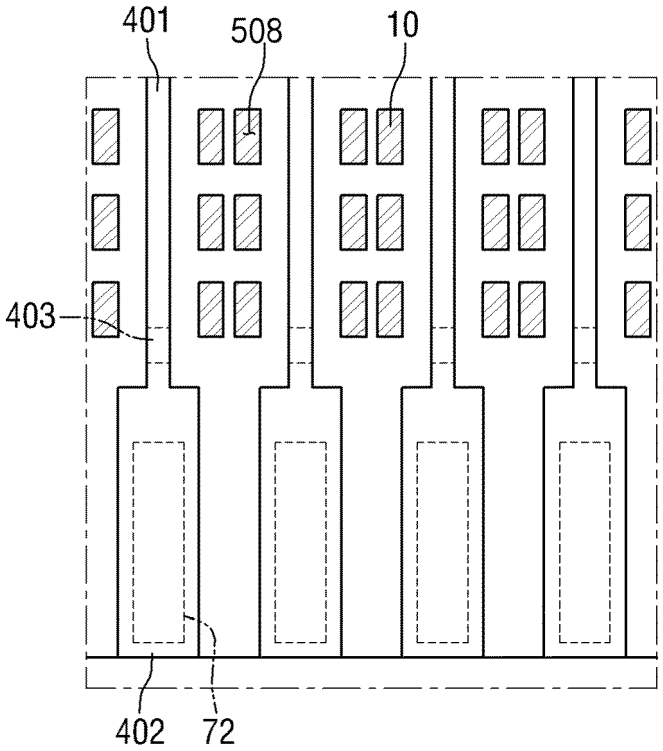
【Fig. 7】



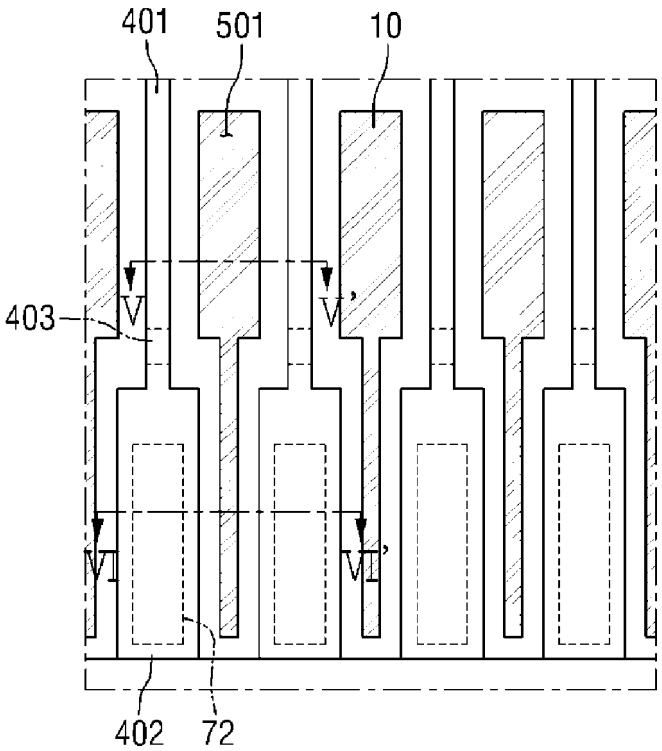
【Fig. 8】



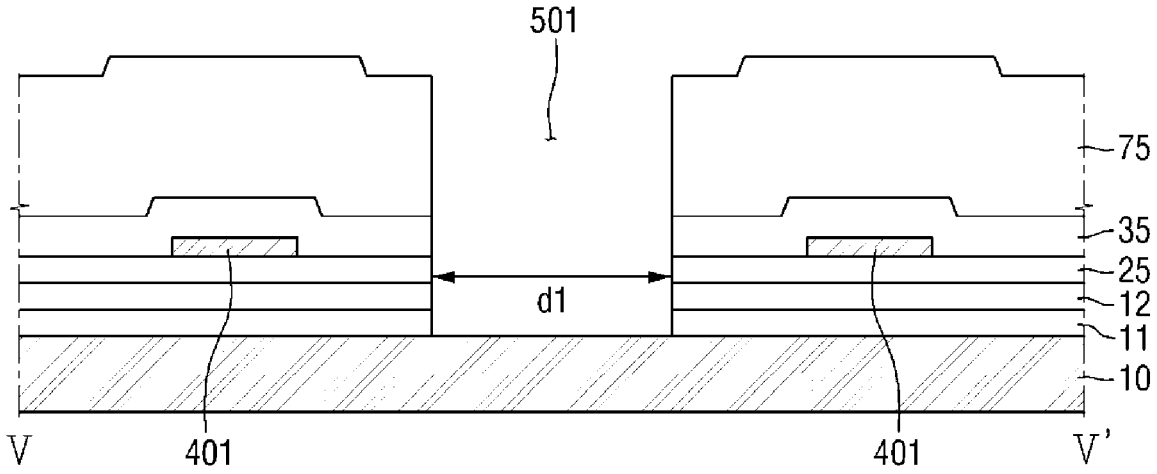
【 Fig. 9】



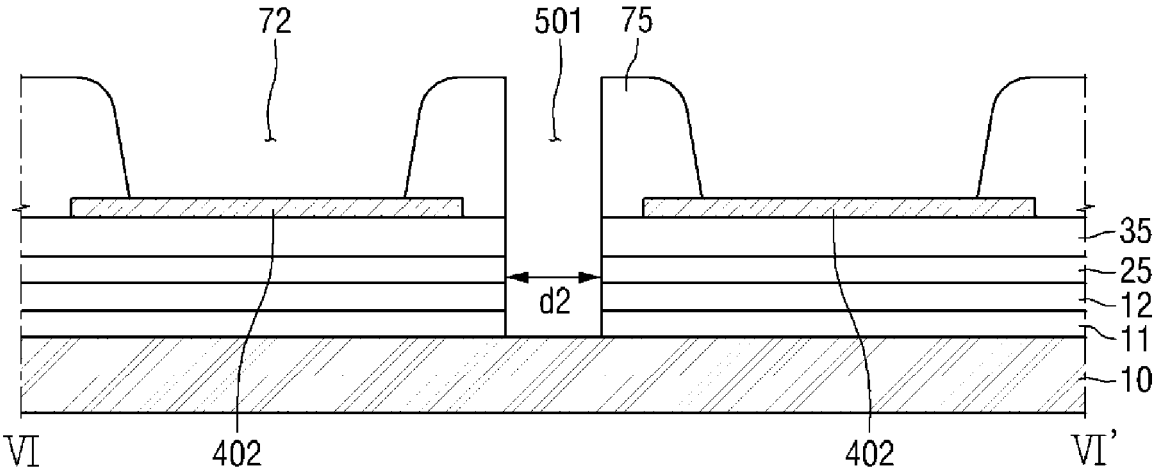
【 Fig. 10】



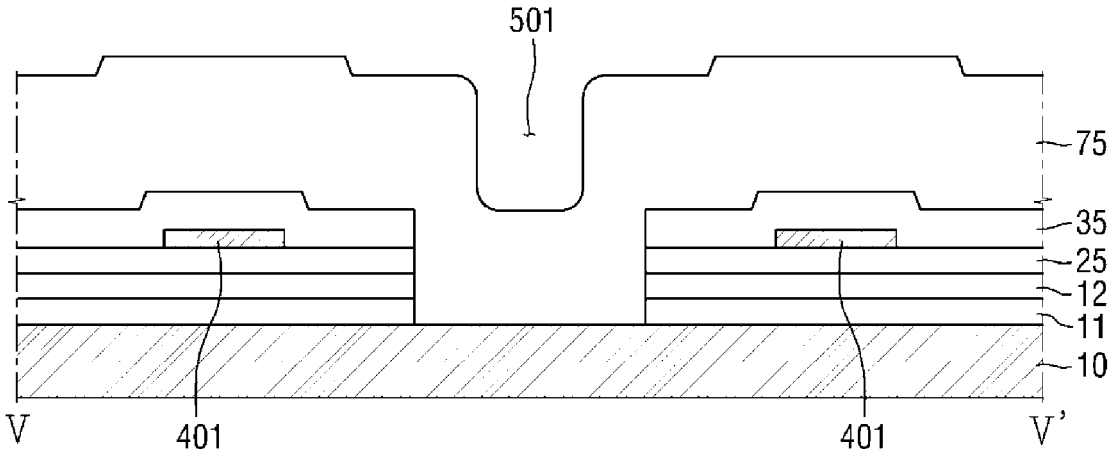
【Fig. 11】



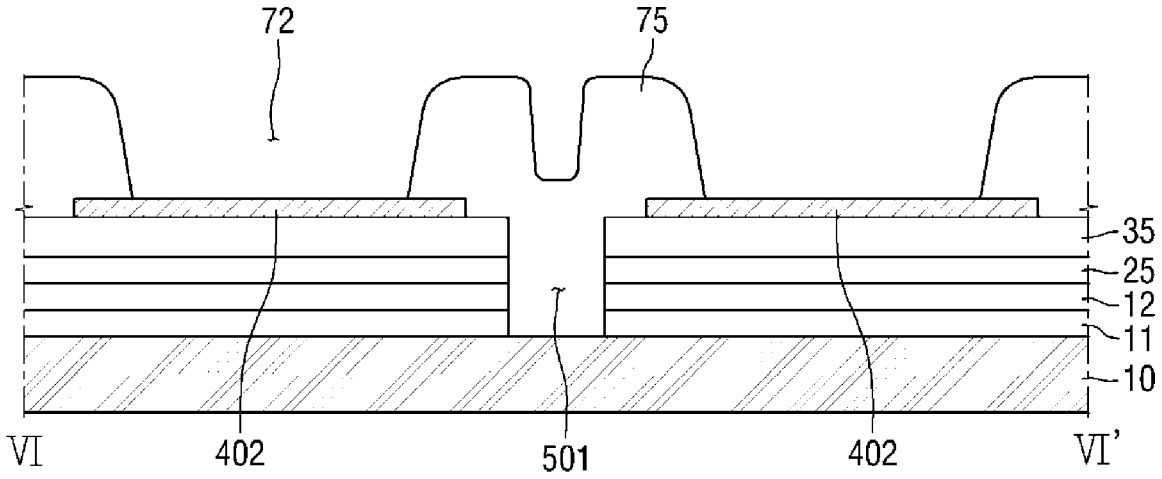
【Fig. 12】



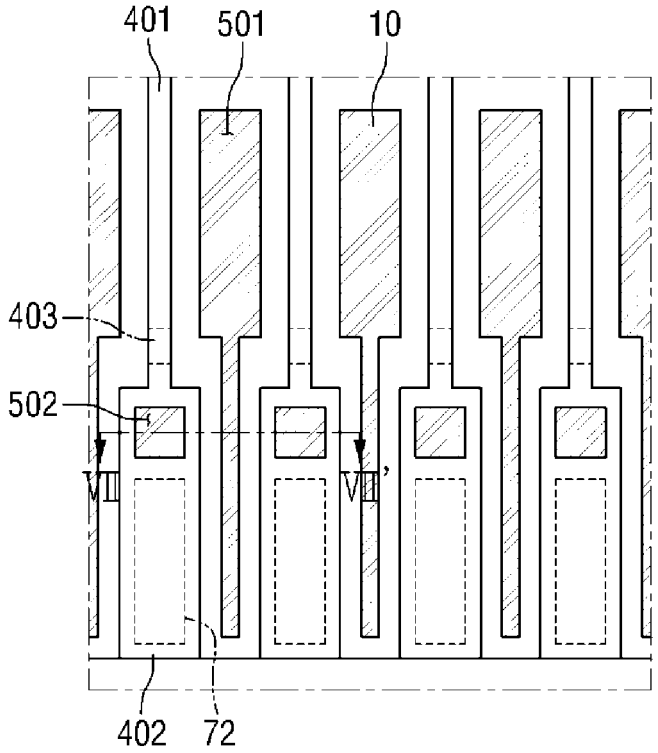
【Fig. 13】



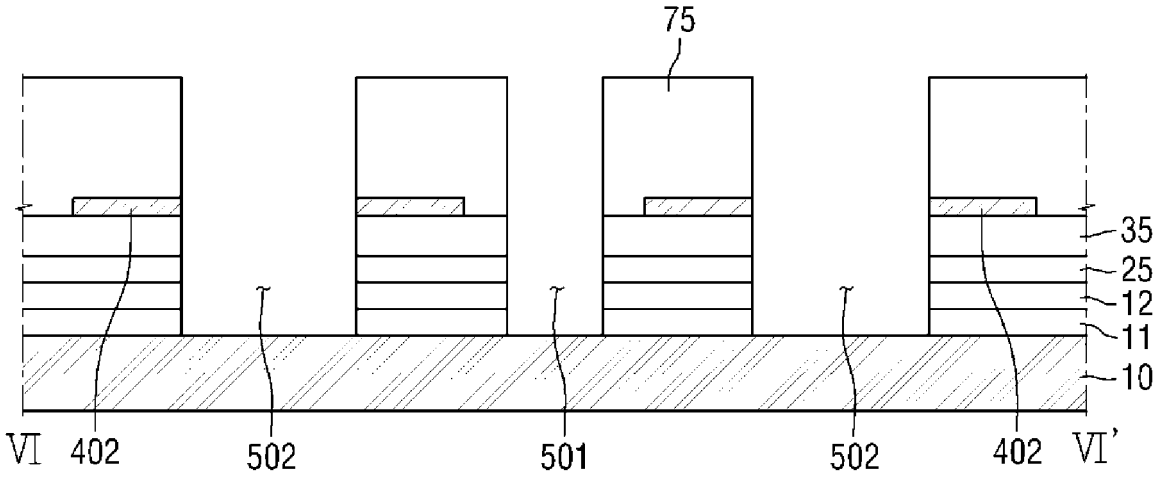
【Fig. 14】


72
75
35
25
12
11
10
VI
402
501
402
VI'

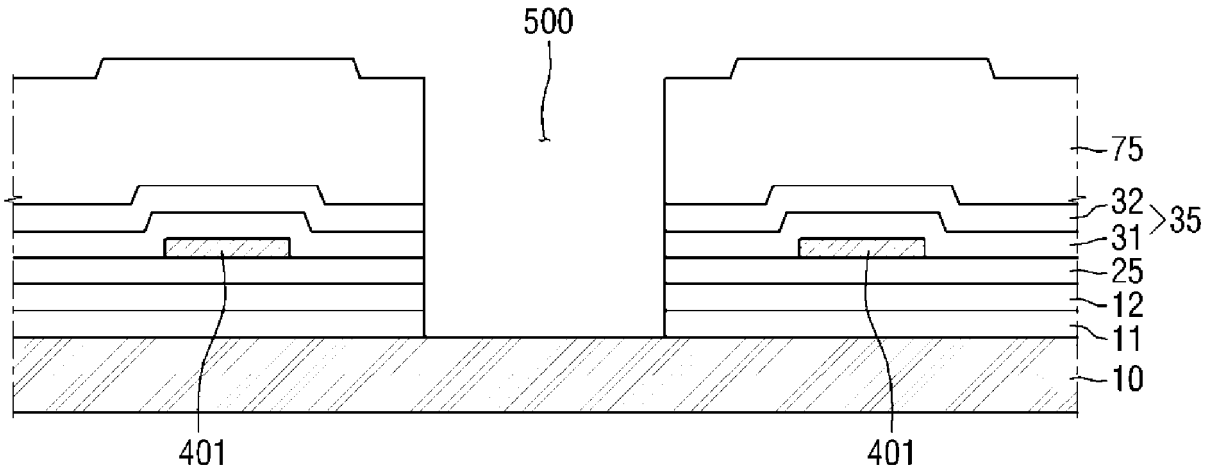
【Fig. 15】


401
501
10
403
502
VII
VII'
402
72

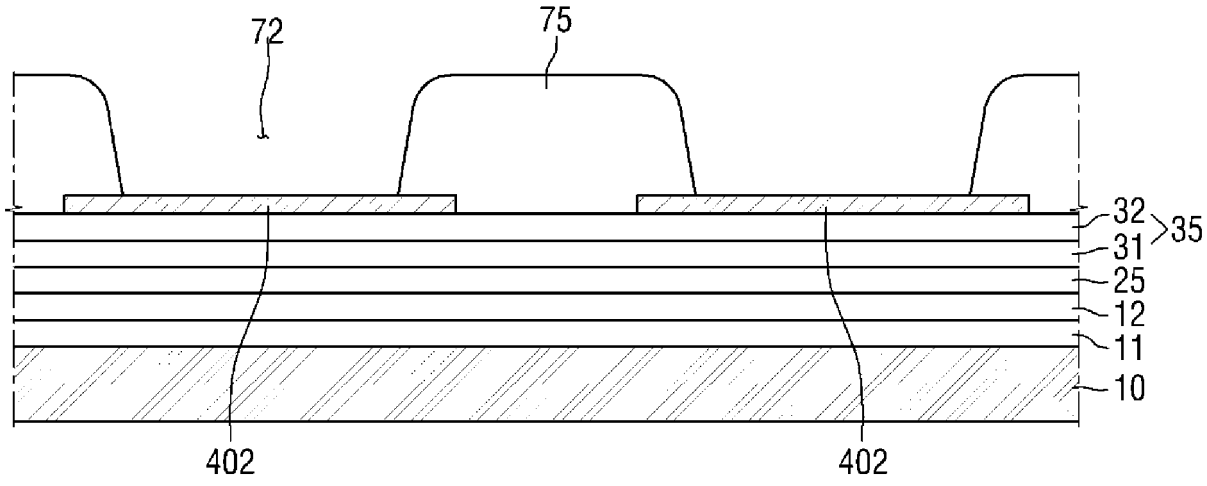
【Fig. 16】



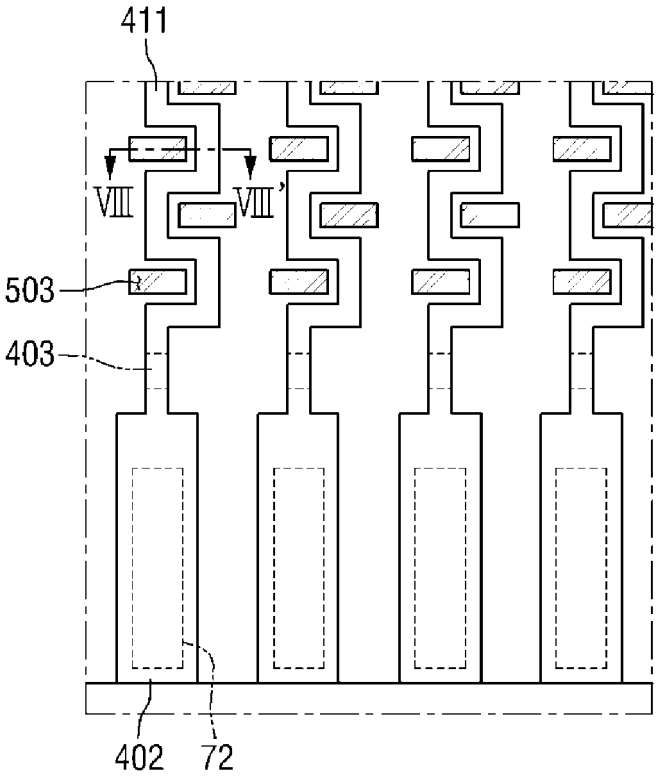
【Fig. 17】



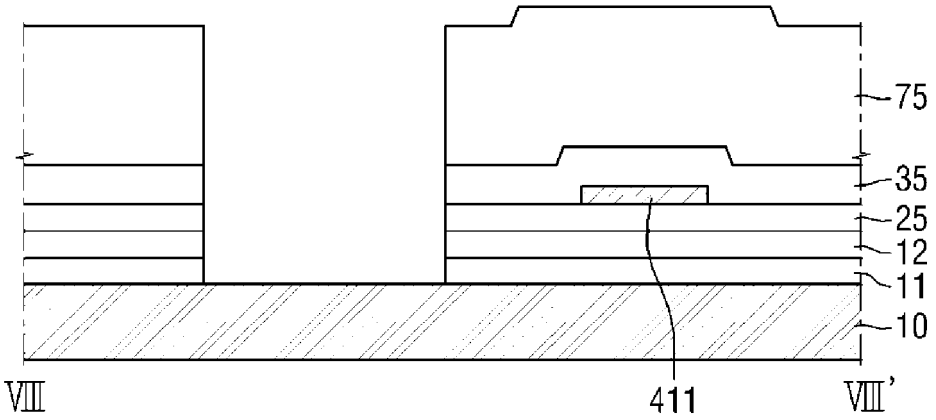
【Fig. 18】



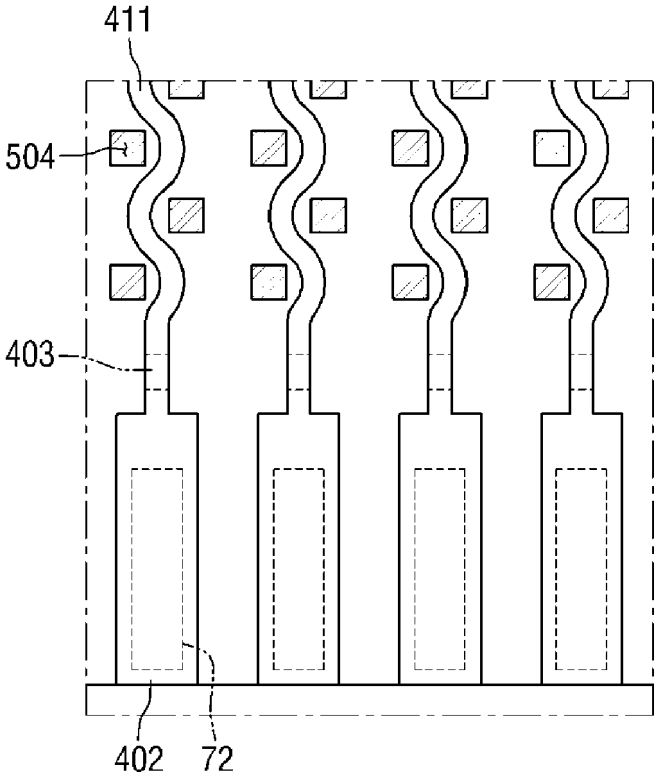
【Fig. 19】



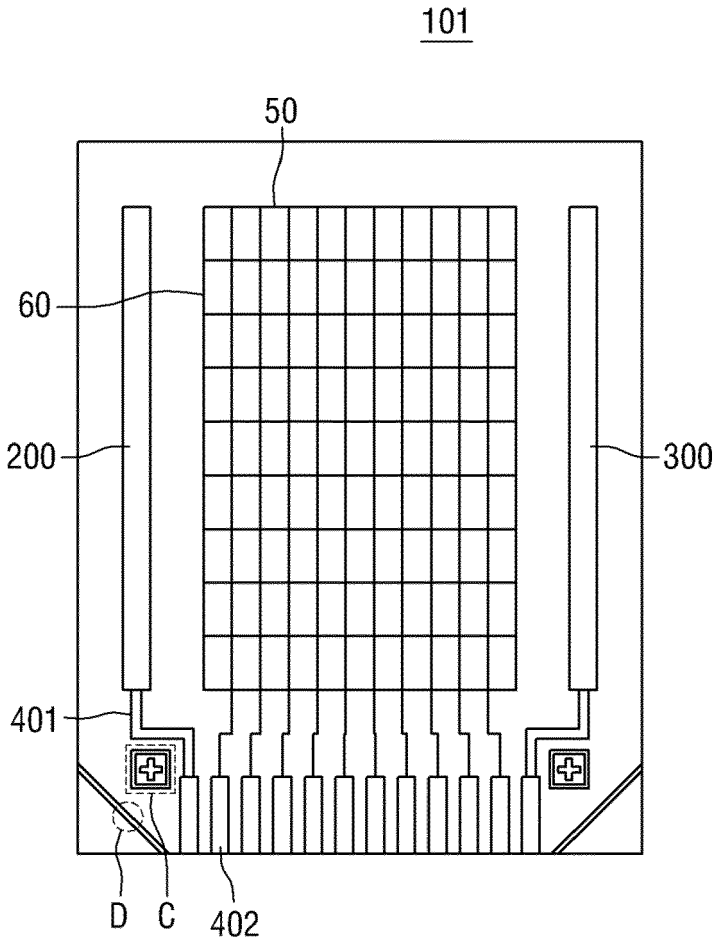
【Fig. 20】



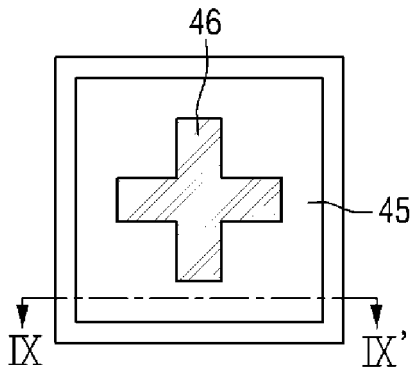
【Fig. 21】



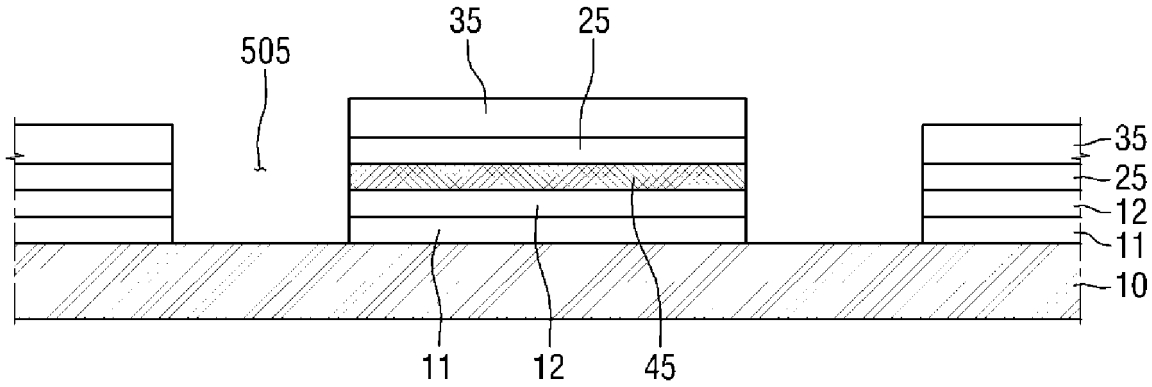
【Fig. 22】



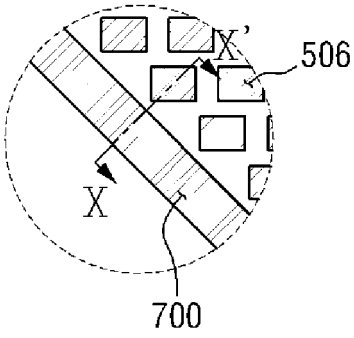
【Fig. 23】



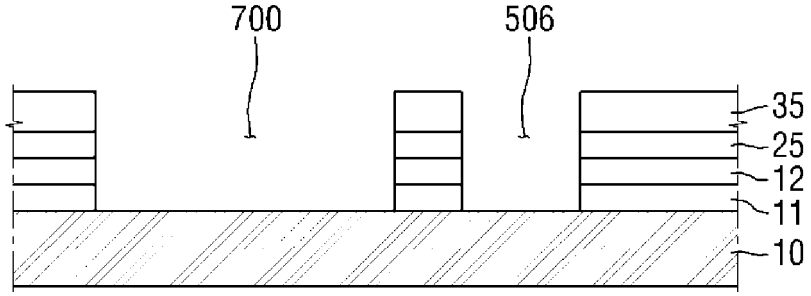
【Fig. 24】



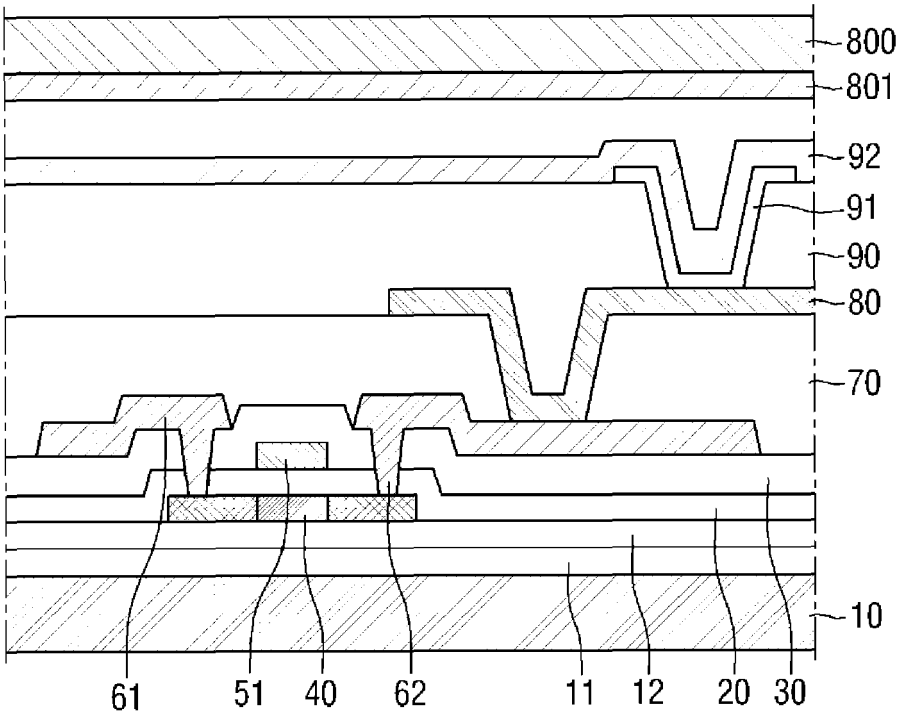
【Fig. 25】



【Fig. 26】



【Fig. 27】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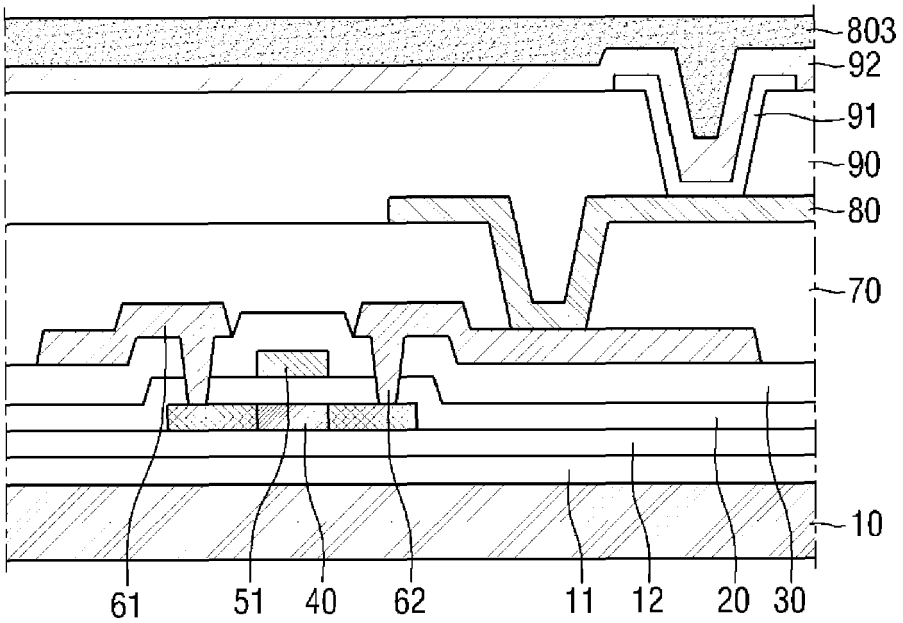
【Fig. 28】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EUROPEAN SEARCH REPORT

Application Number
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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
Munich	28 July 2021	Bernabé Prieto, A

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