



(11) **EP 3 739 565 A1**

(12) **EUROPEAN PATENT APPLICATION**
published in accordance with Art. 153(4) EPC

(43) Date of publication:
18.11.2020 Bulletin 2020/47

(51) Int Cl.:
G09G 3/3225 (2016.01) G09G 3/3233 (2016.01)

(21) Application number: **18899135.0**

(86) International application number:
PCT/CN2018/117758

(22) Date of filing: **27.11.2018**

(87) International publication number:
WO 2019/137105 (18.07.2019 Gazette 2019/29)

(84) Designated Contracting States:
AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO RS SE SI SK SM TR
Designated Extension States:
BA ME
Designated Validation States:
KH MA MD TN

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(30) Priority: **11.01.2018 CN 201810026813**

(54) **PIXEL CIRCUIT, DRIVE METHOD, ELECTROLUMINESCENT LIGHT EMITTING DISPLAY PANEL, AND DISPLAY APPARATUS**

(57) A pixel circuit, a drive method, an electroluminescent light emitting display panel, and a display apparatus, the pixel circuit (PX) comprising: a light emitting device (L); a drive transistor (M0) is configured to generate a drive current (IL) during a light emitting phase in order to drive the light emitting device (L) to emit light; a gate electrode (G) of the drive transistor (M0) is respectively coupled to a capacitance circuit (3) and a data write circuit (2), a first electrode (S) of the drive transistor (M0) is coupled to a reset circuit (1), and a second electrode

(D) of the drive transistor (M0) is respectively coupled to the reset circuit (1) and a first electrode of the light emitting device (L); the capacitance circuit (3) is configured to store the voltage of the gate electrode (G) of the drive transistor (M0); the data write circuit (2) is configured to provide a data signal (Data) to the gate electrode (G) of the drive transistor (M0) during a data write phase; and the reset circuit (1) is configured to reset the first electrode (S) and the second electrode (D) of the drive transistor (M0) during a reset phase.

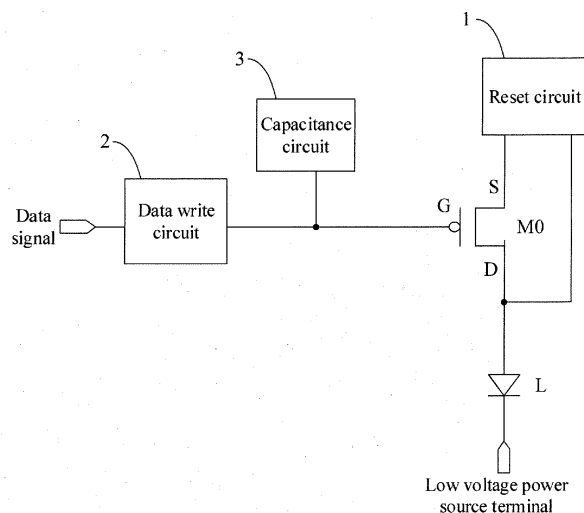


Fig. 1

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Description

[0001] The present application claims priority to Chinese Patent Application No. 201810026813.6, entitled "PIXEL CIRCUIT, DRIVE METHOD, ELECTROLUMINESCENT LIGHT EMITTING DISPLAY PANEL, AND DISPLAY APPARATUS", filed to Patent Office of the People's Republic of China on January 11, 2018, which is incorporated herein by reference in its entirety.

FIELD

[0002] The disclosure relates to the technical field of display and in particular relates to a pixel circuit, a drive method, an electroluminescent light emitting display panel, and a display apparatus.

BACKGROUND

[0003] An organic light emitting diode (OLED) is one of hotspots in the research field of flat panel displays nowadays, and compared with a liquid crystal display (LCD), an OLED display has the advantages such as low energy consumption, low production cost, self-illumination, wide viewing angle and high response speed. At present, the OLED display has begun to replace a traditional LCD display in the field of displays such as mobile phones, tablet personal computers and digital cameras. Different from the LCD of which the brightness is controlled by virtue of a stable voltage, the OLED is driven by a current and is required to be controlled by a stable current to emit light. Generally, a pixel circuit is arranged to drive the OLED to emit light. At present, voltages of a first electrode and a second electrode of a drive transistor may be affected by a voltage during previous frame display when the pixel circuit drives the OLED to emit the light, therefore, the problem of brightness inconsistency exists.

SUMMARY

[0004] Some embodiments of the disclosure provide a pixel circuit, including:

a light emitting device;
a drive transistor, configured to generate a drive current during a light emitting phase in order to drive the light emitting device to emit light; wherein a gate electrode of the drive transistor is respectively coupled to a capacitance circuit and a data write circuit, a first electrode of the drive transistor is coupled to a reset circuit, and a second electrode of the drive transistor is respectively coupled to the reset circuit and a first electrode of the light emitting device;
the capacitance circuit, configured to store the voltage of the gate electrode of the drive transistor;
the data write circuit, configured to provide a data signal to the gate electrode of the drive transistor

during a data write phase;

and the reset circuit, configured to reset the first electrode and the second electrode of the drive transistor during a reset phase.

[0005] Alternatively, in some embodiments of the disclosure, the reset circuit is further coupled to the gate electrode of the drive transistor, is configured to reset the gate electrode of the drive transistor during the reset phase and is configured to compensate the threshold voltage of the drive transistor during a threshold compensation phase.

[0006] Alternatively, in some embodiments of the disclosure, the reset circuit includes a first switching transistor, a second switching transistor and a third switching transistor;

a gate electrode of the first switching transistor is coupled to a first scanning signal line, a first electrode of the first switching transistor is coupled to a first reference signal line, and a second electrode of the first switching transistor is coupled to the second electrode of the drive transistor;

a gate electrode of the second switching transistor is coupled to a second scanning signal line, a first electrode of the second switching transistor is coupled to a second reference signal line, and a second electrode of the second switching transistor is coupled to the first electrode of the drive transistor;

and a gate electrode of the third switching transistor is coupled to a third scanning signal line, a first electrode of the third switching transistor is coupled to a third reference signal line, and a second electrode of the third switching transistor is coupled to the gate electrode of the drive transistor.

[0007] Alternatively, in some embodiments of the disclosure, materials of active layers of the first switching transistor and the third switching transistor include a metal oxide semiconductor material;

and a material of an active layer of the second switching transistor includes a low temperature poly-silicon material.

[0008] Alternatively, in some embodiments of the disclosure, a signal of the first scanning signal line is the same as a signal of the third scanning signal line.

[0009] Alternatively, in some embodiments of the disclosure, a signal of the first reference signal line is the same as a signal of the third reference signal line.

[0010] Alternatively, in some embodiments of the disclosure, the capacitance circuit includes a storage capacitor and a voltage dividing capacitor:

the storage capacitor is coupled between the gate electrode and the first electrode of the drive transistor;

and the voltage dividing capacitor is coupled between the first electrode of the drive transistor and the second reference signal line.

[0011] Alternatively, in some embodiments of the disclosure, the data write circuit includes a fourth switching transistor;

a gate electrode of the fourth switching transistor is coupled to a fourth scanning signal line, a first electrode of the fourth switching transistor is coupled to a data signal line for receiving a data signal, and a second electrode of the fourth switching transistor is coupled to the gate electrode of the drive transistor.

[0012] Alternatively, in some embodiments of the disclosure, a material of an active layer of the fourth switching transistor includes a metal oxide semiconductor material.

[0013] Alternatively, in some embodiments of the disclosure, the pixel circuit further includes a light emitting control circuit; the second electrode of the drive transistor and the reset circuit are respectively coupled to the first electrode of the light emitting device by the light emitting control circuit; wherein the light emitting control circuit is used for controlling the second electrode of the drive transistor and the first electrode of the light emitting device to be turned on or off.

[0014] Alternatively, in some embodiments of the disclosure, the light emitting control circuit includes a fifth switching transistor;

a gate electrode of the fifth switching transistor is coupled to a light emitting control signal line, a first electrode of the fifth switching transistor is coupled to the second electrode of the drive transistor, and a second electrode of the fifth switching transistor is coupled to the first electrode of the light emitting device.

[0015] Alternatively, in some embodiments of the disclosure, a material of an active layer of the fifth switching transistor includes a low temperature poly-silicon material.

[0016] Alternatively, in some embodiments of the disclosure, a signal of the light emitting control signal line is the same as a signal of the second scanning signal line.

[0017] Alternatively, in some embodiments of the disclosure, a material of an active layer of the drive transistor includes a low temperature poly-silicon material.

[0018] Accordingly, some embodiments of the disclosure further provides a pixel circuit, including:

a light emitting device;

a first switching transistor, a gate electrode of the first switching transistor being coupled to a first scanning signal line, a first electrode of the first switching transistor being coupled to a first reference signal line, and a second electrode of the first switching transistor being coupled to a second electrode of a drive transistor;

a second switching transistor, a gate electrode of the second switching transistor being coupled to a second scanning signal line, a first electrode of the second switching transistor being coupled to a second reference signal line, and a second electrode of the second switching transistor being coupled to a first

electrode of the drive transistor;

a third switching transistor, a gate electrode of the third switching transistor being coupled to a third scanning signal line, a first electrode of the third switching transistor being coupled to a third reference signal line, and a second electrode of the third switching transistor being coupled to a gate electrode of the drive transistor;

a fourth switching transistor, a gate electrode of the fourth switching transistor being coupled to a fourth scanning signal line, a first electrode of the fourth switching transistor being coupled to a data signal line, and a second electrode of the fourth switching transistor being coupled to the gate electrode of the drive transistor;

a fifth switching transistor, a gate electrode of the fifth switching transistor being coupled to a light emitting control signal line, a first electrode of the fifth switching transistor being respectively coupled to the second electrode of the drive transistor and the second electrode of the first switching transistor, and a second electrode of the fifth switching transistor being coupled to a first electrode of the light emitting device;

a storage capacitor, the storage capacitor being coupled between the gate electrode and the first electrode of the drive transistor;

and a voltage dividing capacitor, the voltage dividing capacitor being coupled between the first electrode of the drive transistor and the second reference signal line.

[0019] Alternatively, in some embodiments of the disclosure, materials of active layers of the first switching transistor, the third switching transistor and the fourth switching transistor include a metal oxide semiconductor material;

and materials of active layers of the second switching transistor, the fifth switching transistor and the drive transistor include a low temperature poly-silicon material.

[0020] Alternatively, in some embodiments of the disclosure, a signal of the first scanning signal line is the same as a signal of the third scanning signal line.

[0021] Alternatively, in some embodiments of the disclosure, a signal of the first reference signal line is the same as a signal of the third reference signal line.

[0022] Alternatively, in some embodiments of the disclosure, a signal of the light emitting control signal line is the same as a signal of the second scanning signal line.

[0023] Accordingly, some embodiments of the disclosure provides an electroluminescent light emitting display panel, including a pixel circuit, a data signal line, a first scanning signal line, a second scanning signal line, a third scanning signal line, a fourth scanning signal line, a light emitting control signal line, a first reference voltage line, a second reference voltage line and a third reference voltage line;

the pixel circuit includes a first switching transistor, a sec-

ond switching transistor, a third switching transistor, a fourth switching transistor, a fifth switching transistor, a drive transistor, a storage capacitor, a voltage dividing capacitor and a light emitting device; wherein

a gate electrode of the first switching transistor is coupled to the first scanning signal line applying the current corresponding signal to the gate electrode of the first switching transistor, a first electrode of the first switching transistor is coupled to the first reference signal line, and a second electrode of the first switching transistor is coupled to a second electrode of the drive transistor;

a gate electrode of the second switching transistor is coupled to the second scanning signal line applying the current corresponding signal to the gate electrode of the second switching transistor, a first electrode of the second switching transistor is coupled to the second reference signal line, and a second electrode of the second switching transistor is coupled to a first electrode of the drive transistor;

a gate electrode of the third switching transistor is coupled to the third scanning signal line applying the current corresponding signal to the gate electrode of the third switching transistor, a first electrode of the third switching transistor is coupled to the third reference signal line, and a second electrode of the third switching transistor is coupled to a gate electrode of the drive transistor;

a gate electrode of the fourth switching transistor is coupled to the fourth scanning signal line applying the current corresponding signal to the gate electrode of the fourth switching transistor, a first electrode of the fourth switching transistor is coupled to the data signal line applying the current corresponding signal to the first electrode of the fourth switching transistor, and a second electrode of the fourth switching transistor is coupled to the gate electrode of the drive transistor;

a gate electrode of the fifth switching transistor is coupled to the light emitting control signal line applying the current corresponding signal to the gate electrode of the fifth switching transistor, a first electrode of the fifth switching transistor is respectively coupled to the second electrode of the drive transistor and the second electrode of the first switching transistor, and a second electrode of the fifth switching transistor is coupled to a first electrode of the light emitting device;

the storage capacitor is coupled between the gate electrode and the first electrode of the drive transistor;

and the voltage dividing capacitor is coupled between the first electrode of the drive transistor and the second reference signal line.

[0024] Alternatively, in some embodiments of the disclosure, signals of the first scanning signal line and the third scanning signal line coupled to the same pixel circuit are the same.

[0025] Alternatively, in some embodiments of the disclosure, a signal of the first reference signal line is the same as a signal of the third reference signal line.

[0026] Alternatively, in some embodiments of the disclosure, signals of the light emitting control signal line

and the second scanning signal line coupled to the same pixel circuit are the same.

[0027] Alternatively, some embodiments of the disclosure provides a display apparatus including the electroluminescent light emitting display panel according to any one of claims 20-23.

[0028] Accordingly, some embodiments of the disclosure provides a drive method of the pixel circuit, including:

resetting the first electrode and the second electrode of the drive transistor by the reset circuit during a reset phase;

providing the data signal to the gate electrode of the drive transistor by the data write circuit during a data write phase;

and storing the voltage of the gate electrode of the drive transistor by the capacitance circuit, and generating the drive current by the drive transistor in order to drive the light emitting device to emit light during a light emitting phase.

[0029] Alternatively, in some embodiments of the disclosure, the method further includes: resetting the gate electrode of the drive transistor by the reset circuit during the reset phase;

and after the reset phase and before the data write phase, the method further includes: compensating the threshold voltage of the drive transistor by the reset circuit during a threshold compensation phase.

[0030] Alternatively, in some embodiments of the disclosure, during the reset phase, the first switching transistor in the reset circuit is controlled to be turned on and the signal of the first reference signal line is controlled to be provided to the second electrode of the drive transistor, the second switching transistor is controlled to be turned on and the signal of the second reference signal line is controlled to be provided to the first electrode of the drive transistor, the third switching transistor is controlled to be turned on and the signal of the third reference signal line is controlled to be provided to the gate electrode of the drive transistor;

and during the threshold compensation phase, the second switching transistor in the reset circuit is controlled to be turned off, the first switching transistor is controlled to be turned on and the signal of the first reference signal line is controlled to be provided to the second electrode of the drive transistor, the third switching transistor is controlled to be turned on and the signal of the third reference signal line is controlled to be provided to the gate electrode of the drive transistor; and the drive transistor is turned on to perform threshold compensation.

[0031] Alternatively, in some embodiments of the disclosure, the method further includes: turning on the second electrode of the drive transistor and the first electrode of the light emitting device by the light emitting control circuit during the reset phase and the light emitting phase.

BRIEF DESCRIPTION OF THE DRAWINGS

[0032]

Fig. 1 is a first structural schematic diagram of a pixel circuit provided by some embodiments of the disclosure;

Fig. 2 is a second structural schematic diagram of the pixel circuit provided by some embodiments of the disclosure;

Fig. 3a is a first specific structural schematic diagram of the pixel circuit provided by some embodiments of the disclosure;

Fig. 3b is a second specific structural schematic diagram of the pixel circuit provided by some embodiments of the disclosure;

Fig. 4a is a third specific structural schematic diagram of the pixel circuit provided by some embodiments of the disclosure;

Fig. 4b is a fourth specific structural schematic diagram of the pixel circuit provided by some embodiments of the disclosure;

Fig. 5a is a first circuit sequence diagram in some embodiments of the disclosure;

Fig. 5b is a second circuit sequence diagram in some embodiments of the disclosure;

Fig. 5c is a third circuit sequence diagram in some embodiments of the disclosure;

Fig. 5d is a fourth circuit sequence diagram in some embodiments of the disclosure;

Fig. 6 is a flow diagram of a drive method provided by some embodiments of the disclosure;

Fig. 7 is a first structural schematic diagram of an electroluminescent light emitting display panel provided by some embodiments of the disclosure;

Fig. 8 is a second structural schematic diagram of the electroluminescent light emitting display panel provided by some embodiments of the disclosure.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0033] In order to make the objects, technical solutions and advantages of the disclosure clearer, detailed descriptions of a pixel circuit, a drive method, an electroluminescent light emitting display panel, and a display apparatus provided by some embodiments of the disclosure are explained in detail below in combination with accompanying drawings. It should be understood that the preferred embodiments described below merely intend to describe and explain the disclosure, rather than to limit the disclosure. Moreover, the embodiments in the application and features in the embodiments may be combined with each other under the condition that no conflicts exist.

[0034] Some embodiments of the disclosure provide a pixel circuit, as shown in Fig. 1, including:

a light emitting device L;

a drive transistor M0, configured to generate a drive current during a light emitting phase in order to drive the light emitting device L to emit light; wherein a gate electrode G of the drive transistor M0 is respectively coupled to a capacitance circuit 3 and a data write circuit 2, a first electrode S of the drive transistor M0 is coupled to a reset circuit 1, and a second electrode D of the drive transistor M0 is respectively coupled to the reset circuit 1 and a first electrode of the light emitting device L;

the capacitance circuit 3, configured to store the voltage of the gate electrode G of the drive transistor M0;

the data write circuit 2, configured to provide a data signal (Data) to the gate electrode G of the drive transistor M0 during a data write phase;

and the reset circuit 1, configured to reset the first electrode S and the second electrode D of the drive transistor M0 during a reset phase.

[0035] According to the pixel circuit provided by some embodiments of the disclosure, the first electrode and the second electrode of the drive transistor may be reset by the reset circuit during the reset phase, then, the data signal may be written into the gate electrode of the drive transistor by the data write circuit, and the drive current is generated by the drive transistor in order to drive the light emitting device to emit light. Thus, the voltage of the first electrode of the drive transistor may be set as a fixed voltage before the data signal is written every time, and the voltage of the second electrode of the drive transistor may be set as the fixed voltage, so that influences of the residual voltage of the previous frame on the light emission of the frame may be avoided, and furthermore, the light emitting uniformity of the display panel may be improved.

[0036] The characteristics such as the threshold voltage and migration rate of the drive transistor may be offset due to the action of a bias stress after the drive transistor drives the light emitting device to emit light for a period of time under a certain gray level. However, bias stresses generated when the drive transistor drives the light emitting device to emit light under different gray levels are different to result in different offsets of the characteristics of the drive transistor under different gray levels, and thus, a short-term residual image problem may appear due to a hysteresis effect during high and low gray level switched display. During specific implementation, in the pixel circuit provided by some embodiments of the disclosure, as shown in Fig. 2, the reset circuit 1 is further coupled to the gate electrode G of the drive transistor M0, is configured to reset the gate electrode G of the drive transistor M0 during the reset phase and is configured to compensate the threshold voltage of the drive transistor M0 during a threshold compensation phase. Thus, before the data signal of each frame is written, the voltage of the gate electrode G of the drive transistor M0 is reset, namely the voltage of the gate electrode G becomes a fixed voltage, in addition, the voltage

of the first electrode S of the drive transistor M0 becomes a fixed voltage, the voltage of the second electrode D of the drive transistor M0 becomes a fixed voltage, when the data signal Data is written every time, the gate electrode G of the drive transistor M0 is jumped by the same voltage, and the voltage of the first electrode S of the drive transistor M0 is jumped by the same voltage, so that the short-term residual image problem caused by the hysteresis effect may be relieved.

[0037] The disclosure is described in detail below in combination with a specific embodiment. It should be explained that some embodiments intend to better explain the disclosure, rather than to limit the disclosure.

[0038] A transistor with an active layer made of a low temperature poly-silicon (LTPS) material is high in migration rate and may be made thinner and smaller as well as lower in power consumption, and during specific implementation, the material of the active layer of the drive transistor may include the low temperature poly-silicon material.

[0039] Alternatively, during specific implementation, in the pixel circuit provided by some embodiments of the disclosure, as shown in Fig. 1 to Fig. 4b, the drive transistor M0 may be a P-type transistor; wherein the first electrode S of the drive transistor M0 is used as a source electrode of the drive transistor M0, and the second electrode D of the drive transistor M0 is used as a drain electrode of the drive transistor M0. Moreover, the current flows from the source electrode to the drain electrode of the drive transistor M0 when the drive transistor M0 is in a saturated state.

[0040] During specific implementation, in the pixel circuit provided by some embodiments of the disclosure, as shown in Fig. 1 to Fig. 4b, the second electrode of the light emitting device L is coupled to a low voltage power source terminal (ELVSS). The voltage of the low voltage power source terminal ELVSS is generally grounded or is a negative value, and the specific voltage value of the low voltage power source terminal ELVSS needs to be designed and determined according to an actual application environment, but is not limited herein.

[0041] During specific implementation, in the pixel circuit provided by some embodiments of the disclosure, the light emitting device may be an electroluminescent light emitting diode, wherein the anode of the electroluminescent light emitting diode is the first electrode of the light emitting device, and the cathode of the electroluminescent light emitting diode is the second electrode of the light emitting device, moreover, the light emitting device achieves light emission under the action of the current generated when the drive transistor is in the saturated state. In addition, a common light emitting device has a light emitting threshold voltage VL and emits light when the voltage difference of two electrodes of the light emitting device is greater than or equal to the light emitting threshold voltage VL. Wherein the electroluminescent light emitting diode may include an organic light emitting diode or a quantum dot light emitting diode which

are not limited herein.

[0042] During specific implementation, in the pixel circuit provided by some embodiments of the disclosure, as shown in Fig. 3a to Fig. 4b, the data write circuit 2 may include a fourth switching transistor M4; wherein a gate electrode of the fourth switching transistor M4 is coupled to a fourth scanning signal line (Scan4), a first electrode of the fourth switching transistor M4 is coupled to a data signal line (DATA) for receiving a data signal, and a second electrode of the fourth switching transistor M4 is coupled to the gate electrode G of the drive transistor M0.

[0043] During specific implementation, in the pixel circuit provided by some embodiments of the disclosure, the fourth switching transistor is in a turn-on state under the control of a signal of the fourth scanning signal line during the data write phase, so that the data signal of the data signal line may be written into the gate electrode of the drive transistor.

[0044] The leakage current of a transistor with an active layer made of a metal oxide semiconductor material is generally relatively small, in order to reduce the leakage current, during specific implementation, in the pixel circuit provided by some embodiments of the disclosure, the material of the active layer of the fourth switching transistor may include the metal oxide semiconductor material such as IGZO (Indium Gallium Zinc Oxide), of course, the material of the active layer of the fourth switching transistor may also be other metal oxide semiconductor materials which are not limited herein. Thus, a leakage current generated when the fourth switching transistor M4 is turned off may be reduced, so that the disturbance of the leakage current of the fourth switching transistor M4 to the drive transistor M0 may be favorably reduced when the light emitting device L emits light, and furthermore, the drive current, for driving the light emitting device to emit light, of the drive transistor M0 may be prevented from being affected.

[0045] The specific structure of the data write circuit in the pixel circuit provided by some embodiments of the disclosure is merely illustrated, and during specific implementation, the specific structure of the data write circuit is not limited to the structure provided by some embodiments of the disclosure, may also be other structures known by the skilled in the art, but is not limited herein.

[0046] During specific implementation, in the pixel circuit provided by some embodiments of the disclosure, as shown in Fig. 3a to Fig. 4b, the reset circuit 1 may include a first switching transistor M1, a second switching transistor M2 and a third switching transistor M3.

[0047] A gate electrode of the first switching transistor M1 is coupled to a first scanning signal line (Scan1), a first electrode of the first switching transistor M1 is coupled to a first reference signal line (Vref1), and a second electrode of the first switching transistor M1 is coupled to the second electrode D of the drive transistor M0.

[0048] A gate electrode of the second switching transistor M2 is coupled to a second scanning signal line (Scan2), a first electrode of the second switching tran-

sistor M2 is coupled to a second reference signal line (Vref2), and a second electrode of the second switching transistor M2 is coupled to the first electrode S of the drive transistor M0.

[0049] A gate electrode of the third switching transistor M3 is coupled to a third scanning signal line (Scan3), a first electrode of the third switching transistor M3 is coupled to a third reference signal line (Vref3), and a second electrode of the third switching transistor M3 is coupled to the gate electrode G of the drive transistor M0.

[0050] During specific implementation, in the pixel circuit provided by some embodiments of the disclosure, the first switching transistor is in a turn-on state under the control of a signal of the first scanning signal line during the reset phase, so that a signal of the first reference signal line may be provided to the second electrode of the drive transistor, and furthermore, the second electrode of the drive transistor is reset during the reset phase. The second switching transistor is in a turn-on state under the control of a signal of the second scanning signal line during the reset phase, so that a signal of the second reference signal line may be provided to the first electrode of the drive transistor, and furthermore, the first electrode of the drive transistor is reset during the reset phase. The third switching transistor is in a turn-on state under the control of a signal of the third scanning signal line during the reset phase, so that a signal of the third reference signal line may be provided to the gate electrode of the drive transistor, and furthermore, the gate electrode of the drive transistor is reset during the reset phase. The third switching transistor is in a turn-on state under the control of the signal of the third scanning signal line during the threshold compensation phase, so that the signal of the third reference signal line may be provided to the gate electrode of the drive transistor; the first switching transistor is in a turn-on state under the control of the signal of the first scanning signal line during the threshold compensation phase, so that the signal of the first reference signal line may be provided to the second electrode of the drive transistor; and the drive transistor is turned on during the threshold compensation phase so as to realize threshold compensation.

[0051] During specific implementation, in the pixel circuit provided by some embodiments of the disclosure, a material of an active layer of the first switching transistor may include a metal oxide semiconductor. Thus, a leakage current generated when the first switching transistor is turned off may be reduced, so that the disturbance of the leakage current of the first switching transistor to the drive transistor may be favorably reduced when the light emitting device emits light, and furthermore, the drive current, for driving the light emitting device to emit light, of the drive transistor may be prevented from being affected.

[0052] During specific implementation, in the pixel circuit provided by some embodiments of the disclosure, a material of an active layer of the third switching transistor may include a metal oxide semiconductor material. Thus,

a leakage current generated when the third switching transistor is turned off may be reduced, so that the disturbance of the leakage current of the third switching transistor to the drive transistor may be favorably reduced when the light emitting device emits light, and furthermore, the drive current, for driving the light emitting device to emit light, of the drive transistor may be prevented from being affected.

[0053] During specific implementation, in the pixel circuit provided by some embodiments of the disclosure, a material of an active layer of the second switching transistor may include low-temperature poly-silicon material, and thus, the second switching transistor may be high in migration rate and may be made thinner and smaller as well as lower in power consumption.

[0054] In order to reduce the arrangement and number of the signal lines and save the line arrangement space, during specific implementation, in the pixel circuit provided by some embodiments of the disclosure, the signals of the first reference signal line and the third reference signal line may be set to be the same. Alternatively, the first reference signal line and the third reference signal line are enabled to be set as the same signal line. Optionally, as shown in Fig. 3b and Fig. 4b, both the first electrode of the first switching transistor M1 and the first electrode of the third switching transistor M3 may be coupled to the first reference signal line Vref1. Of course, both the first electrode of the first switching transistor and the first electrode of the third switching transistor may also be coupled to the third reference signal line, there are no limits herein.

[0055] In order to reduce the arrangement and number of the signal lines and save the line arrangement space, during specific implementation, in the pixel circuit provided by some embodiments of the disclosure, the signals of the first scanning signal line and the third scanning signal line may be set to be the same. Alternatively, the first scanning signal line and the third scanning signal line are enabled to be set as the same signal line. Optionally, as shown in Fig. 3b and Fig. 4b, both the gate electrode of the first switching transistor M1 and the gate electrode of the third switching transistor M3 may be coupled to the first scanning signal line Scan1, at the moment, the first switching transistor M1 and the third switching transistor M3 are the same type of transistor, namely an N-type transistor, there are no limits herein. Of course, both the gate electrode of the first switching transistor and the gate electrode of the third switching transistor may also be coupled to the third scanning signal line, there are no limits herein.

[0056] In order to reduce the arrangement and number of the signal lines and save the line arrangement space, during specific implementation, in the pixel circuit provided by some embodiments of the disclosure, the signals of the first scanning signal line and the third scanning signal line are set to be the same, and the signal of the first reference signal line and the signal of the third reference signal line are set to be the same. Specifically,

as shown in Fig. 3b and Fig. 4b, both the first electrode of the first switching transistor M1 and the first electrode of the third switching transistor M3 may be coupled to the first reference signal line Vref1, and both the gate electrode of the first switching transistor M1 and the gate electrode of the third switching transistor M3 may also be coupled to the first scanning signal line Scan1.

[0057] During specific implementation, in the pixel circuit provided by some embodiments of the disclosure, a voltage Vref2 of the signal of the second reference signal line is generally a positive value, for example, the signal of the second reference signal line may be a signal of a high voltage power source terminal ELVDD. A voltage Vref1 of the signal of the first reference signal line is preferably a negative value, and a voltage Vref3 of the signal of the third reference signal line is generally a negative value, wherein the voltage Vref1 of the first reference signal line and a voltage Vss of the low voltage power source terminal generally meet a formula: $V_{ref1} - V_{ss} < V_L$. Moreover, the specific voltage value of the signal of the signal line needs to be designed and determined according to an actual application environment, but is not limited herein.

[0058] The specific structure of the reset circuit in the pixel circuit provided by some embodiments of the disclosure is merely illustrated, and during specific implementation, the specific structure of the reset circuit is not limited to the structure provided by some embodiments of the disclosure, may also be other structures known by the skilled in the art, but is not limited herein.

[0059] During specific implementation, in the pixel circuit provided by some embodiments of the disclosure, as shown in Fig. 3a to Fig. 4b, the capacitance circuit 3 may include a storage capacitor C1 and a voltage dividing capacitor C2:

the storage capacitor C1 is coupled between the gate electrode G and the first electrode S of the drive transistor M0;
and the voltage dividing capacitor C2 is coupled between the first electrode S of the drive transistor M0 and the second reference signal line Vref2.

[0060] During specific implementation, in the pixel circuit provided by some embodiments of the disclosure, the storage capacitor may keep the voltages of the gate electrode and the first electrode of the drive transistor stable, may charge or discharge under the actions of signals input to the gate electrode and the first electrode of the drive transistor and may also couple a variable voltage difference of the gate electrode of the drive transistor to the first electrode of the drive transistor when the first electrode of the drive transistor is in a floating state.

[0061] The specific structure of the capacitance circuit in the pixel circuit provided by some embodiments of the disclosure is merely illustrated, and during specific implementation, the specific structure of the capacitance circuit is not limited to the structure provided by some

embodiments of the disclosure, may also be other structures known by the skilled in the art, but is not limited herein.

[0062] In order to avoid affecting performances of the light emitting device during the threshold compensation phase, during specific implementation, in the pixel circuit provided by some embodiments of the disclosure, as shown in Fig. 2, the pixel circuit may further include a light emitting control circuit 4; the second electrode D of the drive transistor M0 and the reset circuit 1 are respectively coupled to the first electrode of the light emitting device L by the light emitting control circuit 4; wherein the light emitting control circuit 4 is configured to control the second electrode D of the drive transistor M0 and the first electrode of the light emitting device L to be turned on or off. Thus, the light emitting device L may be reset during the reset phase, and the drive current generated by the drive transistor M0 may flow to the light emitting device L during the light emitting phase in order to drive the light emitting device L to emit light.

[0063] During specific implementation, in the pixel circuit provided by some embodiments of the disclosure, as shown in Fig. 4a and Fig. 4b, the light emitting control circuit 4 may include a fifth switching transistor M5; a gate electrode of the fifth switching transistor M5 is coupled to a light emitting control signal line (EMIT), a first electrode of the fifth switching transistor M5 is respectively coupled to the second electrode D of the drive transistor M0 and the first electrode of the first switching transistor, and a second electrode of the fifth switching transistor M5 is coupled to the first electrode of the light emitting device L.

[0064] During specific implementation, in the pixel circuit provided by some embodiments of the disclosure, the fifth switching transistor may be in a turn-on state under the control of a signal of the light emitting control signal line during the reset phase, so that the second electrode of the drive transistor and the first electrode of the light emitting device are turned on, and furthermore, the light emitting device is reset. The fifth switching transistor may be in a turn-on state under the control of the signal of the light emitting control signal line during the light emitting phase, so that the second electrode of the drive transistor and the first electrode of the light emitting device are turned on, and furthermore, the drive current generated by the drive transistor is output to the light emitting device so as to drive the light emitting device to emit light.

[0065] During specific implementation, in the pixel circuit provided by some embodiments of the disclosure, a material of an active layer of the fifth switching transistor may include a low temperature poly-silicon material, so that the fifth switching transistor may be made thinner and smaller as well as lower in power consumption.

[0066] In order to further reduce the arrangement and number of the signal lines and save the line arrangement space, during specific implementation, in the pixel circuit provided by some embodiments of the disclosure, the

signal of the light emitting control signal line and the signal of the second scanning signal line may be set to be the same. Alternatively, the light emitting control signal line and the second scanning signal line are set as the same signal line. Optionally, as shown in Fig. 4b, both the gate electrode of the second switching transistor M2 and the gate electrode of the fifth switching transistor M5 may be coupled to the light emitting control signal line EMIT. Of course, the gate electrode of the second switching transistor and the gate electrode of the fifth switching transistor may also be coupled to the second scanning signal line, there are no limits herein.

[0067] The specific structure of the light emitting control circuit in the pixel circuit provided by some embodiments of the disclosure is merely illustrated, and during specific implementation, the specific structure of the light emitting control circuit is not limited to the structure provided by some embodiments of the disclosure, may also be other structures known by the skilled in the art, but is not limited herein.

[0068] Generally, the active layer may be subjected to ion doping by adopting a doping process when the metal oxide semiconductor material or the low temperature poly-silicon material is adopted as the active layer, so that the type of the formed transistor is P-type or N-type. During specific implementation, in the pixel circuit provided by some embodiments of the disclosure, each of the switching transistors may be set as a P-type transistor or an N-type transistor according to an actual application environment, there are no limits herein.

[0069] Alternatively, during specific implementation, in the pixel circuit provided by some embodiments of the disclosure, as shown in Fig. 3a to Fig. 4b, the first switching transistor M1, the third switching transistor M3 and the fourth switching transistor M4 may be set as the N-type transistor, and the second switching transistor M2 and the fifth switching transistor may be set as the P-type transistor.

[0070] In order to further reduce the leakage current, the switching transistors may adopt double-gate structures. During specific implementation, the first switching transistor, the third switching transistor and the fourth switching transistor may be preferably set to be of the double-gate structures. Thus, the disturbance to the drive transistor may be reduced when the light emitting device emits light, and furthermore, the drive current, for driving the light emitting device to emit light, of the drive transistor may be prevented from being affected. Moreover, in the pixel circuit provided by some embodiments of the disclosure, any switching transistor may be set to be of the double-gate structure in view of reducing the leakage current, there are no limits herein.

[0071] Optionally, in the pixel circuit provided by some embodiments of the disclosure, the P-type transistor is turned on under the action of a low-potential signal and is turned off under the action of a high-potential signal; and the N-type transistor is turned on under the action of a high-potential signal and is turned off under the action

of a low-potential signal.

[0072] Optionally, in the pixel circuit provided by some embodiments of the disclosure, the first electrode of each of the switching transistors may be used as a source electrode of the switching transistor, and the second electrode of each of the switching transistors may be used as a drain electrode of the switching transistor, or the first electrode of each of the switching transistors may be used as the drain electrode of the switching transistor, and the second electrode of each of the switching transistors may be used as the source electrode of the switching transistor, there are no specific differences herein.

[0073] Further, during specific implementation, in the pixel circuit provided by some embodiments of the disclosure, the materials of the active layers of all the first switching transistor, the third switching transistor and the fourth switching transistor may be set as the metal oxide semiconductor material, namely all the first switching transistor, the third switching transistor and the fourth switching transistor are set as oxide thin film transistors, and thus, the leakage currents of the first switching transistor, the third switching transistor and the fourth switching transistor may be relatively small. Moreover, a process for preparing the transistors by taking the metal oxide semiconductor material as the active layers may be the same as a process for preparing the oxide thin film transistors in the prior art, the descriptions thereof are omitted herein. The materials of the active layers of the second switching transistor, the fifth switching transistor and the drive transistor are set as the low temperature poly-silicon material, namely all the drive transistor, the second switching transistor and the fifth switching transistor are set as LTPS-type transistors, and thus, the second switching transistor, the fifth switching transistor and the drive transistor are relatively high in migration rate and may be made thinner and smaller as well as lower in power consumption. Moreover, a process for preparing the transistors by taking the low temperature poly-silicon as the active layers may be the same as a process for preparing the LTPS-type transistors in the prior art, the descriptions thereof are omitted herein. Thus, an LTPO pixel circuit is prepared by combining the two processes for preparing the transistors including the LTPS-type transistors and the oxide thin film transistors, so that the leakage current of the gate electrode of the drive transistor may be relatively small, and the power consumption may be relatively low. Therefore, if the pixel circuit is configured to be applied to an electroluminescent light emitting display panel, the display uniformity may be guaranteed when the display panel performs display by reducing the refresh frequency.

[0074] The working process of the pixel circuit provided by some embodiments of the disclosure is described below in combination with a circuit sequence diagram. In the description, 1 represents for a high potential, and 0 represents for a low potential. It should be explained that 1 and 0 are logic potentials which merely intend to better explain the specific working process of some embodi-

ments of the disclosure instead of a specific voltage value.

[0075] In some embodiments, with the pixel circuit as shown in Fig. 3b as an example, a corresponding input sequence diagram is shown as Fig. 5a. Optionally, total three phases including a reset phase T1, a data write phase T2 and a light emitting phase T3 in the input sequence diagram as shown in Fig. 5a are mainly selected.

[0076] During the reset phase T1, a first scanning signal Scan1 is equal to 1, a second scanning signal Scan2 is equal to 0, and a fourth scanning signal Scan4 is equal to 0.

[0077] Since Scan1 is equal to 1, both the first switching transistor M1 and the third switching transistor M3 are turned on. The turn-on first switching transistor M1 provides the signal of the first reference signal line Vref1 to the second electrode D of the drive transistor M0, so that the second electrode D of the drive transistor M0 and the light emitting device L are reset, and furthermore, light emitting disturbance between two adjacent display frames is avoided. The turn-on third switching transistor M3 provides the signal of the first reference signal line Vref1 to the gate electrode G of the drive transistor M0, so that the gate electrode G of the drive transistor M0 is reset. Since Scan2 is equal to 0, the second switching transistor M2 is turned on to provide the signal of the second reference signal line Vref2 to the first electrode S of the drive transistor M0, so that the first electrode S of the drive transistor M0 is reset. Of course, the third switching transistor M3 may not be arranged when the reset circuit only resets the first electrode S and the second electrode D of the drive transistor M0. Since Scan4 is equal to 0, the fourth switching transistor M4 is turned off.

[0078] During the data write phase T2, Scan1 is equal to 0, Scan2 is equal to 1, and Scan4 is equal to 1.

[0079] Since Scan4 is equal to 1, the fourth switching transistor M4 is turned on to write the data signal of the data signal line DATA into the gate electrode G of the drive transistor M0, so that the voltage of the gate electrode G of the drive transistor M0 is a voltage Vdata of the data signal and is stored by the storage capacitor C1. Since Scan1 is equal to 0, both the first switching transistor M1 and the third switching transistor M3 are turned off. Since Scan2 is equal to 1, the second switching transistor M2 is turned off.

[0080] During the light emitting phase T3, Scan1 is equal to 0, Scan2 is equal to 0, and Scan4 is equal to 0.

[0081] Since Scan2 is equal to 0, the second switching transistor M2 is turned on to provide the signal of the second reference signal line Vref2 to the first electrode S of the drive transistor M0, so that the voltage of the first electrode S of the drive transistor M0 is Vref2. The drive transistor M0 generates the drive current IL under the control of the voltage Vref2 of the first electrode S and the voltage Vdata of the gate electrode G of the drive transistor M0, and $I_L = K[V_{data} - V_{ref2} - V_{th}]^2$, so that the drive

current IL drives the light emitting device L to emit light. Moreover, Vth is the threshold voltage of the drive transistor M0, K is a structural parameter, and

$$K = \frac{1}{2} \mu_n C_{ox} \frac{W}{L}$$

, μ_n represents for the migration rate of the drive transistor M0, Cox is the capacitance of a gate

oxide layer on a unit area, $\frac{W}{L}$ is the width-to-length ratio of the drive transistor M0, and the numerical values in the same structure are relatively stable and may be regarded as constants.

[0082] The first electrode and the second electrode of the drive transistor are reset during the reset phase, the data signal is written into the gate electrode of the drive transistor during the data write phase, and the drive transistor drives the light emitting device to emit light during the light emitting phase. Thus, the voltage of the first electrode of the drive transistor may be set as the fixed voltage before the data signal is written every time, and the voltage of the second electrode of the drive transistor may be set as the fixed voltage, so that influences of the residual voltage of the previous frame on the light emission of the frame may be avoided, and furthermore, the light emitting uniformity of the display panel may be improved.

[0083] The threshold voltage Vth of the drive transistor may drift due to technological processes and device aging, and thus, the drive current flowing through each light emitting device is affected by the drifting of Vth to change to result in display brightness non-uniformity, and furthermore, the display effect of the whole image is affected. Moreover, the drive current flowing through each light emitting device is related to the voltage Vref2 of the second reference signal line connected with the first electrode of the drive transistor, so that the drive current is further affected by the IR Drop of the second reference signal line to result in the phenomenon of brightness non-uniformity of the light emitting devices in different regions.

[0084] The specific implementation way for relieving the influences of the threshold voltage Vth of the drive transistor and IR Drop is described below by some embodiments. However, a reader should know that the specific implementation way is not limited herein.

[0085] In some other embodiments, with the pixel circuit as shown in Fig. 3b as an example, the working process of the pixel circuit is described, and an input sequence diagram corresponding to the pixel circuit is shown as Fig. 5b. Optionally, total four phases including a reset phase T1, a threshold compensation phase T2, a data write phase T3 and a light emitting phase T4 in the input sequence diagram as shown in Fig. 5b are mainly selected.

[0086] During the reset phase T1, Scan1 is equal to 1, Scan2 is equal to 0, and Scan4 is equal to 0.

[0087] Since Scan1 is equal to 1, both the first switching transistor M1 and the third switching transistor M3 are turned on. The turn-on first switching transistor M1

provides the signal of the first reference signal line Vref1 to the second electrode D of the drive transistor M0, so that the second electrode D of the drive transistor M0 and the light emitting device L are reset, and furthermore, light emitting disturbance between two adjacent display frames is avoided. The turn-on third switching transistor M3 provides the signal of the first reference signal line Vref1 to the gate electrode G of the drive transistor M0, so that the gate electrode G of the drive transistor M0 is reset. Since Scan2 is equal to 0, the second switching transistor M2 is turned on and provides the signal of the second reference signal line Vref2 to the first electrode S of the drive transistor M0, so that the first electrode S of the drive transistor M0 is reset, and the voltage Vref2 of the signal of the second reference signal line Vref2 is stored by the storage capacitor C1. Since Scan4 is equal to 0, the fourth switching transistor M4 is turned off.

[0088] During the threshold compensation phase T2, Scan1 is equal to 1, Scan2 is equal to 1, and Scan4 is equal to 0.

[0089] Since Scan1 is equal to 1, both the first switching transistor M1 and the third switching transistor M3 are turned on. The turn-on third switching transistor M3 provides the signal of the first reference signal line Vref1 to the gate electrode of the drive transistor M0, so that the voltage of the gate electrode of the drive transistor M0 is Vref1. The turn-on first switching transistor M1 provides the signal of the first reference signal line Vref1 to the second electrode D of the drive transistor M0, so that the voltage of the second electrode D of the drive transistor M0 is Vref1. Since Scan2 is equal to 1, the second switching transistor M2 is turned off. The storage capacitor C1 is capable of instantly keeping the voltage Vref2 of the first electrode of the drive transistor M0, so that the drive transistor M0 is turned on under the actions of Vref1 and Vref2, and furthermore, the voltage of the first electrode S of the drive transistor M0 is discharged by the turn-on drive transistor M0 until the voltage of the first electrode S of the drive transistor M0 becomes $V_{ref1} - V_{th}$, at the moment, the drive transistor M0 is turned off, the threshold voltage Vth of the drive transistor M0 is written into the storage capacitor C1. Therefore, the compensation of the threshold voltage Vth of the drive transistor M0 is realized, and the compensation process may not affect the light emitting device L. Since Scan4 is equal to 0, the fourth switching transistor M4 is turned off.

[0090] During the data write phase T3, Scan1 is equal to 0, Scan2 is equal to 1, and Scan4 is equal to 1.

[0091] Since Scan4 is equal to 1, the fourth switching transistor M4 is turned on to provide the voltage Vdata of the data signal to the gate electrode G of the drive transistor M0, so that the voltage of the gate electrode G of the drive transistor M0 becomes Vdata. Since Scan2 is equal to 1, the second switching transistor M2 is turned off. Therefore, the first electrode S of the drive transistor M0 is in a floating state; due to the coupling effect of the storage capacitor C1 and the voltage dividing effect of the voltage dividing capacitor C2, the voltage of the first

electrode S of the drive transistor M0 may become

$$(V_{data} - V_{ref1}) \frac{c_1}{c_1 + c_2} + V_{ref1} - V_{th};$$

wherein c1 represents for a capacitance value of the storage capacitor C1, and c2 represents for a capacitance value of the voltage dividing capacitor C2. Since Scan1 is equal to 0, both the first switching transistor M1 and the third switching transistor M3 are turned off.

[0092] During the light emitting phase T4, Scan1 is equal to 0, Scan2 is equal to 0, and Scan4 is equal to 0.

[0093] Since Scan2 is equal to 0, the second switching transistor M2 is turned on and provides the voltage Vref2 of the second reference signal line Vref2 to the first electrode S of the drive transistor M0, so that the voltage of the first electrode S of the drive transistor M0 is Vref2. The voltage of the gate electrode G of the drive transistor

M0 becomes $(V_{data} - V_{ref1}) \frac{c_2}{c_1 + c_2} + V_{ref2} + V_{th}$ according to a charge conservation principle of charges of the storage capacitor C before and after jumping. Therefore, the drive transistor M0 is in a saturated state, and the drive transistor M0 generates the drive current IL for driving the light emitting device L to emit light according to the characteristics of the current in the saturated state, IL meets a formula:

$$I_L = K[V_{gs} - V_{th}]^2 = K[(V_{data} - V_{ref1}) \frac{c_2}{c_1 + c_2}]^2;$$

wherein Vgs is a gate-source voltage of the drive transistor M0, namely

$$V_{gs} = (V_{data} - V_{ref1}) \frac{c_2}{c_1 + c_2} + V_{ref2} + V_{th} - V_{ref2}.$$

Moreover, K is a structural parameter, and

$$K = \frac{1}{2} \mu_n C_{ox} \frac{W}{L},$$

μ_n represents for the migration rate of the drive transistor M0, Cox is the capacitance of a

gate oxide layer on a unit area, $\frac{W}{L}$ is the width-to-length ratio of the drive transistor M0, and the numerical values in the same structure are relatively stable and may be regarded as constants. The drive current IL generated by the drive transistor M0 is provided to the light emitting device L in order to drive the light emitting device L to emit light. Known from the formula that the drive current IL meets, the drive current IL, for driving the light emitting device L to emit light, of the drive transistor M0 is only related to the voltage Vdata of the data signal Data and the voltage Vref1 of the first reference signal line Vref1, but is unrelated to the threshold voltage Vth of the drive transistor M0 and the voltage Vref2 of the second reference signal line Vref2, and influences of threshold voltage Vth drifting and IR Drop caused by the technological

processes and long-term operation of the drive transistor M0 on the drive current IL for driving the light emitting device L may be overcome, so that the drive current IL for the light emitting device L is kept stable, and furthermore, the normal work of the light emitting device L is guaranteed.

[0094] The working process of the pixel circuit as shown in Fig. 3a may refer to that of the pixel circuit as shown in Fig. 3b, the descriptions thereof are omitted herein.

[0095] In some other embodiments, with the pixel circuit as shown in Fig. 4a as an example, the working process of the pixel circuit is described, and an input sequence diagram corresponding to the pixel circuit is shown as Fig. 5c. Optionally, total four phases including a reset phase T1, a threshold compensation phase T2, a data write phase T3 and a light emitting phase T4 in the input sequence diagram as shown in Fig. 5c are mainly selected.

[0096] During the reset phase T1, Scan1 is equal to 1, Scan2 is equal to 0, the third scanning signal Scan3 is equal to 0, Scan4 is equal to 0, and a light emitting control signal EM is equal to 0.

[0097] Since Scan1 is equal to 1, the first switching transistor M1 is turned on and provides the signal of the first reference signal line Vref1 to the second electrode D of the drive transistor M0, so that the second electrode D of the drive transistor M0 is set. Since Scan2 is equal to 0, the second switching transistor M2 is turned on and provides the signal of the second reference signal line Vref2 to the first electrode S of the drive transistor M0, so that the first electrode S of the drive transistor M0 is reset, and the voltage Vref2 of the signal of the second reference signal line Vref2 is stored by the storage capacitor C1. Since EM is equal to 0, the fifth switching transistor M5 is turned on, and the second electrode D of the drive transistor M0 and the first electrode of the light emitting device L are turned on, so that the signal of the first reference signal line Vref1 is provided to the light emitting device L, and the light emitting device L is reset, and furthermore, light emitting disturbance between two adjacent display frames is avoided. Since Scan4 is equal to 0, the fourth switching transistor M4 is turned off. Since Scan3 is equal to 0, the third switching transistor M3 is turned off.

[0098] During the threshold compensation phase T2, Scan1 is equal to 1, Scan2 is equal to 1, Scan3 is equal to 1, Scan4 is equal to 0, and EM is equal to 1.

[0099] Since Scan3 is equal to 1, the third switching transistor M3 is turned on and provides the signal of the third reference signal line Vref3 to the gate electrode G of the drive transistor M0, so that the voltage of the gate electrode of the drive transistor M0 is Vref3. Since Scan1 is equal to 1, the first switching transistor M1 is turned on and provides the signal of the first reference signal line Vref1 to the second electrode D of the drive transistor M0, so that the voltage of the second electrode D of the drive transistor M0 is Vref1. Since Scan2 is equal to 1,

the second switching transistor M2 is turned off. Since EM is equal to 1, the fifth switching transistor M5 is turned off. The storage capacitor C1 is capable of instantly keeping the voltage Vref2 of the first electrode of the drive transistor M0, so that the drive transistor M0 is turned on under the actions of Vref3 and Vref2, and furthermore, the voltage of the first electrode S of the drive transistor M0 is discharged by the turn-on drive transistor M0 until the voltage of the first electrode S of the drive transistor M0 becomes $V_{\text{ref3}} - V_{\text{th}}$, at the moment, the drive transistor M0 is turned off, the threshold voltage Vth of the drive transistor M0 is written into the storage capacitor C1. Therefore, the compensation of the threshold voltage Vth of the drive transistor M0 is realized, and the compensation process may not affect the light emitting device L. Since Scan4 is equal to 0, the fourth switching transistor M4 is turned off.

[0100] During the data write phase T3, Scan1 is equal to 0, Scan2 is equal to 1, Scan3 is equal to 0, Scan4 is equal to 1, and EM is equal to 1.

[0101] Since Scan4 is equal to 1, the fourth switching transistor M4 is turned on to provide the voltage Vdata of the data signal to the gate electrode G of the drive transistor M0, so that the voltage of the gate electrode G of the drive transistor M0 becomes Vdata. Since Scan2 is equal to 1, the second switching transistor M2 is turned off. Since Scan3 is equal to 0, the third switching transistor M3 is turned off. Therefore, the first electrode S of the drive transistor M0 is in a floating state; due to the coupling effect of the storage capacitor C1 and the voltage dividing effect of the voltage dividing capacitor C2, the voltage of the first electrode S of the drive transistor

$$(V_{\text{data}} - V_{\text{ref3}}) \frac{c_1}{c_1 + c_2} + V_{\text{ref3}} - V_{\text{th}}$$

M0 may become $(V_{\text{data}} - V_{\text{ref3}}) \frac{c_1}{c_1 + c_2} + V_{\text{ref3}} - V_{\text{th}}$; where-
in c1 represents for a capacitance value of the storage capacitor C1, and c2 represents for a capacitance value of the voltage dividing capacitor C2. Since Scan1 is equal to 0, the first switching transistor M1 is turned off. Since EM is equal to 1, the fifth switching transistor M5 is turned off.

[0102] During the light emitting phase T4, Scan1 is equal to 0, Scan2 is equal to 0, Scan3 is equal to 0, Scan4 is equal to 0, and EM is equal to 0.

[0103] Since Scan2 is equal to 0, the second switching transistor M2 is turned on and provides the voltage Vref2 of the second reference signal line Vref2 to the first electrode S of the drive transistor M0, so that the voltage of the first electrode S of the drive transistor M0 is Vref2. The voltage of the gate electrode G of the drive transistor

$$(V_{\text{data}} - V_{\text{ref3}}) \frac{c_2}{c_1 + c_2} + V_{\text{ref2}} + V_{\text{th}}$$

M0 becomes $(V_{\text{data}} - V_{\text{ref3}}) \frac{c_2}{c_1 + c_2} + V_{\text{ref2}} + V_{\text{th}}$ according to a charge conservation principle of charges of the storage capacitor C before and after jumping. Therefore, the drive transistor M0 is in a saturated state, and the drive transistor M0 generates the drive current IL for driving the light emitting device L to emit light according to the char-

acteristics of the current in the saturated state, I_L meets a formula:

$$I_L = K[V_{gs} - V_{th}]^2 = K[(V_{data} - V_{ref3}) \frac{c_2}{c_1 + c_2}]^2; \text{ wherein}$$

V_{gs} is a gate-source voltage of the drive transistor M0,

$$V_{gs} = (V_{data} - V_{ref3}) \frac{c_2}{c_1 + c_2} + V_{ref2} + V_{th} - V_{ref2}$$

namely

Moreover, K is a structural parameter, and

$$K = \frac{1}{2} \mu_n C_{ox} \frac{W}{L}, \mu_n \text{ represents for the migration rate of the drive transistor M0, } C_{ox} \text{ is the capacitance of a gate}$$

oxide layer on a unit area, $\frac{W}{L}$ is the width-to-length ratio of the drive transistor M0, and the numerical values in the same structure are relatively stable and may be regarded as constants. Since EM is equal to 0, the fifth switching transistor M5 is turned on, and the second electrode D of the drive transistor M0 and the light emitting device L are turned on, so that the drive current I_L generated by the drive transistor M0 is provided to the light emitting device L in order to drive the light emitting device L to emit light. Known from the formula that the drive current I_L meets, the drive current I_L , for driving the light emitting device L to emit light, of the drive transistor M0 is only related to the voltage V_{data} of the data signal Data and the voltage V_{ref1} of the first reference signal line V_{ref1} , but is unrelated to the threshold voltage V_{th} of the drive transistor M0 and the voltage V_{ref2} of the second reference signal line V_{ref2} , and influences of threshold voltage V_{th} drifting and IR Drop caused by the technological processes and long-term operation of the drive transistor M0 on the drive current I_L for driving the light emitting device L may be overcome, so that the drive current I_L for the light emitting device L is kept stable, and furthermore, the normal work of the light emitting device L is guaranteed.

[0104] Of course, during the reset phase, the signal of the third scanning signal line may also be changed to control the third switching transistor to be turned on, so that the gate electrode of the drive transistor is reset, and the voltage of the gate electrode of the drive transistor becomes V_{ref3} . Thus, during the reset phase, the voltage of the gate electrode of the drive transistor is enabled to be V_{ref3} , the voltage of the second electrode of the drive transistor is enabled to be V_{ref1} , and the voltage of the first electrode of the drive transistor is enabled to be V_{ref2} , so that the three electrodes of the drive transistor may be simultaneously reset. During the threshold compensation phase, the voltage of the gate electrode of the drive transistor is enabled to be V_{ref3} , the voltage of the second electrode of the drive transistor is enabled to be V_{ref1} , and the voltage of the first electrode of the drive transistor becomes $V_{ref3} - V_{th}$, namely before a phase that each frame data is written, the gate electrode of the drive

transistor may have the fixed voltage V_{ref3} , the first electrode of the drive transistor may have the fixed voltage $V_{ref3} - V_{th}$, and the second electrode of the drive transistor may have the fixed voltage V_{ref1} . Therefore, when the data signal is written every time, the gate electrode of the drive transistor may be jumped by the same fixed voltage, the voltage of the first electrode of the drive transistor may be jumped by the same fixed voltage, and furthermore, the short-term residual image problem caused by the hysteresis effect may be relieved.

[0105] In some other embodiments, with the pixel circuit as shown in Fig. 4b as an example, the working process of the pixel circuit is described, and an input sequence diagram corresponding to the pixel circuit is shown as Fig. 5d. Specifically, total four phases including a reset phase T1, a threshold compensation phase T2, a data write phase T3 and a light emitting phase T4 in the input sequence diagram as shown in Fig. 5d are mainly selected.

[0106] During the reset phase T1, Scan1 is equal to 1, Scan4 is equal to 0, and EM is equal to 0.

[0107] Since Scan1 is equal to 1, both the first switching transistor M1 and the third switching transistor M3 are turned on. The turn-on first switching transistor M1 provides the signal of the first reference signal line V_{ref1} to the second electrode D of the drive transistor M0, so that the second electrode D of the drive transistor M0 is reset. The turn-on third switching transistor M3 provides the signal of the first reference signal line V_{ref1} to the gate electrode G of the drive transistor M0, so that the gate electrode G of the drive transistor M0 is reset. Since EM is equal to 0, both the second switching transistor M2 and the fifth switching transistor M5 are turned on. The turn-on second switching transistor M2 provides the signal of the second reference signal line V_{ref2} to the first electrode S of the drive transistor M0, so that the first electrode S of the drive transistor M0 is reset, and the voltage V_{ref2} of the signal of the second reference signal line V_{ref2} is stored by the storage capacitor C1. The turn-on fifth switching transistor M5 turns on the second electrode D of the drive transistor M0 and the first electrode of the light emitting device L to provide the signal of the first reference signal line V_{ref1} to the light emitting device L, so that the light emitting device L is reset, and furthermore, light emitting disturbance between two adjacent display frames is avoided. Since Scan4 is equal to 0, the fourth switching transistor M4 is turned off.

[0108] During the threshold compensation phase T2, Scan1 is equal to 1, Scan4 is equal to 0, and EM is equal to 1.

[0109] Since Scan1 is equal to 1, both the first switching transistor M1 and the third switching transistor M3 are turned on. The turn-on third switching transistor M3 provides the signal of the first reference signal line V_{ref1} to the gate electrode of the drive transistor M0, so that the voltage of the gate electrode of the drive transistor M0 is V_{ref1} . The turn-on first switching transistor M1 provides the signal of the first reference signal line V_{ref1} to

the second electrode D of the drive transistor M0, so that the voltage of the second electrode D of the drive transistor M0 is Vref1. Since EM is equal to 1, both the second switching transistor M2 and the fifth switching transistor M5 are turned off. The storage capacitor C1 is capable of instantly keeping the voltage Vref2 of the first electrode of the drive transistor M0, so that the drive transistor M0 is turned on under the actions of Vref1 and Vref2, and furthermore, the voltage of the first electrode S of the drive transistor M0 is discharged by the turn-on drive transistor M0 until the voltage of the first electrode S of the drive transistor M0 becomes $V_{ref1} - V_{th}$, at the moment, the drive transistor M0 is turned off, the threshold voltage Vth of the drive transistor M0 is written into the storage capacitor C1. Therefore, the compensation of the threshold voltage Vth of the drive transistor M0 is realized, and the compensation process may not affect the light emitting device L. Since Scan4 is equal to 0, the fourth switching transistor M4 is turned off.

[0110] During the data write phase T3, Scan1 is equal to 0, Scan4 is equal to 1, and EM is equal to 1.

[0111] Since Scan4 is equal to 1, the fourth switching transistor M4 is turned on to provide the voltage Vdata of the data signal Data to the gate electrode G of the drive transistor M0, so that the voltage of the gate electrode G of the drive transistor M0 becomes Vdata. Since EM is equal to 1, both the second switching transistor M2 and the fifth switching transistor M5 are turned off. Therefore, the first electrode S of the drive transistor M0 is in a floating state; due to the coupling effect of the storage capacitor C1 and the voltage dividing effect of the voltage dividing capacitor C2, the voltage of the first electrode S of the drive transistor M0 may become

$$(V_{data} - V_{ref1}) \frac{c_1}{c_1 + c_2} + V_{ref1} - V_{th};$$

wherein c1 represents for a capacitance value of the storage capacitor C1, and c2 represents for a capacitance value of the voltage dividing capacitor C2. Since Scan1 is equal to 0, both the first switching transistor M1 and the third switching transistor M3 are turned off.

[0112] During the light emitting phase T4, Scan1 is equal to 0, Scan4 is equal to 0, and EM is equal to 0.

[0113] Since EM is equal to 0, both the second switching transistor M2 and the fifth switching transistor M5 are turned on. The turn-on second switching transistor M2 provides the voltage Vref2 of the second reference signal line Vref2 to the first electrode S of the drive transistor M0, so that the voltage of the first electrode S of the drive transistor M0 is Vref2. The voltage of the gate electrode G of the drive transistor M0 becomes

$$(V_{data} - V_{ref1}) \frac{c_2}{c_1 + c_2} + V_{ref2} + V_{th}$$

according to a charge conservation principle of charges of the storage capacitor C before and after jumping. Therefore, the drive transistor M0 is in a saturated state, and the drive transistor M0 generates the drive current IL for driving the light emitting

device L to emit light according to the characteristics of the current in the saturated state, IL meets a formula:

$$I_L = K[V_{gs} - V_{th}]^2 = K[(V_{data} - V_{ref1}) \frac{c_2}{c_1 + c_2}]^2;$$

wherein Vgs is a gate-source voltage of the drive transistor M0, namely

$$V_{gs} = (V_{data} - V_{ref1}) \frac{c_2}{c_1 + c_2} + V_{ref2} + V_{th} - V_{ref2}$$

Moreover,

$$K = \frac{1}{2} \mu_n C_{ox} \frac{W}{L},$$

ver, K is a structural parameter, and

represents for the migration rate of the drive transistor M0, Cox is the capacitance of a gate oxide layer on a

$$\frac{W}{L}$$

unit area, $\frac{W}{L}$ is the width-to-length ratio of the drive transistor M0, and the numerical values in the same structure are relatively stable and may be regarded as constants. The turn-on fifth switching transistor M5 turns on the second electrode D of the drive transistor M0 and the light emitting device L, so that the drive current IL generated by the drive transistor M0 is provided to the light emitting device L in order to drive the light emitting device L to emit light. Known from the formula that the drive current IL meets, the drive current IL, for driving the light emitting device L to emit light, of the drive transistor M0 is only related to the voltage Vdata of the data signal Data and the voltage Vref1 of the first reference signal line Vref1, but is unrelated to the threshold voltage Vth of the drive transistor M0 and the voltage Vref2 of the second reference signal line Vref2, and influences of threshold voltage Vth drifting and IR Drop caused by the technological processes and long-term operation of the drive transistor M0 on the drive current IL for driving the light emitting device L may be overcome, so that the drive current IL for the light emitting device L is kept stable, and furthermore, the normal work of the light emitting device L is guaranteed.

[0114] During the reset phase, the voltages of the gate electrode and the second electrode of the drive transistor respectively become Vref1, the voltage of the first electrode of the drive transistor becomes Vref2, so that the three electrodes of the drive transistor may be simultaneously reset. During the threshold compensation phase, the voltages of the gate electrode and the second electrode of the drive transistor are respectively enabled to be Vref1, and the voltage of the first electrode of the drive transistor is enabled to become $V_{ref1} - V_{th}$, namely before the phase that each frame data is written, the gate electrode of the drive transistor may have the fixed voltage Vref1, the first electrode of the drive transistor may have the fixed voltage $V_{ref1} - V_{th}$, and the second electrode of the drive transistor may have the fixed voltage Vref1. Therefore, when the data signal is written every time, the gate electrode of the drive transistor may be jumped by

the same fixed voltage, the voltage of the first electrode of the drive transistor may be jumped by the same fixed voltage, and furthermore, the short-term residual image problem caused by the hysteresis effect may be relieved.

[0115] Based on the same inventive concept, some embodiments of the disclosure further provide a drive method of the pixel circuit provided by some embodiments of the disclosure, as shown in Fig. 6, including:

S601, resetting the first electrode and the second electrode of the drive transistor by the reset circuit during the reset phase;

S602, providing the data signal to the gate electrode of the drive transistor by the data write circuit during the data write phase;

and S603, storing the voltage of the gate electrode of the drive transistor by the capacitance circuit, and generating the drive current by the drive transistor in order to drive the light emitting device to emit light during the light emitting phase.

[0116] According to the drive method provided by some embodiments of the disclosure, the first electrode and the second electrode of the drive transistor may be reset by the reset circuit during the reset phase, then, the data signal may be written into the gate electrode of the drive transistor by the data write circuit, and the drive current is generated by the drive transistor in order to drive the light emitting device to emit light. Thus, the voltage of the first electrode of the drive transistor may be set as the fixed voltage before the data signal is written every time, and the voltage of the second electrode of the drive transistor may be set as the fixed voltage, so that influences of the residual voltage of the previous frame on the light emission of the frame may be avoided, and furthermore, the light emitting uniformity of the display panel may be improved.

[0117] During specific implementation, the drive method provided by some embodiments of the disclosure may further include: resetting the gate electrode of the drive transistor by the reset circuit during the reset phase.

[0118] Moreover, after the reset phase and before the data write phase, the method provided by some embodiments of the disclosure may further include: compensating the threshold voltage of the drive transistor by the reset circuit during the threshold compensation phase.

[0119] During specific implementation, when the reset circuit includes the first switching transistor, the second switching transistor and the third switching transistor, in the drive method provided by some embodiments of the disclosure, during the reset phase, the first switching transistor in the reset circuit is controlled to be turned on and the signal of the first reference signal line is controlled to be provided to the second electrode of the drive transistor, the second switching transistor is controlled to be

trolled to be turned on and the signal of the third reference signal line is controlled to be provided to the gate electrode of the drive transistor.

[0120] Moreover, during the threshold compensation phase, the second switching transistor in the reset circuit is controlled to be turned off, the first switching transistor is controlled to be turned on and the signal of the first reference signal line is controlled to be provided to the second electrode of the drive transistor, the third switching transistor is controlled to be turned on and the signal of the third reference signal line is controlled to be provided to the gate electrode of the drive transistor; and the drive transistor is turned on to perform threshold compensation.

[0121] During specific implementation, the drive method provided by some embodiments of the disclosure may further include: turning on the second electrode of the drive transistor and the first electrode of the light emitting device by the light emitting control circuit during the reset phase and the light emitting phase.

[0122] During specific implementation, due to the effects of the reset phase, the threshold compensation phase, the data write phase and the light emitting phase, the drive current, for driving the light emitting device to emit light, of the drive transistor may be only related to the voltage of the data signal and the voltage of the signal of the first reference signal line, but may be unrelated to the threshold voltage of the drive transistor and the voltage of the signal of the second reference signal line, and influences of the threshold voltage of the drive transistor and the IR Drop of the second reference signal line on the drive current flowing through the light emitting device may be avoided, so that the working current for driving the light emitting device to emit light is kept stable, and furthermore, the brightness uniformity of a display frame in the display panel may be improved.

[0123] Based on the same inventive concept, some embodiments of the disclosure further provide an electroluminescent light emitting display panel, as shown in Fig. 7, including a pixel circuit (PX), a data signal line DATA, a first scanning signal line Scan1, a second scanning signal line Scan2, a third scanning signal line Scan3, a fourth scanning signal line Scan4, a light emitting control signal line EMIT, a first reference voltage line Vref1, a second reference voltage line Vref2 and a third reference voltage line Vref3;

the pixel circuit PX may include a first switching transistor M1, a second switching transistor M2, a third switching transistor M3, a fourth switching transistor M4, a fifth switching transistor M5, a drive transistor M0, a storage capacitor C1, a voltage dividing capacitor C2 and a light emitting device L; wherein

a gate electrode of the first switching transistor M1 is coupled to the first scanning signal line Scan1 applying the current corresponding signal to the gate electrode of the first switching transistor M1, a first electrode of the first switching transistor M1 is coupled to the first reference signal line Vref1, and a second electrode of the first

switching transistor M1 is coupled to a second electrode D of the drive transistor M0;

a gate electrode of the second switching transistor M2 is coupled to the second scanning signal line Scan2 applying the current corresponding signal to the gate electrode of the second switching transistor M2, a first electrode of the second switching transistor M2 is coupled to the second reference signal line Vref2, and a second electrode of the second switching transistor M2 is coupled to a first electrode S of the drive transistor M0;

a gate electrode of the third switching transistor M3 is coupled to the third scanning signal line Scan3 applying the current corresponding signal to the gate electrode of the third switching transistor M3, a first electrode of the third switching transistor M3 is coupled to the third reference signal line Vref3, and a second electrode of the third switching transistor M3 is coupled to a gate electrode G of the drive transistor M0;

a gate electrode of the fourth switching transistor M4 is coupled to the fourth scanning signal line Scan4 applying the current corresponding signal to the gate electrode of the fourth switching transistor M4, a first electrode of the fourth switching transistor M4 is coupled to the data signal line DATA applying the current corresponding signal to the first electrode of the fourth switching transistor M4, and a second electrode of the fourth switching transistor M4 is coupled to the gate electrode G of the drive transistor M0;

a gate electrode of the fifth switching transistor M5 is coupled to the light emitting control signal line EMIT applying the current corresponding signal to the gate electrode of the fifth switching transistor M5, a first electrode of the fifth switching transistor M5 is respectively coupled to the second electrode D of the drive transistor M0 and the second electrode of the first switching transistor M1, and a second electrode of the fifth switching transistor M5 is coupled to a first electrode of the light emitting device L;

the storage capacitor C1 is coupled between the gate electrode G and the first electrode S of the drive transistor M0;

and the voltage dividing capacitor C2 is coupled between the first electrode S of the drive transistor M0 and the second reference signal line Vref2.

[0124] According to the electroluminescent light emitting display panel provided by some embodiments of the disclosure, the corresponding signal is input by each signal line, so that the first switching transistor, the second switching transistor, the third switching transistor, the fourth switching transistor, the fifth switching transistor, the drive transistor, the storage capacitor, the voltage dividing capacitor and the light emitting device in the pixel circuit are controlled to mutually cooperate, so that the light emitting display of the electroluminescent light emitting display panel may be realized.

[0125] During specific implementation, the electroluminescent light emitting display panel provided by some embodiments of the disclosure may further include a gate

electrode drive circuit; wherein corresponding gate electrode scanning signals are provided to the first scanning signal line, the second scanning signal line, the third scanning signal line and the fourth scanning signal line by the gate electrode drive circuit.

[0126] During specific implementation, the electroluminescent light emitting display panel provided by some embodiments of the disclosure may further include a light emitting control circuit; wherein a corresponding light emitting control signal is provided to the light emitting control signal line by the light emitting control circuit.

[0127] During specific implementation, the electroluminescent light emitting display panel provided by some embodiments of the disclosure may further include a source electrode drive circuit; wherein a corresponding data signal is provided to the data signal line by the source electrode drive circuit.

[0128] During specific implementation, the working process of the pixel circuit in the electroluminescent light emitting display panel provided by some embodiments of the disclosure may refer to the implementation of the pixel circuit, and the descriptions thereof are omitted herein.

[0129] During specific implementation, the electroluminescent light emitting display panel provided by some embodiments of the disclosure is capable of guaranteeing display uniformity when performing display by reducing the refresh frequency by combining the two processes for preparing the transistors including the LTPS-type transistors and the oxide thin film transistors.

[0130] During specific implementation, in the electroluminescent light emitting display panel provided by some embodiments of the disclosure, the data signal line and the second reference signal line may be respectively made of the same material and arranged on the same layer with the first electrodes and the second electrodes of the switching transistors in the pixel circuit; moreover, the first scanning signal line, the second scanning signal line, the third scanning signal line, the fourth scanning signal line, the light emitting control signal line, the first reference signal line and the third reference signal line may be respectively made of the same material and arranged on the same layer with the gate electrodes of the switching transistors in the pixel circuit. Thus, patterns of the data signal line, the second reference signal line as well as the first electrodes and the second electrodes of the switching transistors in the pixel circuit may be simultaneously formed by adopting a primary patterning process, and patterns of all scanning signal lines, the first reference signal line, the third reference signal line, the light emitting control signal line as well as the gate electrodes of the switching transistors in the pixel circuit may be simultaneously formed by adopting another primary patterning process, so that the preparation process may be simplified, and the thickness of the electroluminescent light emitting display panel may be reduced.

[0131] During specific implementation, when the data signal line and the second reference signal line as well

as the first electrodes and the second electrodes of the switching transistors in the pixel circuit are made of the same material and are arranged on the same layer, in the electroluminescent light emitting display panel provided by some embodiments of the disclosure, the data signal line may extend in a column direction of pixel units formed by the pixel circuit, and the second reference signal line extends in the column direction of the pixel units. Of course, the second reference signal line may also be arranged in the electroluminescent light emitting display panel by adopting a grid structure.

[0132] During specific implementation, when all scanning signal lines, all reference signal lines, the light emitting control signal line and the gate electrodes of the switching transistors in the pixel circuit are made of the same material and arranged on the same layer, in the electroluminescent light emitting display panel provided by some embodiments of the disclosure, all scanning signal lines, the first reference signal line, the third reference signal line and the light emitting control signal line may extend in a row direction of the pixel units. Moreover, since a gap between two adjacent rows of pixel units is generally larger than that of two adjacent columns of pixel units, the layout design of the electroluminescent light emitting display panel may be further optimized by respectively enabling all reference signal lines towards the row direction of the pixel units.

[0133] In order to reduce the arrangement of the signal lines and save the line arrangement space, during specific implementation, in the electroluminescent light emitting display panel provided by some embodiments of the disclosure, the signals of the first scanning signal line and the third scanning signal line coupled to the same pixel circuit may be set to be the same. Alternatively, the first scanning signal line and the third scanning signal line coupled to the same pixel circuit are enabled to be set as the same signal line. Optionally, as shown in Fig. 8, both the gate electrode of the first switching transistor M1 and the gate electrode of the third switching transistor M3 are coupled to the first scanning signal line Scan1.

[0134] In order to reduce the arrangement of the signal lines and save the line arrangement space, during specific implementation, in the electroluminescent light emitting display panel provided by some embodiments of the disclosure, the signals of the light emitting control signal line and the second scanning signal line coupled to the same pixel circuit may be set to be the same. Alternatively, the light emitting control signal line and the second scanning signal line coupled to the same pixel circuit are enabled to be set as the same signal line. Thus, the layout design of the electroluminescent light emitting display panel may be further optimized. Specifically, as shown in Fig. 8, both the second switching transistor M2 and the fifth switching transistor M5 are coupled to the light emitting control signal line EMIT.

[0135] In order to reduce the arrangement of the signal lines and save the line arrangement space, during specific implementation, in the electroluminescent light emitting

display panel provided by some embodiments of the disclosure, the signal of the first reference signal line and the signal of the third reference signal line may be set to be the same. Alternatively, the first reference signal line and the third reference signal line are enabled to be also set as the same signal line. Thus, the layout design of the electroluminescent light emitting display panel may be further optimized. Optionally, as shown in Fig. 8, both the first switching transistor M1 and the third switching transistor M3 are coupled to the first reference signal line Vref1.

[0136] The cathode of the light emitting device in the electroluminescent light emitting display panel provided by some embodiments of the disclosure may be the same as the design in the prior art, for example, the cathode may be designed to be a one-whole-side cathode layer, the descriptions thereof are omitted herein.

[0137] During specific implementation, the electroluminescent light emitting display panel provided by some embodiments of the disclosure may be an organic light emitting display panel or a quantum dot light emitting display panel, but is not limited herein.

[0138] Based on the same inventive concept, some embodiments of the disclosure further provide a display apparatus including the electroluminescent light emitting display panel provided by some embodiments of the disclosure. The display apparatus may be any product or component with a display function, such as a mobile phone, a tablet personal computer, a display, a notebook computer, a digital photo frame and a navigator. Other essential components of the display apparatus should be understood to be provided by the ordinary skilled in the art, the descriptions thereof are omitted herein, and the components should not be regarded as limits to the disclosure. The implementation of the display apparatus may refer to some embodiments of the pixel circuit, the descriptions thereof are omitted herein.

[0139] According to the pixel circuit, the drive method, the electroluminescent light emitting display panel, and the display apparatus provided by some embodiments of the disclosure, the first electrode and the second electrode of the drive transistor may be reset by the reset circuit during the reset phase, then, the data signal may be written into the gate electrode of the drive transistor by the data write circuit, and the drive current is generated by the drive transistor in order to drive the light emitting device to emit light. Thus, the voltage of the first electrode of the drive transistor may be set as a fixed voltage before the data signal is written every time, and the voltage of the second electrode of the drive transistor may be set as the fixed voltage, so that influences of the residual voltage of the previous frame on the light emission of the frame may be avoided, and furthermore, the light emitting uniformity of the display panel may be improved.

[0140] Although the preferred embodiments of the disclosure have been described, the embodiments may be further altered and modified once the basic creative concept is known by the skilled in the art. Therefore, append-

ed claims intend to be explained to include the preferred embodiments and all alterations and modifications falling into the scope of the disclosure.

[0141] It is apparent that various alternations and modifications of some embodiments of the disclosure may be made without departing from the spirit and scope of some embodiments of the disclosure by the skilled in the art. Thus, if the alterations and modifications of some embodiments of the disclosure fall into the claims of the disclosure and the equivalent technical scope thereof, the disclosure also intends to include the alterations and modifications.

Claims

1. A pixel circuit, comprising:

a light emitting device;
 a drive transistor, configured to generate a drive current during a light emitting phase in order to drive the light emitting device to emit light; wherein a gate electrode of the drive transistor is respectively coupled to a capacitance circuit and a data write circuit, a first electrode of the drive transistor is coupled to a reset circuit, and a second electrode of the drive transistor is respectively coupled to the reset circuit and a first electrode of the light emitting device;
 the capacitance circuit, configured to store a voltage of the gate electrode of the drive transistor;
 the data write circuit, configured to provide a data signal to the gate electrode of the drive transistor during a data write phase;
 and the reset circuit, configured to reset the first electrode and the second electrode of the drive transistor during a reset phase.

2. The pixel circuit according to claim 1, wherein the reset circuit is further coupled to the gate electrode of the drive transistor, is configured to reset the gate electrode of the drive transistor during the reset phase and is configured to compensate a threshold voltage of the drive transistor during a threshold compensation phase.

3. The pixel circuit according to claim 2, wherein the reset circuit comprises a first switching transistor, a second switching transistor and a third switching transistor;
 a gate electrode of the first switching transistor is coupled to a first scanning signal line, a first electrode of the first switching transistor is coupled to a first reference signal line, and a second electrode of the first switching transistor is coupled to the second electrode of the drive transistor;
 a gate electrode of the second switching transistor

is coupled to a second scanning signal line, a first electrode of the second switching transistor is coupled to a second reference signal line, and a second electrode of the second switching transistor is coupled to the first electrode of the drive transistor;
 and a gate electrode of the third switching transistor is coupled to a third scanning signal line, a first electrode of the third switching transistor is coupled to a third reference signal line, and a second electrode of the third switching transistor is coupled to the gate electrode of the drive transistor.

4. The pixel circuit according to claim 3, wherein materials of active layers of the first switching transistor and the third switching transistor comprise a metal oxide semiconductor material;
 and a material of an active layer of the second switching transistor comprises a low temperature poly-silicon material.

5. The pixel circuit according to claim 3, wherein a signal of the first scanning signal line is same as a signal of the third scanning signal line.

6. The pixel circuit according to claim 3, wherein a signal of the first reference signal line is same as a signal of the third reference signal line.

7. The pixel circuit according to claim 1, wherein the capacitance circuit comprises a storage capacitor and a voltage dividing capacitor:

the storage capacitor is coupled between the gate electrode and the first electrode of the drive transistor;
 and the voltage dividing capacitor is coupled between the first electrode of the drive transistor and the second reference signal line.

8. The pixel circuit according to claim 1, wherein the data write circuit comprises a fourth switching transistor;
 a gate electrode of the fourth switching transistor is coupled to a fourth scanning signal line, a first electrode of the fourth switching transistor is coupled to a data signal line and is configured to receive a data signal, and a second electrode of the fourth switching transistor is coupled to the gate electrode of the drive transistor.

9. The pixel circuit according to claim 8, wherein a material of an active layer of the fourth switching transistor comprises a metal oxide semiconductor material.

10. The pixel circuit according to claim 1, further comprising a light emitting control circuit; the second electrode of the drive transistor and the reset circuit

being respectively coupled to the first electrode of the light emitting device by the light emitting control circuit; wherein the light emitting control circuit is configured to control the second electrode of the drive transistor and the first electrode of the light emitting device to be turned on or off.

11. The pixel circuit according to claim 10, wherein the light emitting control circuit comprises a fifth switching transistor;

a gate electrode of the fifth switching transistor is coupled to a light emitting control signal line, a first electrode of the fifth switching transistor is coupled to the second electrode of the drive transistor, and a second electrode of the fifth switching transistor is coupled to the first electrode of the light emitting device.

12. The pixel circuit according to claim 11, wherein a material of an active layer of the fifth switching transistor comprises a low temperature poly-silicon material.

13. The pixel circuit according to claim 11, wherein a signal of the light emitting control signal line is same as a signal of the second scanning signal line.

14. The pixel circuit according to any one of claims 1-13, wherein a material of an active layer of the drive transistor comprises a low temperature poly-silicon material.

15. A pixel circuit, comprising:

a light emitting device;

a first switching transistor, a gate electrode of the first switching transistor being coupled to a first scanning signal line, a first electrode of the first switching transistor being coupled to a first reference signal line, and a second electrode of the first switching transistor being coupled to a second electrode of a drive transistor;

a second switching transistor, a gate electrode of the second switching transistor being coupled to a second scanning signal line, a first electrode of the second switching transistor being coupled to a second reference signal line, and a second electrode of the second switching transistor being coupled to a first electrode of the drive transistor;

a third switching transistor, a gate electrode of the third switching transistor being coupled to a third scanning signal line, a first electrode of the third switching transistor being coupled to a third reference signal line, and a second electrode of the third switching transistor being coupled to a gate electrode of the drive transistor;

a fourth switching transistor, a gate electrode of

the fourth switching transistor being coupled to a fourth scanning signal line, a first electrode of the fourth switching transistor being coupled to a data signal line, and a second electrode of the fourth switching transistor being coupled to the gate electrode of the drive transistor;

a fifth switching transistor, a gate electrode of the fifth switching transistor being coupled to a light emitting control signal line, a first electrode of the fifth switching transistor being respectively coupled to the second electrode of the drive transistor and the second electrode of the first switching transistor, and a second electrode of the fifth switching transistor being coupled to a first electrode of the light emitting device;

a storage capacitor, the storage capacitor being coupled between the gate electrode and the first electrode of the drive transistor;

and a voltage dividing capacitor, the voltage dividing capacitor being coupled between the first electrode of the drive transistor and the second reference signal line.

16. The pixel circuit according to claim 15, wherein materials of active layers of the first switching transistor, the third switching transistor and the fourth switching transistor comprise a metal oxide semiconductor material;

and materials of active layers of the second switching transistor, the fifth switching transistor and the drive transistor comprise a low temperature poly-silicon material.

17. The pixel circuit according to claim 15, wherein a signal of the first scanning signal line is same as a signal of the third scanning signal line.

18. The pixel circuit according to claim 15, wherein a signal of the first reference signal line is same as a signal of the third reference signal line.

19. The pixel circuit according to claim 15, wherein a signal of the light emitting control signal line is same as a signal of the second scanning signal line.

20. An electroluminescent light emitting display panel, comprising a pixel circuit, a data signal line, a first scanning signal line, a second scanning signal line, a third scanning signal line, a fourth scanning signal line, a light emitting control signal line, a first reference voltage line, a second reference voltage line and a third reference voltage line;

the pixel circuit comprising a first switching transistor, a second switching transistor, a third switching transistor, a fourth switching transistor, a fifth switching transistor, a drive transistor, a storage capacitor, a voltage dividing capacitor and a light emitting device; wherein

a gate electrode of the first switching transistor is coupled to the first scanning signal line applying the current corresponding signal to the gate electrode of the first switching transistor, a first electrode of the first switching transistor is coupled to the first reference signal line, and a second electrode of the first switching transistor is coupled to the second electrode of the drive transistor;

a gate electrode of the second switching transistor is coupled to the second scanning signal line applying the current corresponding signal to the gate electrode of the second switching transistor, a first electrode of the second switching transistor is coupled to the second reference signal line, and a second electrode of the second switching transistor is coupled to a first electrode of the drive transistor;

a gate electrode of the third switching transistor is coupled to the third scanning signal line applying the current corresponding signal to the gate electrode of the third switching transistor, a first electrode of the third switching transistor is coupled to the third reference signal line, and a second electrode of the third switching transistor is coupled to a gate electrode of the drive transistor;

a gate electrode of the fourth switching transistor is coupled to the fourth scanning signal line applying the current corresponding signal to the gate electrode of the fourth switching transistor, a first electrode of the fourth switching transistor is coupled to the data signal line applying the current corresponding signal to the first electrode of the fourth switching transistor, and a second electrode of the fourth switching transistor is coupled to the gate electrode of the drive transistor;

a gate electrode of the fifth switching transistor is coupled to the light emitting control signal line applying the current corresponding signal to the gate electrode of the fifth switching transistor, a first electrode of the fifth switching transistor is respectively coupled to the second electrode of the drive transistor and the second electrode of the first switching transistor, and a second electrode of the fifth switching transistor is coupled to a first electrode of the light emitting device;

the storage capacitor is coupled between the gate electrode and the first electrode of the drive transistor;

and the voltage dividing capacitor is coupled between the first electrode of the drive transistor and the second reference signal line.

21. The electroluminescent light emitting display panel according to claim 20, wherein signals of the first scanning signal line and the third scanning signal line coupled to a same pixel circuit are same.
22. The electroluminescent light emitting display panel according to claim 20, wherein a signal of the first

reference signal line is same as a signal of the third reference signal line.

23. The electroluminescent light emitting display panel according to claim 20, wherein signals of the light emitting control signal line and the second scanning signal line coupled to a same pixel circuit are same.
24. A display apparatus, comprising the electroluminescent light emitting display panel according to any one of claims 20-23.
25. A drive method of the pixel circuit according to any one of claims 1-14, comprising:

resetting the first electrode and the second electrode of the drive transistor by the reset circuit during a reset phase;
providing the data signal to the gate electrode of the drive transistor by the data write circuit during a data write phase;
and storing the voltage of the gate electrode of the drive transistor by the capacitance circuit, and generating the drive current by the drive transistor in order to drive the light emitting device to emit light during a light emitting phase.

26. The method according to claim 25, further comprising: resetting the gate electrode of the drive transistor by the reset circuit during the reset phase;
and after the reset phase and before the data write phase, the method further comprising: compensating the threshold voltage of the drive transistor by the reset circuit during a threshold compensation phase.
27. The method according to claim 26, wherein during the reset phase, the first switching transistor in the reset circuit is controlled to be turned on and the signal of the first reference signal line is controlled to be provided to the second electrode of the drive transistor, the second switching transistor is controlled to be turned on and the signal of the second reference signal line is controlled to be provided to the first electrode of the drive transistor, the third switching transistor is controlled to be turned on and the signal of the third reference signal line is controlled to be provided to the gate electrode of the drive transistor;
and during the threshold compensation phase, the second switching transistor in the reset circuit is controlled to be turned off, the first switching transistor is controlled to be turned on and the signal of the first reference signal line is controlled to be provided to the second electrode of the drive transistor, the third switching transistor is controlled to be turned on and the signal of the third reference signal line is controlled to be provided to the gate electrode of the

drive transistor; and the drive transistor is turned on to perform threshold compensation.

- 28.** The method according to claim 25, further comprising: turning on the second electrode of the drive transistor and the first electrode of the light emitting device by the light emitting control circuit during the reset phase and the light emitting phase.

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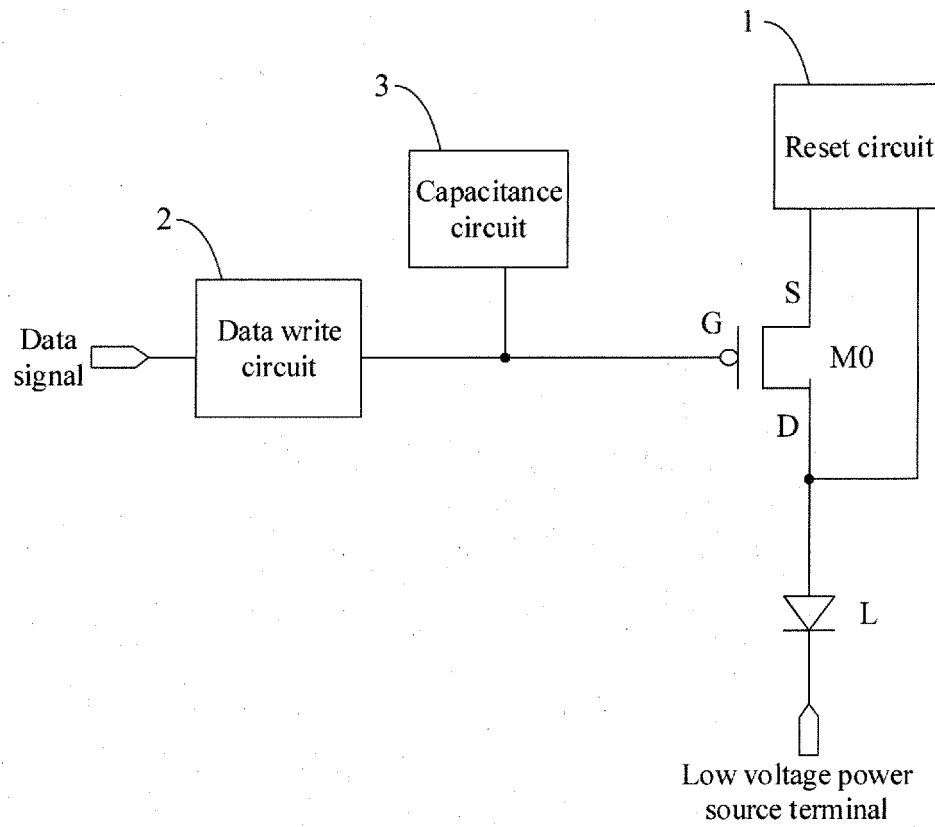


Fig. 1

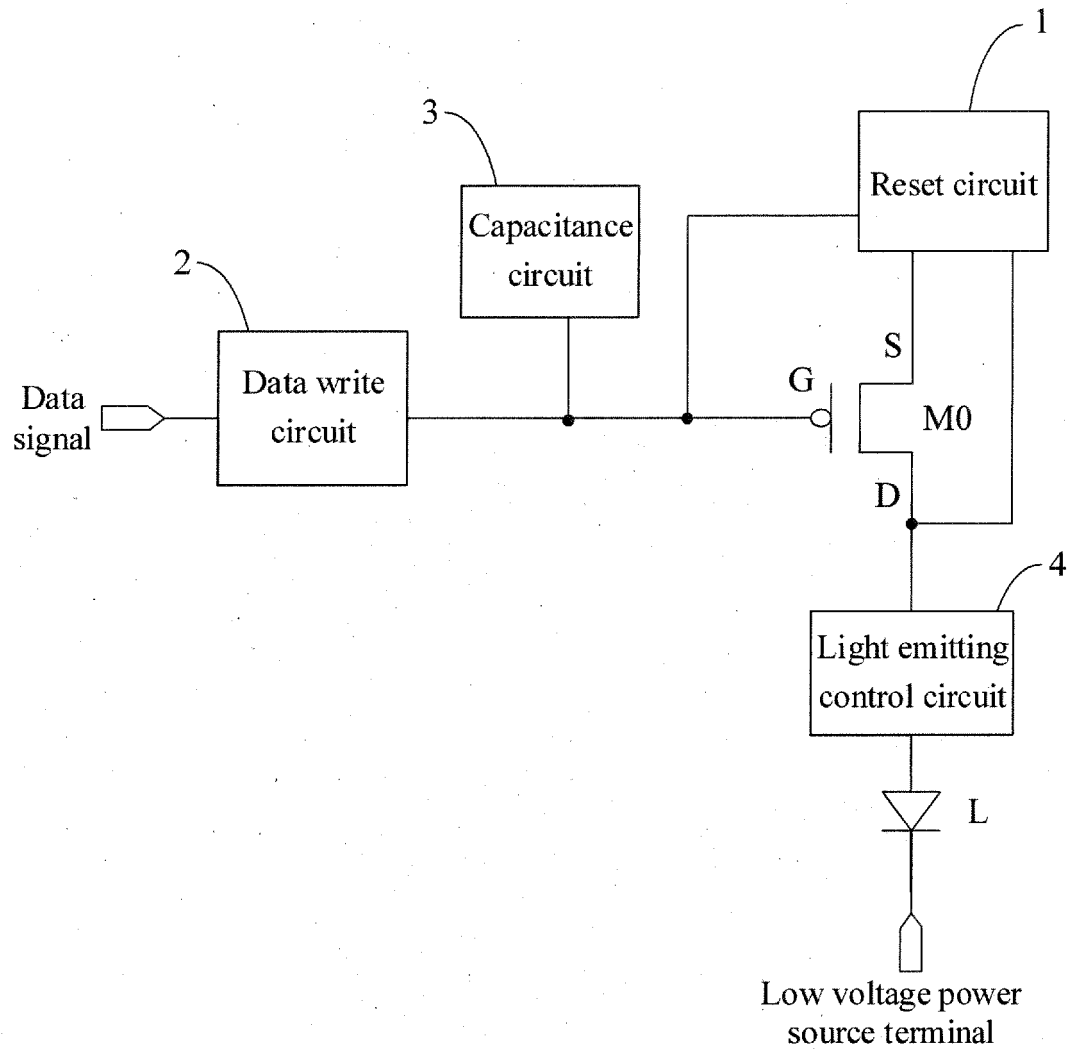


Fig. 2

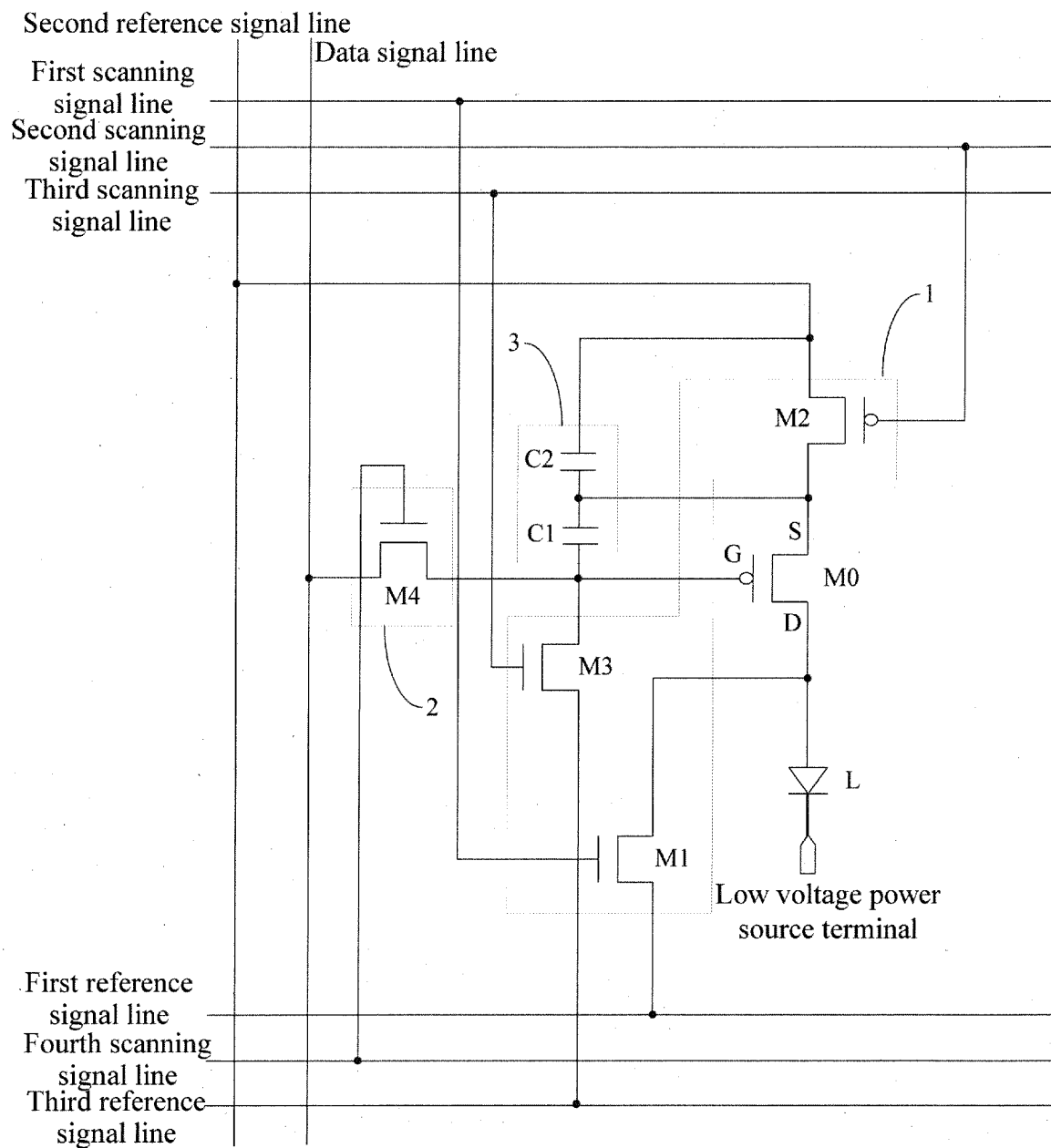


Fig. 3a

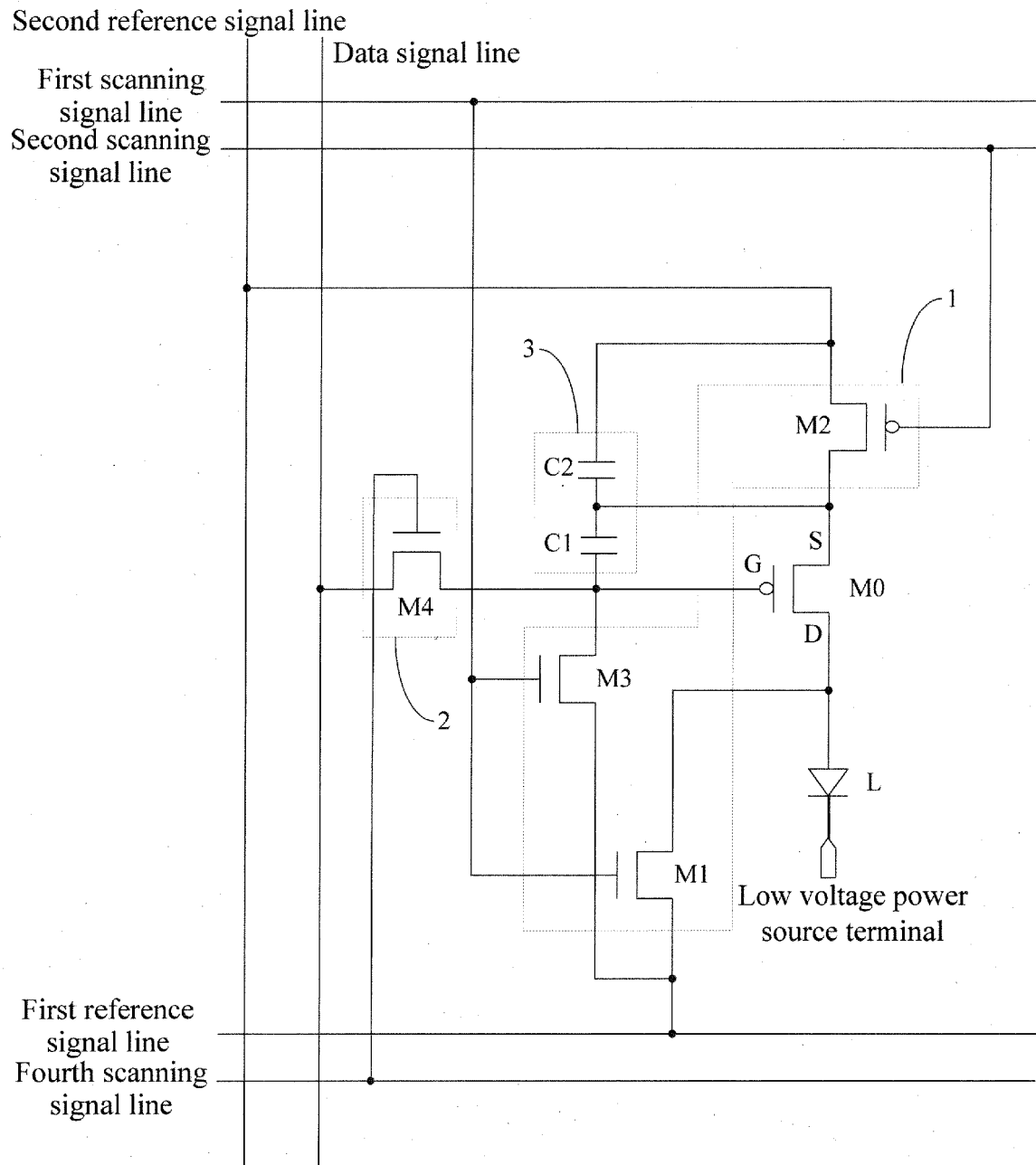


Fig. 3b

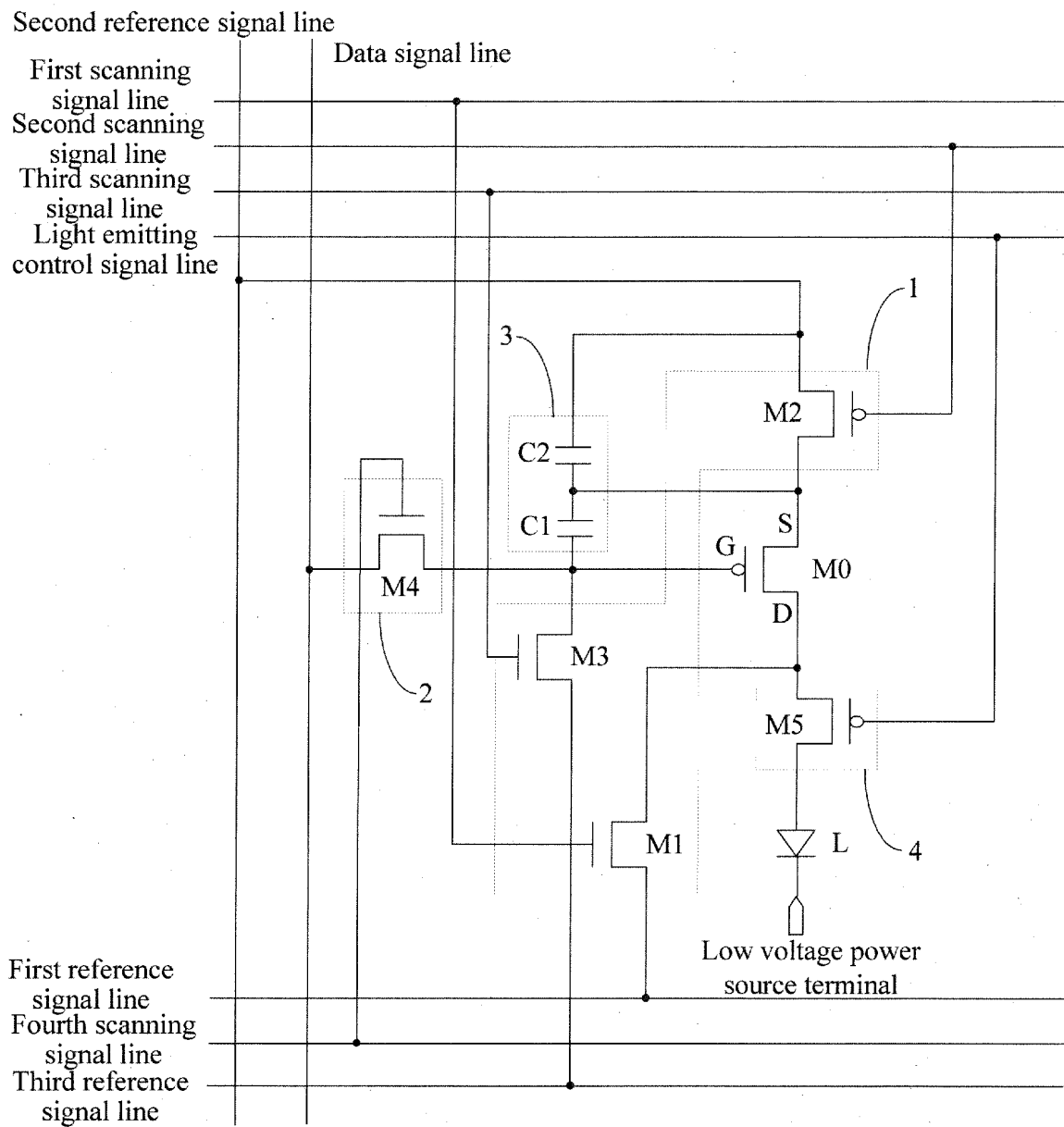


Fig. 4a

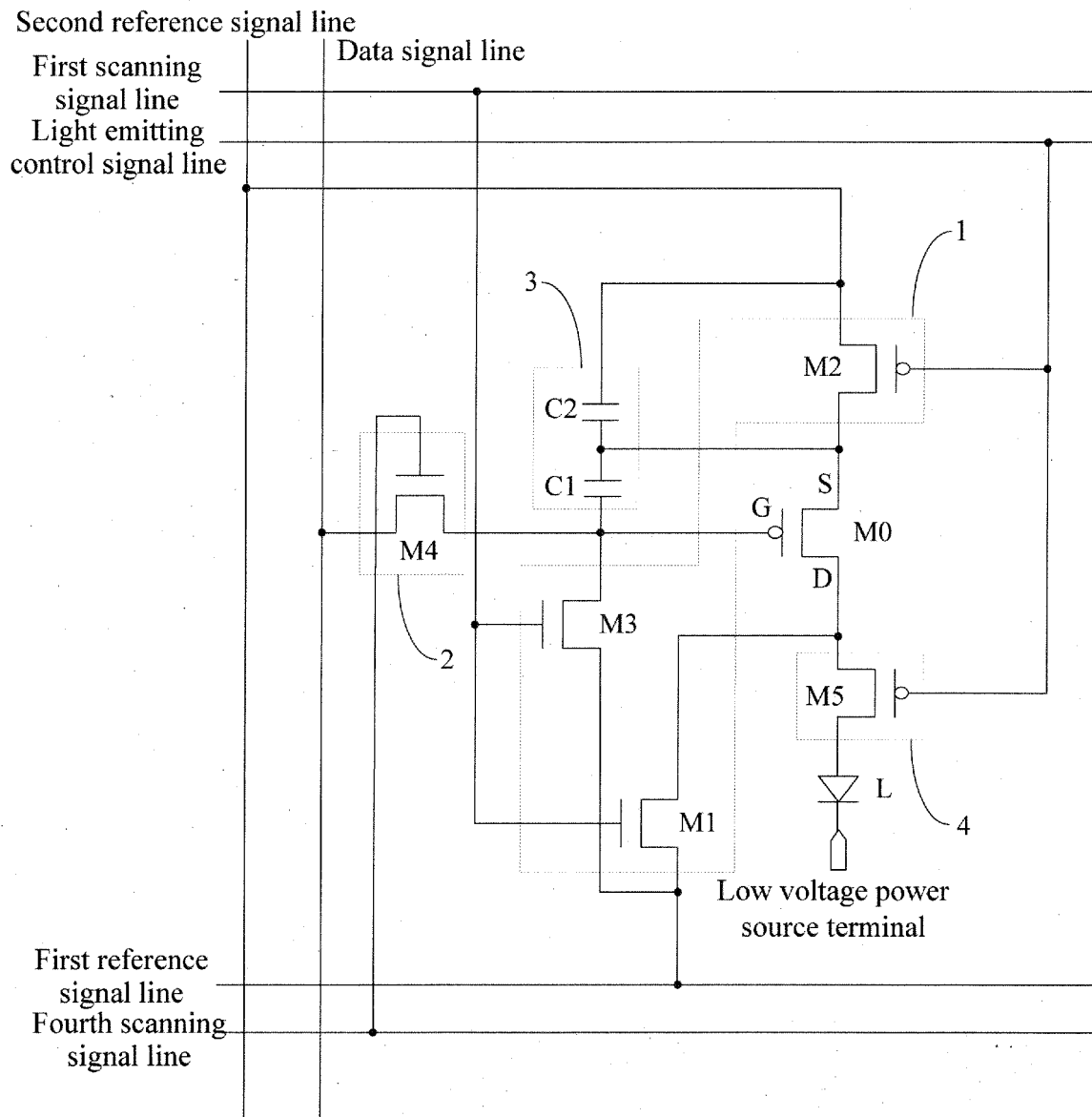


Fig. 4b

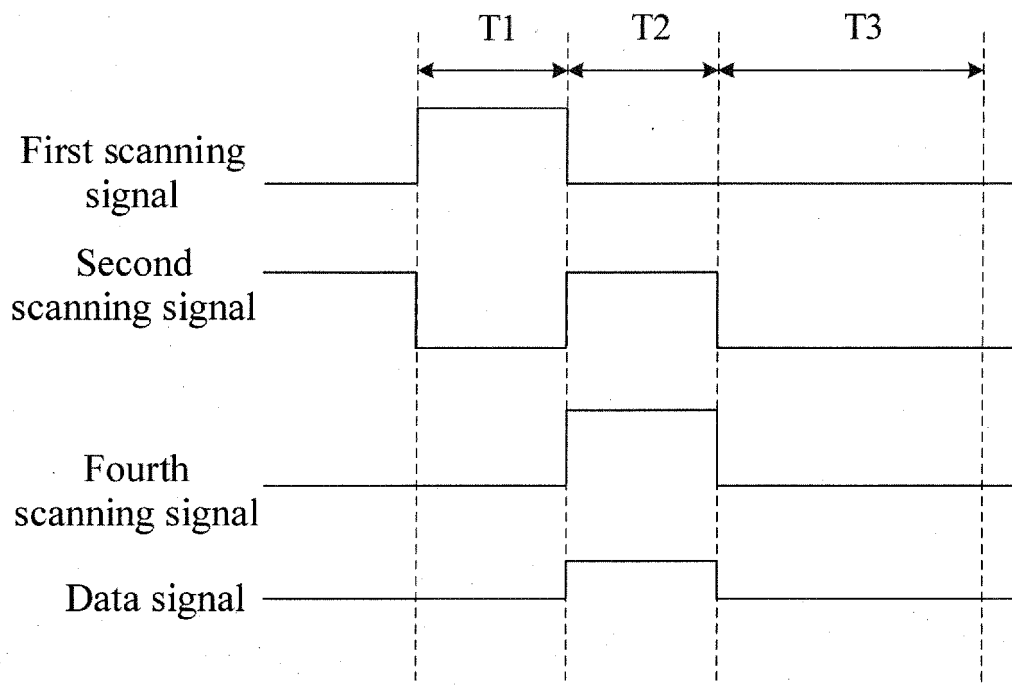


Fig. 5a

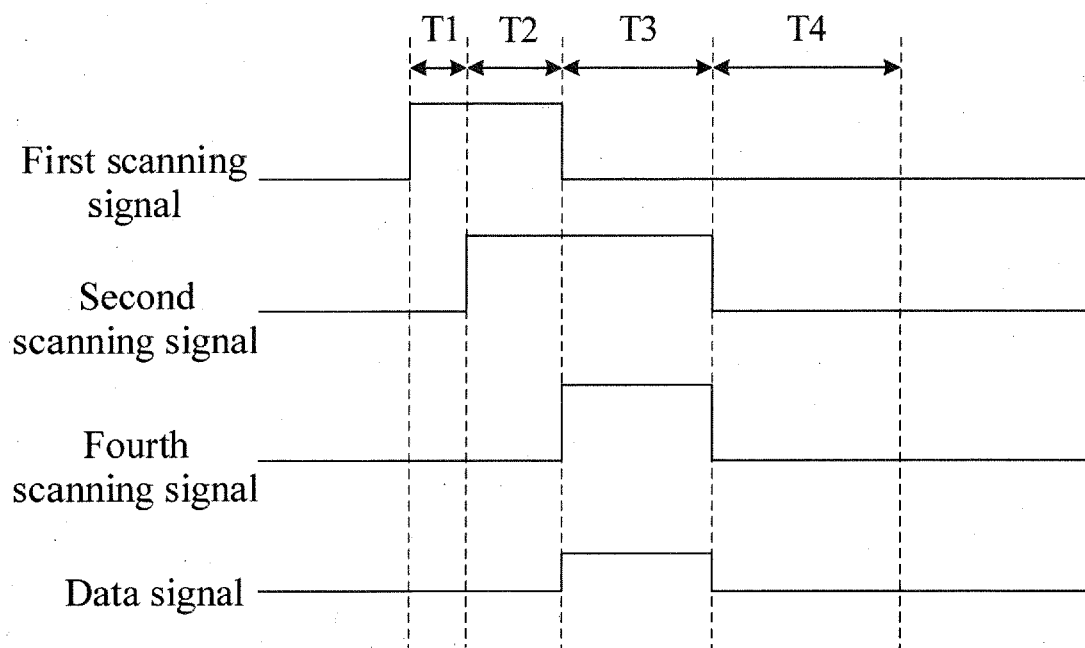


Fig. 5b

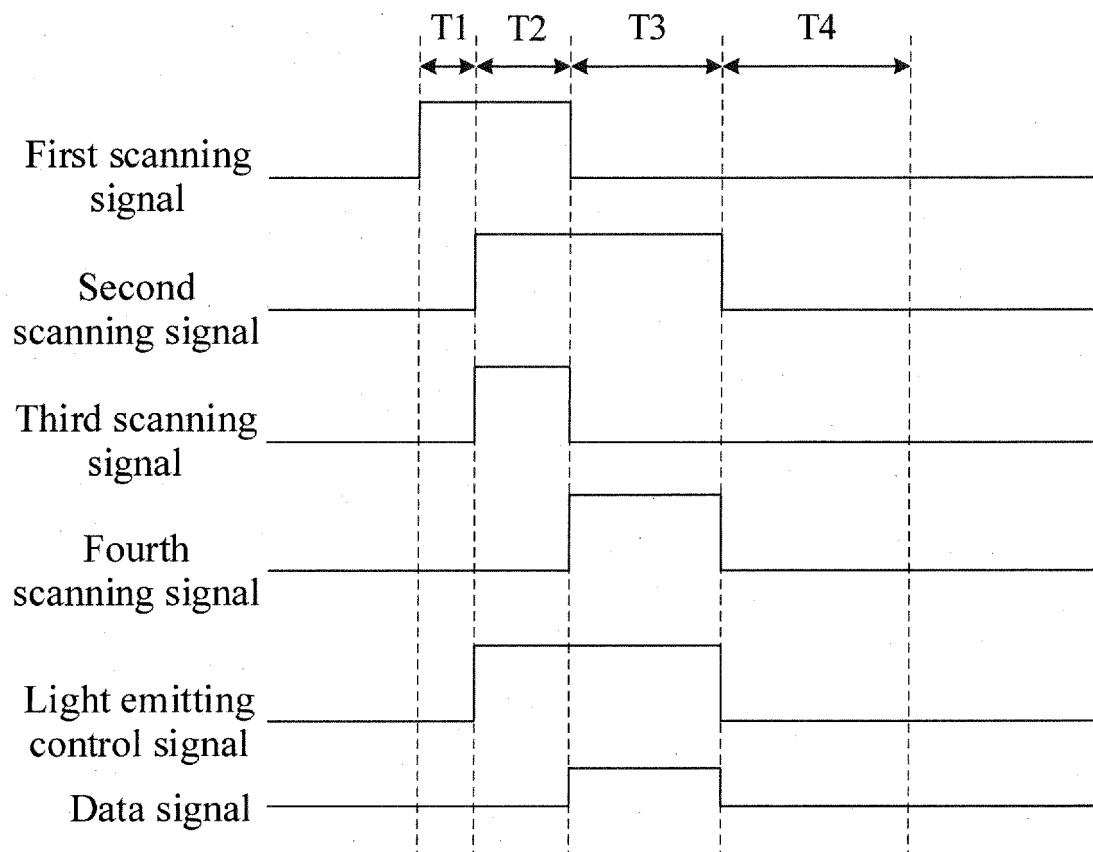


Fig. 5c

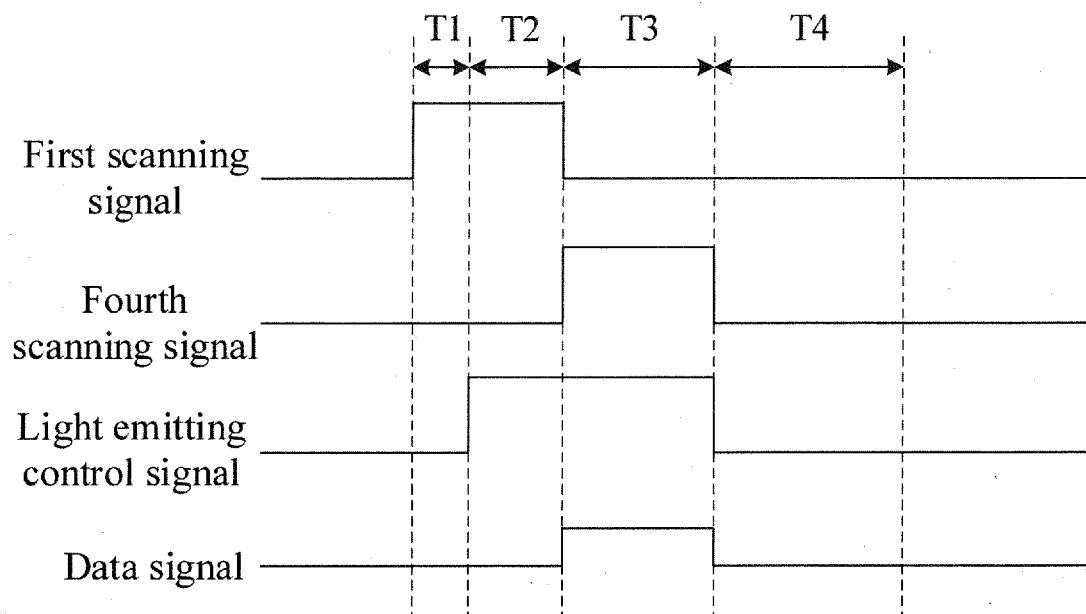


Fig. 5d

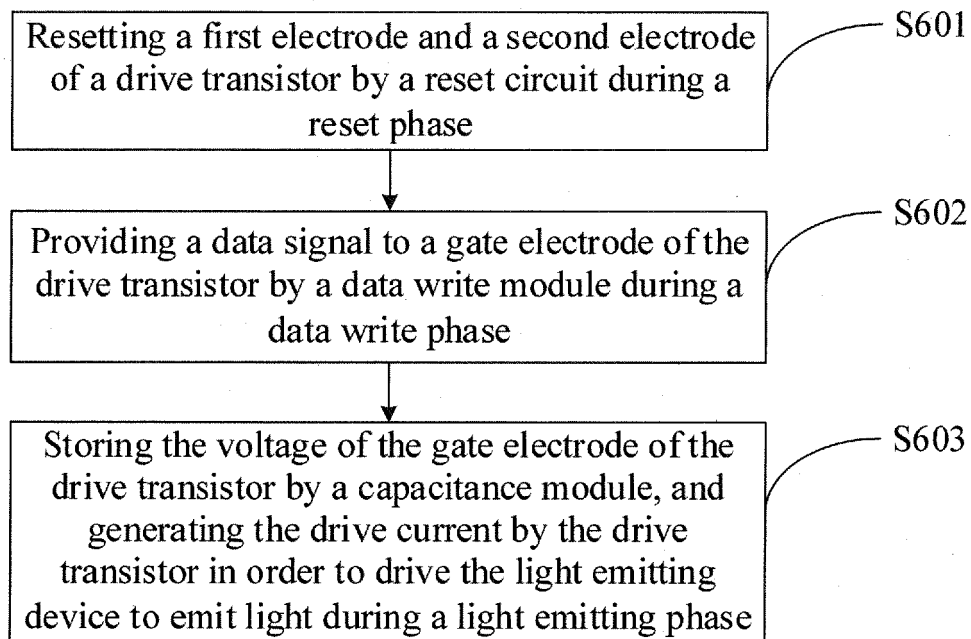


Fig. 6

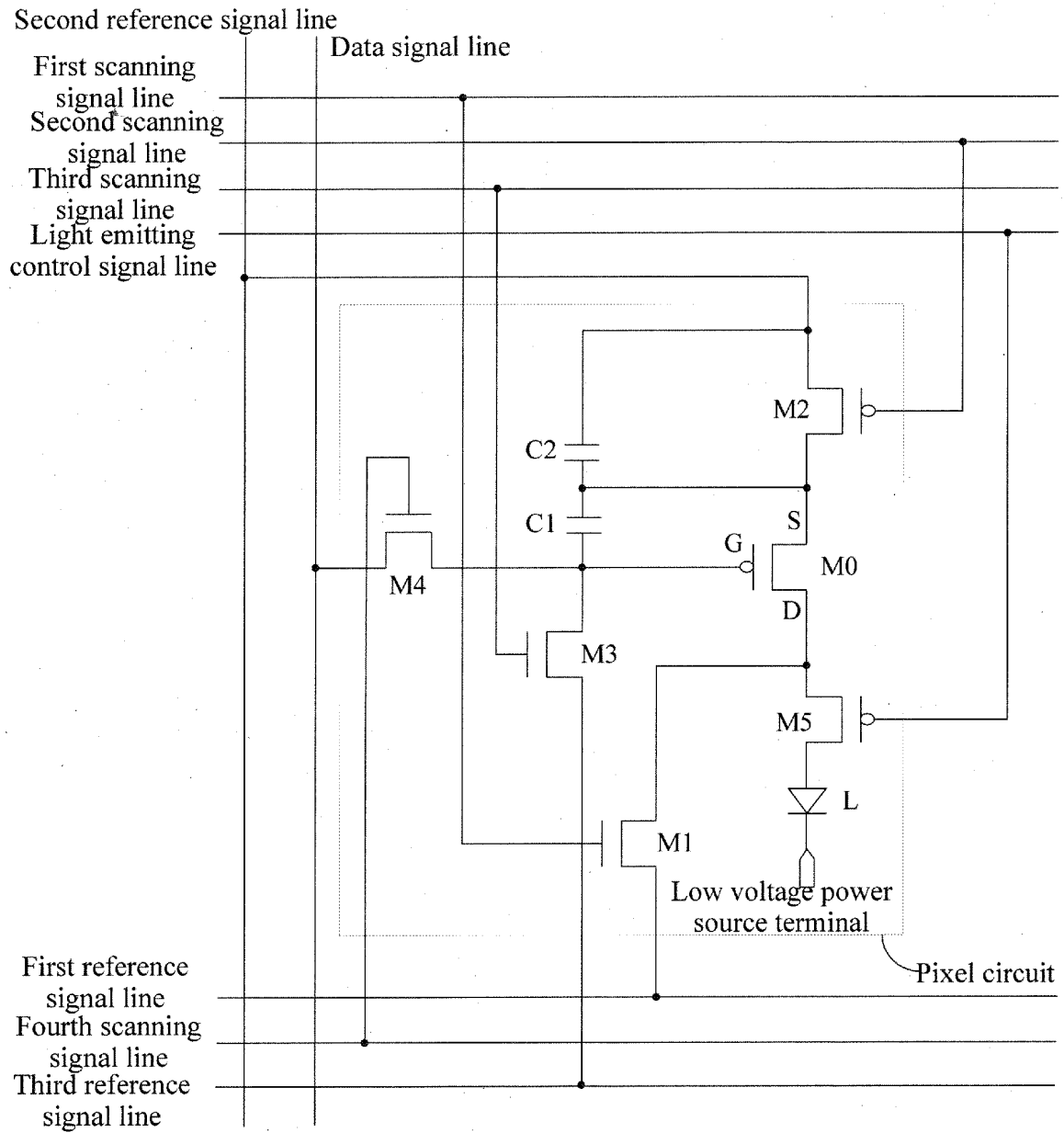


Fig. 7

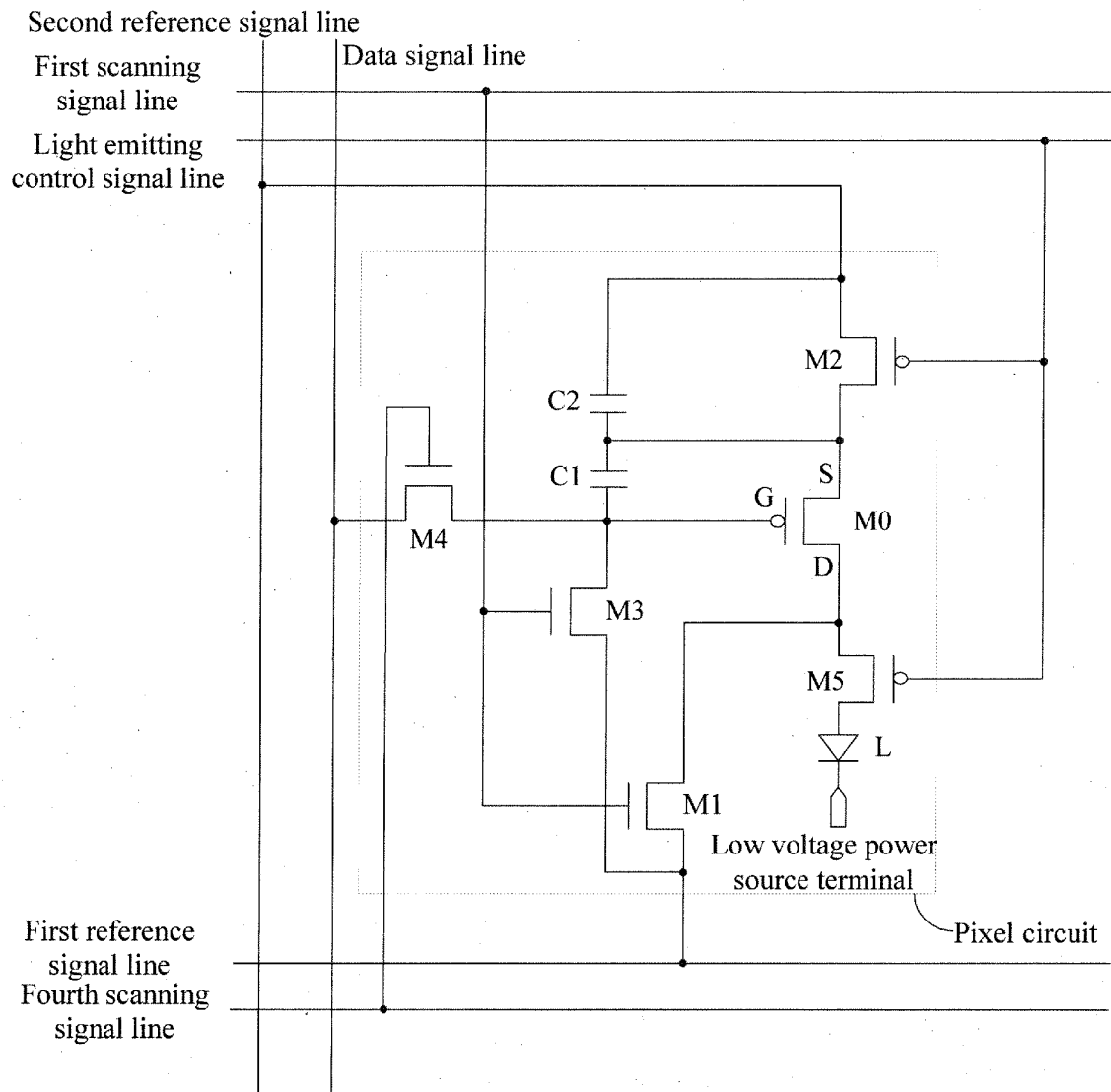


Fig. 8

INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2018/117758

A. CLASSIFICATION OF SUBJECT MATTER

G09G 3/3225(2016.01)i; G09G 3/3233(2016.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G09G

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNPAT, WPI, EPODOC, CNKI: 京东方, 董甜, 像素, 电路, 结构, 电容, 分压, 复位, 重置, 初始化, 源极, 漏极, 参考, 晶体管, 阈值, 补偿, 有机EL, 有机电致发光, 有机LED, 有机发光二极管, pixel, circuit, structure, emit+, capacit+, reset, initial+, electrode, source, drain, reference, Vref, OLED, TFT, threshold, compensate+, divid+, C2

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
PX	CN 108206008 A (BOE TECHNOLOGY GROUP CO., LTD.) 26 June 2018 (2018-06-26) description, paragraphs [0082]-[0210], and figures 1-8	1-28
X	CN 105427803 A (BOE TECHNOLOGY GROUP CO., LTD.) 23 March 2016 (2016-03-23) description, paragraphs [0103]-[0149], and figures 5-8	1-28
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☒ Further documents are listed in the continuation of Box C.
 ☒ See patent family annex.

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"A" document defining the general state of the art which is not considered to be of particular relevance	"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E" earlier application or patent but published on or after the international filing date	"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&" document member of the same patent family
"O" document referring to an oral disclosure, use, exhibition or other means	
"P" document published prior to the international filing date but later than the priority date claimed	

Date of the actual completion of the international search 31 January 2019	Date of mailing of the international search report 27 February 2019
Name and mailing address of the ISA/CN State Intellectual Property Office of the P. R. China No. 6, Xitucheng Road, Jimenqiao Haidian District, Beijing 100088 China	Authorized officer
Facsimile No. (86-10)62019451	Telephone No.

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2018/117758

C. DOCUMENTS CONSIDERED TO BE RELEVANT		
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INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.

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