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(54) **DISPLAY BACKPLATE AND MANUFACTURING METHOD THEREFOR, AND DISPLAY DEVICE**

ANZEIGERÜCKPLATTE UND HERSTELLUNGSVERFAHREN DAFÜR UND ANZEIGEVORRICHTUNG

PLAQUE ARRIÈRE D'AFFICHAGE ET SON PROCÉDÉ DE FABRICATION, ET DISPOSITIF D'AFFICHAGE

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Description

Related Applications

[0001] The present application claims the benefit of Chinese Patent Application No. 201510111902.7, filed on March 13, 2015.

FIELD OF THE INVENTION

[0002] The present invention relates to the field of display technology, and in particular to a display backplane and a manufacturing method thereof, as well as a display device.

BACKGROUND ART

[0003] Oxide backplanes have attracted wide attention for their excellent performances. However, the performances of oxide backplanes are sensitive to factors such as heat and light, and this problem is even more prominent for an AMOLED display screen made of an oxide backplane. Since an active-matrix organic light-emitting diode (AMOLED) is driven by current, the temperature of the oxide backplane will easily rise during lightening, which influences the performances of the oxide backplane and thus gives rise to problems such as decreased display brightness, a shortened service lifetime and large-size unevenness of display brightness.

[0004] EP 1 093 167 A2 relates to an EL display device, comprising: a substrate 11, an insulating film 12, a switching TFT 201, a current control TFT 202, and an EL element (including anode, 46, EL layer 47 and cathode 48), see figure 5 thereof, where the EL element is connected with the current control TFT 202 by a via hole passing through a passivation layer 41, an interlayer insulation layer 44 and a passivation layer 45.

[0005] US 2006/0022589 A1 relates to an OLED display, comprising: a substrate 12, a TFT active-matrix layer 14, a first electrode 18, a first heat insulating layer 16, a second heat insulating layer 17, an organic EL layer 19, a common second electrode 30, and an encapsulating or protective layer 31, see figure 2 thereof

[0006] US 2004/0085019 A1 relates to an OLED, comprising: a transparent substrate 61, a first electrode 62, an organic function layer 63, a second electrode 64, a covering component 65, and a heat-dissipating component 65 provided with a heat-dissipating pin 661, see figures 6-7 thereof.

[0007] US 2008/0197778 A1 relates to a light emitting device, comprising: a substrate, a light emitting element, an element layer, an auxiliary electrode, and an insulating layer.

[0008] US 2007/0029545 A1 relates to a vertical pixel architecture useful in display device, comprising a planarisation dielectric layer disposed between a thin-film transistors based backplane and an organic light emitting diodes device to planarise a vertical profile on the backplane.

SUMMARY

[0009] In regard to defects in the prior art, one goal of the present invention is to reduce the influence of heat generated by the OLED on the display backplane.

[0010] The present invention provides a display Z backplane as recited in claim 1.

[0011] The above display backplane provided according to the present invention has a heat insulation layer formed between the array of organic light emitting elements and the array of transistors, wherein the heat insulation layer is provided with a heat insulation layer via hole, through which the array of transistors is connected with the array of organic light emitting elements.

[0012] Thus, the conduction of heat generated by the array of organic light emitting elements during lighting to the array of transistors can be reduced, and accordingly problems caused thereby such as uneven display can be avoided.

[0013] Besides, with the slope angle as mentioned above, breakage of the bottom electrode of the organic light emitting element in the array of organic light emitting elements can be avoided.

[0014] According to embodiments of the present invention, the display backplane further optionally comprises: a passivation layer formed between the array of organic light emitting elements and the array of transistors, wherein

> the heat insulation layer is positioned between the passivation layer and the bottom electrode of the organic light emitting element in the array of organic light emitting elements; and
>
> the passivation layer is provided with a passivation layer via hole formed therein, the position of which corresponds to that of the heat insulation layer via hole, and the drain of the transistor in the array of transistors is connected with the bottom electrode of the organic light emitting element in the array of organic light emitting elements via the passivation layer via hole and the heat insulation layer via hole.

[0015] Thus, mutual interferences between the array of organic light emitting elements and the array of transistors are avoided by taking advantage of the passivation layer. Moreover, the formation of a corresponding passivation layer via hole ensures the connection between the array of transistors and the array of organic light emitting elements.

[0016] According to optional embodiments of the present invention, the slope angle of the heat insulation layer via hole is 40-60°.

[0017] According to optional embodiments of the present invention, the display backplane further comprises: a cover plate and a heat dissipation layer arranged on a side of the encapsulation layer away from the array of organic light emitting elements, wherein the cover plate is arranged between the heat dissipation layer and the encapsulation layer. Thereby, the dissipation of heat generated by the organic light emitting elements out from the display is further accelerated.

[0018] According to optional embodiments of the present invention, the heat dissipation layer comprises a heat dissipation sheet and a heat dissipation pin, the heat dissipation pin being formed on a side of the heat dissipation sheet away from the cover plate.

[0019] The present invention further provides a method for manufacturing a display backplane as recited in claim 6.

[0020] In a manner similar to the effect of the above display backplane provided in the present invention, with a display backplane manufactured using the above method of the present invention, the conduction of heat generated by the array of organic light emitting elements during lighting to the array of transistors can be reduced, and accordingly problems caused thereby such as uneven display can be avoided.

[0021] According to embodiments of the present invention, the method further comprises: forming a heat conduction layer on a side of the array of organic light emitting elements away from the array of transistors. Likewise, with this heat conduction layer, heat generated by the organic light emitting elements during lighting can be effectively conducted in a direction opposite to the array of the transistors, and influence of the heat generated by the organic light emitting elements on the performance of the active layer is further reduced

[0022] According to embodiments of the present invention, the method further comprises: forming an encapsulation layer for encapsulating the substrate on which the array of organic light emitting elements and the array of transistors are formed; wherein
the step of forming a heat conduction layer on a side of the array of organic light emitting elements away from the array of transistors comprises: forming a heat conduction layer between the array of organic light emitting elements and the encapsulation layer.

[0023] According to optional embodiments of the present invention, the method further comprises: forming a cover plate and a heat dissipation layer on a side of the encapsulation layer away from the array of organic light emitting elements, wherein the cover plate is formed between the heat dissipation layer and the encapsulation layer. Likewise, with the heat dissipation layer, the dissipation of heat generated by the organic light emitting elements out from the display is further accelerated.

[0024] According to optional embodiments of the present invention, the method further comprises: forming a passivation layer between the array of organic light emitting elements and the array of transistors, wherein

the heat insulation layer is positioned between the passivation layer and the bottom electrode of the organic light emitting element in the array of organic light emitting elements; and
the passivation layer is provided with a passivation layer via hole formed therein, the position of which corresponds to that of the heat insulation layer via hole, and the drain of the transistor in the array of transistors is connected with the bottom electrode of the organic light emitting element in the array of organic light emitting elements via the passivation layer via hole and the heat insulation layer via hole.

[0025] Thus, mutual interferences between the array of organic light emitting elements and the array of transistors are avoided, and moreover, by taking advantage of a corresponding passivation layer via hole, the connection between the array of transistors and the array of organic light emitting elements is ensured

[0026] Furthermore, the step of forming the heat insulation layer may comprise:

coating a mixed material of a heat insulation material and a photoresist onto the passivation layer; and

exposing and developing the mixed material coated onto the passivation layer using a photolithography process, to form a heat insulation layer provided with a heat insulation layer via hole.

[0027] The present invention further provides a display device, comprising the above display backplane as recited in claim

[0028] The technical problem solved by the display device and its related effects are the same as those of the display backplane and the manufacturing method thereof as mentioned above, so no more details shall be described herein for simplicity.

BRIEF DESCRIPTION OF DRAWINGS

[0029]

Fig. 1 is a schematic structural view of a display backplane provided according to embodiments of the present invention; and

Fig. 2 is a schematic view of a possible structure for the heat dissipation layer 16 in Fig. 1.

DETAILED DESCRIPTION OF EMBODIMENTS

[0030] To render the goal of the embodiments of the present invention, the technical solution and the advantages thereof even clearer, the technical solutions according to embodiments of the present invention shall be described as follows in a clear and complete manner with reference to the drawings in the embodiments of the present invention. Obviously, the embodiments described here are only a part of the embodiments of the present invention, rather than all of them.

[0031] Since a heat insulation layer is formed between the array of organic light emitting elements and the array of transistors, and the heat insulation layer is provided with a heat insulation layer via hole, through which the array of transistors is connected with the array of organic light emitting elements, in this case, the conduction of heat generated by the array of organic light emitting elements during lighting to the array of transistors can be reduced, and accordingly problems caused thereby such as uneven display can be avoided.

[0032] Fig. 1 is a schematic structural view of a display backplane provided according to embodiments of the present invention, wherein the display backplane comprises:

glass substrate 1; a gate electrode pattern 2 formed on the glass substrate 1; a gate insulation layer 3 formed over the gate electrode pattern 2 and the glass substrate 1; an active layer pattern 4 formed over the gate insulation layer 3; a source-drain electrode pattern 5 formed over the active layer pattern 4; a passivation layer 6 formed over the active layer pattern 4 and the source-drain electrode pattern 5; a heat insulation layer 7 formed over the passivation layer 6; a resin layer 8 formed over the heat insulation layer 7; a pixel defining layer pattern 9, a bottom electrode pattern 10, a light emitting layer pattern 11 and a top electrode pattern 12 formed over the resin layer 8; a heat conduction layer 13 formed over the pixel defining layer pattern 9 and the top electrode pattern 12; an encapsulation layer 14 formed over the heat conduction layer 13; cover plate glass 15 formed on the encapsulation layer 14; and a heat dissipation layer 16 formed over the cover plate glass 15. In this case, the active layer pattern 4 can be formed from semiconductor materials such as metal oxides, polycrystalline silicon, amorphous silicon and the like; correspondingly, a passivation layer via hole, a heat insulation layer via hole and a resin layer via hole are formed respectively in the passivation layer 6, the heat insulation layer 7 and the resin layer 8, the positions of the passivation layer via hole, the heat insulation layer via hole and the resin layer via hole corresponding with each other, and the top electrode pattern 12 is connected with the source-drain electrode pattern 5 via the above via holes having corresponding positions. The gate electrode pattern 2, the gate insulation layer 3, the active layer pattern 4 and the source-drain electrode pattern 5 here together form an array of transistors, and the bottom electrode pattern 10, the light emitting layer pattern 11 and the top electrode pattern 12 together form an array of organic light emitting elements. Glass substrate 1 is an instance for the substrate. Besides, the substrate can be formed from materials such as transparent resin, quartz, sapphire and the like, which will not be limited in the present invention.

[0033] According to optional embodiments of the present invention, since the heat insulation layer 7 is formed between the passivation layer 6 and the bottom electrode pattern 10, the influence of heat generated by the organic light emitting elements during lighting on the performance of the array of transistors can be effectively avoided, and accordingly problems caused thereby such as uneven display brightness can be avoided. Meanwhile, according to embodiments of the present invention, since a heat conduction layer 13 is further formed over the top electrode pattern 12, heat generated by the organic light emitting elements during lighting can be effectively conducted in a direction opposite to the array of transistors, and hence the influence of heat generated by the organic light emitting elements during lighting on the performance of the active layer is further reduced. On the other hand, according to optional embodiments of the present invention, a heat dissipation layer 16 is further formed outside the cover plate glass 15, which can also further accelerate the dissipation of heat generated by the organic light emitting elements out form the display.

[0034] It should be noted that although Fig. 1 shows a situation where the heat insulation layer 7 is formed between the passivation layer 6 and the resin layer 8, the position of the heat insulation layer 7 is not limited thereto in an actual application. For example, the heat insulation layer can also be arranged between the resin layer 8 and the bottom electrode pattern 10, or the passivation layer 6 or the resin layer 8 can also be formed from a material having heat insulation function. As long as the heat insulation layer is arranged between the array of transistors and the array of organic light emitting elements such that respective solutions can all achieve the goal of reducing the influence of heat generated by the organic light emitting elements on the performance of the active layer, the corresponding technical solutions shall all fall within the protection scope of the present invention. In addition, structures such as a passivation layer, a resin layer and a pixel defining layer pattern are not necessarily present as they can be added or deleted upon the actual or design need. In specific implementations, when only the heat insulation layer 7 is arranged without the heat dissipation layer 16 in Fig. 1, such a technical solution can also reduce to a certain degree the influence of heat generated by the organic light emitting elements on the performance of the active layer, so the corresponding technical solution shall also fall within the protection scope of the present invention.

[0035] In an actual application, the heat insulation layer 7 here can consist of one or more materials with a low thermal conductivity. The material of the heat insulation layer has a thermal conductivity of 0-0.8 W/mK, such as polystyrene (the thermal conductivity of which is 0.08 W/mK) . The thickness of the heat insulation layer 7 can be 1-2μm. In specific implementations, the heat insulation layer 7 here can be made by coating, evaporation or the like.

[0036] According to the invention as claimed, in order to avoid breakage of the bottom electrode pattern 10, the slope angle of the heat insulation layer via hole is arranged as smaller than or equal to 60°. For instance, in WOLED + COA (White OLED + Color filter On Array), if the heat insulation layer 7 is arranged between the passivation layer 6 and a color film layer, the slope angle of the heat insulation layer via hole is arranged as smaller than or equal to 60° if the heat insulation layer 7 is arranged over the resin layer 8 and d between the bottom electrode pattern 10, the slope angle of the heat insulation layer via hole can be arranged as between 40-60°. Besides, in a PLED structure (a P-type LED), the heat insulation layer 7 can be deposited between the passivation layer 6 and the bottom electrode pattern 10, wherein the slope angle of the via hole is 40-60°.

[0037] When the above display backplane is a bottom emission type display backplane, the light transmittance of the heat insulation layer 7 can be arranged as greater than or equal to 95% so as to ensure the transmittance of the display backplane.

[0038] The material of the heat conduction layer 13 may have a thermal conductivity of 100W/mK to 8000W/mK. For instance, it can consist of one or more materials with a high thermal conductivity, such as silver, copper, gold, aluminum, diamond, graphite, graphene, carbon nanotube and so on. The thickness of the heat conduction layer 13 can be 1-100μm. The above materials can be deposited over the top electrode pattern 12 by sputtering, evaporation, coating or the like to form the heat conduction layer 13.

[0039] In an actual application, the material of the heat dissipation layer 16 can have a thermal conductivity of greater than 100W/mK. For example, it can be one or more chosen from the following materials: silver, copper, gold, aluminum, diamond, graphite, grapheme, carbon nanotube and so on.

[0040] As shown in Fig. 2, the heat dissipation layer 16 has a heat dissipation sheet 16a and a heat dissipation pin 16b, the heat dissipation pin 16b being formed on a side of the heat dissipation sheet 16a away from the cover plate glass 14. Such a structure has a better heat dissipation effect.

[0041] In specific implementations, the heat dissipation pin here has a height of at least 1mm, and a width in a range of 1-5mm, and the distance between adjacent heat dissipation pins 16b can be in a range of 2-5mm.

[0042] In specific implementations, materials with a thermal conductivity of greater than 100W/mK can be chosen as the material of the heat dissipation layer, for example, one or more from the group consisting of silver, copper, gold, aluminum, diamond, graphite, grapheme, carbon nanotube and so on. The heat dissipation pin 16b may have different shapes and a larger surface area so as to dissipate heat more quickly. The heat dissipation pin 16b can be made by an etching process.

[0043] In specific implementations, the above display backplane can be either a bottom emission type display backplane or a top emission type display backplane. Fig. 1 shows a situation where it is a bottom emission type display backplane, the bottom electrode pattern 10 here can be an anode, and the corresponding top electrode pattern 12 is a cathode; or, the bottom electrode pattern 10 is a cathode, and the corresponding top electrode pattern 12 is an anode. Besides, the above display backplane can be a WOLED backplane, a PLED backplane and the like as mentioned above.

[0044] In specific implementations, the above heat insulation layer via hole, the passivation layer via hole and the resin layer via hole can be made by photolithography. Furthermore, the aperture of the heat insulation layer via hole can be arranged as greater than that of the passivation layer via hole, and the aperture of the resin layer can be arranged as greater than that of the heat insulation layer via hole.

[0045] In some applications, the above resin layer 8 is not an indispensable structure.

[0046] A further embodiment of the present invention also provides a method for manufacturing a display backplane as recited in claim 6.

[0047] In specific implementations, the array of oxide transistors and the array of organic light emitting elements can be formed with reference to the prior art, and a heat insulation layer pattern can be formed between the array of oxide transistors and the array of organic light emitting elements which have been formed. Specifically, a gate electrode pattern, a gate insulation layer, an oxide active layer pattern, a source-drain electrode pattern and a passivation layer can be formed on the substrate sequentially. Then a heat insulation layer pattern is formed over the passivation layer. After the formation of the heat insulation layer pattern, a resin layer, a bottom electrode pattern, a light emitting layer and a top electrode pattern are formed sequentially. If the display backplane to be manufactured is a top emission type display backplane, a reflective layer should also be formed prior to the formation of the gate electrode pattern.

[0048] In specific optional implementations, when the heat insulation layer pattern is formed directly on the passivation layer, the step of forming a heat insulation layer pattern and a passivation layer pattern can comprise:

forming a passivation layer;

mixing a heat insulation material with a photoresist in a certain proportion and then coating the mixture onto the passivation layer; and

exposing and developing the mixed material layer coated onto the passivation layer using a same mask plate by a photolithography process to form a pattern of the heat insulation layer via hole, and then forming a passivation layer via hole by dry etching.

[0049] The passivation layer via hole formed in the above manner can have a smaller slope angle, thereby avoiding breakage of the bottom electrode pattern.

[0050] Furthermore, the above method further comprises: forming a heat conduction layer on a side of the array of organic light emitting elements away from the array of oxide transistors. The heat conduction layer here can be formed on a surface of the top electrode pattern by sputtering, evaporation, coating or the like.

[0051] Furthermore, the above method further comprises: forming an encapsulation layer for encapsulating the substrate on which the array of organic light emitting elements and the array of oxide transistors are formed.

[0052] According to the invention, the step of forming a heat conduction layer on a side of the array of organic light emitting elements away from the array of oxide transistors comprises:

forming a heat conduction layer between the array of organic light emitting elements and the encapsulation layer.

[0053] Furthermore, the method can further comprise: forming a cover plate and a heat dissipation layer on a side of the encapsulation layer away from the array of organic light emitting elements, wherein the cover plate is formed between the heat dissipation layer and the encapsulation layer.

[0054] In specific implementations, the heat dissipation layer here can be made from a thermally conductive material, and the structure of the heat dissipation layer formed here can be identical to that shown in Fig. 2. Here, the heat dissipation pin therein can be made by an etching process, and the height of the heat dissipation pin can be controlled by controlling the etching time.

[0055] It should be noted that although descriptions are provided in the above embodiments by taking the transistors in the display backplane as oxide transistors, in an actual application, the solution provided in the present invention can also achieve similar effects in a display backplane comprising transistors of other types. Therefore, the corresponding technical solutions shall also fall within the protection scope of the present invention.

[0056] A further embodiment of the present invention further provides a display device comprising any one of the above display backplanes. The display device can be any product or component having a display function, including: an OLED panel, a cell phone, a tablet computer, a television, a display, a notebook computer, a digital photo frame, a navigator and so on.

[0057] The above contents are only specific embodiments of the present invention, but the protection scope of the present invention shall not be limited thereto. The invention is defined by the appended claims.

Claims

1. A display backplane, comprising:

   a substrate (1);
   an array of organic light emitting elements and an array of transistors for driving and controlling the array of organic light emitting elements formed on the substrate (1);
   a heat insulation layer (7) formed between the array of organic light emitting elements and the array of transistors,
   wherein the heat insulation layer (7) is provided with a heat insulation layer via hole, through which the array of transistors is connected with the array of organic light emitting elements, and wherein the slope angle of a side of the heat insulation layer via hole with respect to an extending plane of the heat insulation layer (7) is smaller than or equal to 60°,
   characterised by
   a heat conduction layer (13) formed on a side of the array of the organic light emitting elements away from the array of the transistors,
   an encapsulation layer (14) for encapsulating the substrate (1) on which the array of organic light emitting elements and the array of transistors are formed, wherein the heat conduction layer (13) is formed between the array of organic light emitting elements and the encapsulation layer (14), and
   a thermal conductivity of the heat insulation layer (7) being 0-0.08 W/mK.

2. The display backplane according to claim 1, further comprising: a passivation layer (6) formed between the array of organic light emitting elements and the array of transistors, wherein

   the heat insulation layer (7) is positioned between the passivation layer (6) and a bottom electrode (10) of the organic light emitting element in the array of organic light emitting elements; and
   the passivation layer (6) is provided with a passivation layer via hole formed therein, the position of which corresponds to that of the heat insulation layer via hole, and the drain (5) of the transistor in the array of transistors is connected with the bottom electrode (10) of the organic light emitting element in the array of organic light emitting elements via the passivation layer via hole and the heat insulation layer via hole.

3. The display backplane according to claim 1, wherein the slope angle of the side of the heat insulation layer via hole with respect to the extending plane of the heat insulation layer (7) is 40-60°.

4. The display backplane according to claim 1, further comprising: a cover plate (15) and a heat dissipation layer (16) arranged on a side of the encapsulation layer (14) away from the array of organic light emitting elements, wherein the cover plate (15) is arranged between the heat dissipation layer (16) and the encapsulation layer (14).

5. The display backplane according to claim 4, wherein the heat dissipation layer (16) comprises a heat dis-

sipation sheet (16a) and a heat dissipation pin (16b), the heat dissipation pin (16b) being formed on a side of the heat dissipation sheet (16a) away from the cover plate (15).

6. A method for manufacturing a display backplane, comprising:

forming on a substrate (1) an array of organic light emitting elements and an array of transistors for driving and controlling the array of organic light emitting elements;
forming a heat insulation layer (7) between the array of organic light emitting elements and the array of transistors,
forming a heat conduction layer (13) on a side of the array of organic light emitting elements away from the array of transistors, and
forming an encapsulation layer (14) for encapsulating the substrate (1) on which the array of organic light emitting elements and the array of transistors are formed, the heat conduction layer (13) being formed between the array of organic light emitting elements and the encapsulation layer (14), wherein
the heat insulation layer (7) is provided with a heat insulation layer via hole formed therein, through which the array of transistors is connected with the array of organic light emitting elements,
the slope angle of a side of the heat insulation layer via hole with respect to an extending plane of the heat insulation layer (7) is smaller than or equal to 60°, and
a thermal conductivity of the heat insulation layer (7) is 0-0.08 W/mK.

7. The method according to claim 6, further comprising: forming a cover plate (15) and a heat dissipation layer (16) on a side of the encapsulation layer (14) away from the array of organic light emitting elements, wherein the cover plate (15) is formed between the heat dissipation layer (16) and the encapsulation layer (14).

8. The method according to claim 6, further comprising: forming a passivation layer (6) between the array of organic light emitting elements and the array of transistors, wherein

the heat insulation layer (7) is positioned between the passivation layer (6) and a bottom electrode (10) of the organic light emitting element in the array of organic light emitting elements; and
the passivation layer (6) is provided with a passivation layer via hole formed therein, the position of which corresponds to that of the heat insulation layer via hole, and the drain (5) of the transistor in the array of transistors is connected with the bottom electrode (10) of the organic light emitting element in the array of organic light emitting elements via the passivation layer via hole and the heat insulation layer via hole.

9. The method according to claim 8, wherein the step of forming the heat insulation layer (7) comprises:

coating a mixed material of a heat insulation material and a photoresist onto the passivation layer (6); and
exposing and developing the mixed material coated onto the passivation layer (6) using a photolithography process, to form a heat insulation layer (7) provided with a heat insulation layer via hole.

10. A display device, comprising the display backplane according to any one of claims 1-5.

Patentansprüche

1. Anzeigerückwand, umfassend:

ein Substrat (1);
eine Gruppierung von organischen lichtemittierenden Elementen und eine Gruppierung von Transistoren zum Antreiben und Steuern der Gruppierung von organischen lichtemittierenden Elementen, die auf dem Substrat (1) gebildet sind;
eine Wärmeisolationsschicht (7), die zwischen der Gruppierung der organischen lichtemittierenden Elemente und der Gruppierung der Transistoren gebildet ist,
wobei die Wärmeisolationsschicht (7) mit einem Durchkontaktierungsloch der Wärmeisolationsschicht ausgestattet ist, durch welches die Gruppierung der Transistoren mit der Gruppierung der organischen lichtemittierenden Elemente verbunden wird, und
wobei der Neigungswinkel einer Seite des Durchkontaktierungslochs der Wärmeisolationsschicht in Bezug auf eine sich erstreckende Ebene der Wärmeisolationsschicht (7) kleiner als oder gleich 60° ist,
gekennzeichnet durch eine Wärmeleitungsschicht (13), die auf einer Seite der Gruppierung der organischen lichtemittierenden Elemente gebildet ist, die von der Gruppierung der Transistoren weg weist,
eine Verkapselungsschicht (14) zum Verkapseln des Substrats (1), auf welchem die Gruppierung der organischen lichtemittierenden Elemente und die Gruppierung der Transistoren ge-

bildet sind, wobei die Wärmeleitungsschicht (13) zwischen der Gruppierung der organischen lichtemittierenden Elemente und der Verkapselungsschicht (14) gebildet ist, und
eine Wärmeleitfähigkeit der Wärmeisolationsschicht (7) zwischen 0 und 0,08 W/mK liegt.

2. Anzeigerückwand nach Anspruch 1, des Weiteren umfassend:

eine Passivierungsschicht (6), die zwischen der Gruppierung der organischen lichtemittierenden Elemente und der Gruppierung von Transistoren gebildet ist, wobei
die Wärmeisolationsschicht (7) zwischen der Passivierungsschicht (6) und einer Bodenelektrode (10) des organischen lichtemittierenden Elements in der Gruppierung der organischen lichtemittierenden Elemente positioniert ist; und
die Passivierungsschicht (6) mit einem darin gebildeten Durchkontaktierungsloch der Passivierungsschicht ausgestattet ist, dessen Position derjenigen des Durchkontaktierungslochs der Wärmeisolationsschicht entspricht, und das Drain (5) des Transistors in der Gruppierung der Transistoren mit der Bodenelektrode (10) des organischen lichtemittierenden Elements in der Gruppierung der organischen lichtemittierenden Elemente über das Durchkontaktierungsloch der Passivierungsschicht und das Durchkontaktierungsschicht der Wärmeisolationsschicht verbunden ist.

3. Anzeigerückwand nach Anspruch 1, wobei der Neigungswinkel der Seite des Durchkontaktierungslochs der Wärmeisolationsschicht in Bezug auf die sich erstreckende Ebene der Wärmeisolationsschicht (7) 40 bis 60° beträgt.

4. Anzeigerückwand nach Anspruch 1, des Weiteren umfassend:

eine Abdeckplatte (15) und eine Wärmeabfuhrschicht (16), die auf einer Seite der Verkapselungsschicht (14) angeordnet sind, die von der Gruppierung der organischen lichtemittierenden Elemente weg weist,
wobei die Abdeckplatte (15) zwischen der Wärmeabfuhrschicht (16) und der Verkapselungsschicht (14) angeordnet ist.

5. Anzeigerückwand nach Anspruch 4, wobei die Wärmeabfuhrschicht (16) eine Wärmeabfuhrlage (16a) und einen Wärmeabfuhrstift (16b) umfasst, wobei der Wärmeabfuhrstift (16b) auf einer Seite der Wärmeabfuhrlage (16a) gebildet ist, die von der Abdeckplatte (15) weg weist.

6. Verfahren zum Fertigen einer Anzeigerückwand, umfassend:

Bilden einer Gruppierung von organischen lichtemittierenden Elementen und einer Gruppierung von Transistoren zum Antreiben und Steuern der Gruppierung von organischen lichtemittierenden Elementen auf einem Substrat (1);
Bilden einer Wärmeisolationsschicht (7) zwischen der Gruppierung der organischen lichtemittierenden Elemente und der Gruppierung der Transistoren,
Bilden einer Wärmeleitungsschicht (13) auf einer Seite der Gruppierung der organischen lichtemittierenden Elemente, die von der Gruppierung der Transistoren weg weist, und
Bilden einer Verkapselungsschicht (14) zum Verkapseln des Substrats (1), auf welchem die Gruppierung der organischen lichtemittierenden Elemente und die Gruppierung der Transistoren gebildet sind, wobei die Wärmeleitungsschicht (13) zwischen der Gruppierung der organischen lichtemittierenden Elemente und der Verkapselungsschicht (14) gebildet ist, wobei
die Wärmeisolationsschicht (7) mit einem darin gebildeten Durchkontaktierungsloch der Wärmeisolationsschicht bereitgestellt wird, durch welches die Gruppierung der Transistoren mit der Gruppierung der organischen lichtemittierenden Elemente verbunden wird,
der Neigungswinkel einer Seite des Durchkontaktierungslochs der Wärmeisolationsschicht in Bezug auf eine sich erstreckende Ebene der Wärmeisolationsschicht (7) kleiner als oder gleich 60° ist, und
eine Wärmeleitfähigkeit der Wärmeisolationsschicht (7) zwischen 0 und 0,08 W/mK liegt.

7. Verfahren nach Anspruch 6, des Weiteren umfassend: Bilden einer Abdeckplatte (15) und einer Wärmeabfuhrschicht (16) auf einer Seite der Verkapselungsschicht (14), die von der Gruppierung der organischen lichtemittierenden Elemente weg weist, wobei die Abdeckplatte (15) zwischen der Wärmeabfuhrschicht (16) und der Verkapselungsschicht (14) gebildet wird.

8. Verfahren nach Anspruch 6, des Weiteren umfassend:

Bilden einer Passivierungsschicht (6) zwischen der Gruppierung der organischen lichtemittierenden Elemente und der Gruppierung von Transistoren, wobei
die Wärmeisolationsschicht (7) zwischen der Passivierungsschicht (6) und einer Bodenelektrode (10) des organischen lichtemittierenden Elements in der Gruppierung der organischen

lichtemittierenden Elemente positioniert ist; und die Passivierungsschicht (6) mit einem darin gebildeten Durchkontaktierungsloch der Passivierungsschicht ausgestattet ist, dessen Position derjenigen des Durchkontaktierungslochs der Wärmeisolationsschicht entspricht, und das Drain (5) des Transistors in der Gruppierung der Transistoren mit der Bodenelektrode (10) des organischen lichtemittierenden Elements in der Gruppierung der organischen lichtemittierenden Elemente über das Durchkontaktierungsloch der Passivierungsschicht und das Durchkontaktierungsschicht der Wärmeisolationsschicht verbunden ist.

9. Verfahren nach Anspruch 8, wobei der Schritt des Bildens der Wärmeisolationsschicht (7) umfasst:

Aufbringen einer Beschichtung eines gemischten Materials aus einem Wärmeisolationsmaterial und einem Photoresist auf die Passivierungsschicht (6); und

Belichten und Entwickeln des gemischten Materials, das als Beschichtung auf die Passivierungsschicht (6) aufgebracht worden ist, unter Verwendung eines Photolithographieprozesses, um eine Wärmeisolationsschicht (7) zu bilden, die mit einem Durchkontaktierungsloch der Wärmeisolationsschicht ausgestattet ist.

10. Anzeigevorrichtung, welche die Anzeigerückwand nach einem der Ansprüche 1 bis 5 umfasst.

Revendications

1. Fond de panier d'écran, comprenant :

un substrat (1) ;

une matrice d'éléments émetteurs de lumière organiques et une matrice de transistors pour exciter et commander la matrice d'éléments émetteurs de lumière organiques formées sur le substrat (1) ;

une couche d'isolation thermique (7) formée entre la matrice d'éléments émetteurs de lumière organiques et la matrice de transistors,

la couche d'isolation thermique (7) étant pourvue d'un trou d'interconnexion de couche d'isolation thermique, par lequel la matrice de transistors est reliée à la matrice d'éléments émetteurs de lumière organiques, et

l'angle d'inclinaison d'un côté du trou d'interconnexion de couche d'isolation thermique par rapport à un plan d'extension de la couche d'isolation thermique (7) est inférieur ou égal à 60°,

caractérisé par

une couche de conduction thermique (13) formée sur un côté de la matrice des éléments émetteurs de lumière organiques à l'opposé de la matrice des transistors,

une couche d'encapsulation (14) pour encapsuler le substrat (1) sur lequel sont formées la matrice d'éléments émetteurs de lumière organiques et la matrice de transistors, la couche de conduction thermique (13) étant formée entre la matrice d'éléments émetteurs de lumière organiques et la couche d'encapsulation (14), et

une conductivité thermique de la couche d'isolation thermique (7) qui est de 0-0,08 W/mK.

2. Fond de panier d'écran selon la revendication 1, comprenant en outre une couche de passivation (6) formée entre la matrice d'éléments émetteurs de lumière organiques et la matrice de transistors, dans lequel

la couche d'isolation thermique (7) est positionnée entre la couche de passivation (6) et une électrode inférieure (10) de l'élément émetteur de lumière organique dans la matrice d'éléments émetteurs de lumière organiques ; et

la couche de passivation (6) est pourvue d'un trou d'interconnexion de couche de passivation formé à l'intérieur, dont la position correspond à celle du trou d'interconnexion de couche d'isolation thermique, et le drain (5) du transistor dans la matrice de transistors est relié à l'électrode inférieure (10) de l'élément émetteur de lumière organique dans la matrice d'éléments émetteurs de lumière organiques par le biais du trou d'interconnexion de couche de passivation et du trou d'interconnexion de couche d'isolation thermique.

3. Fond de panier d'écran selon la revendication 1, dans lequel l'angle d'inclinaison du côté du trou d'interconnexion de couche d'isolation thermique par rapport au plan d'extension de la couche d'isolation thermique (7) est de 40-60°.

4. Fond de panier d'écran selon la revendication 1, comprenant en outre une plaque de recouvrement (15) et une couche de dissipation thermique (16) disposées sur un côté de la couche d'encapsulation (14) à l'opposé de la matrice d'éléments émetteurs de lumière organiques, la plaque de recouvrement (15) étant disposée entre la couche de dissipation thermique (16) et la couche d'encapsulation (14).

5. Fond de panier d'écran selon la revendication 4, dans lequel la couche de dissipation thermique (16) comprend une feuille de dissipation thermique (16a) et une broche de dissipation thermique (16b), la broche de dissipation thermique (16b) étant formée sur un côté de la feuille de dissipation thermique (16a) à l'opposé de la plaque de recouvrement (15).

6. Procédé de fabrication d'un fond de panier d'écran, comprenant :

la formation, sur un substrat (1), d'une matrice d'éléments émetteurs de lumière organiques et d'une matrice de transistors pour exciter et commander la matrice d'éléments émetteurs de lumière organiques ;
la formation d'une couche d'isolation thermique (7) entre la matrice d'éléments émetteurs de lumière organiques et la matrice de transistors ;
la formation d'une couche de conduction thermique (13) sur un côté de la matrice d'éléments émetteurs de lumière organiques à l'opposé de la matrice de transistors ; et
la formation d'une couche d'encapsulation (14) pour encapsuler le substrat (1) sur lequel sont formées la matrice d'éléments émetteurs de lumière organiques et la matrice de transistors, la couche de conduction thermique (13) étant formée entre la matrice d'éléments émetteurs de lumière organiques et la couche d'encapsulation (14), dans lequel
la couche d'isolation thermique (7) est pourvue d'un trou d'interconnexion de couche d'isolation thermique formé à l'intérieur, par lequel la matrice de transistors est reliée à la matrice d'éléments émetteurs de lumière organiques,
l'angle d'inclinaison d'un côté du trou d'interconnexion de couche d'isolation thermique par rapport à un plan d'extension de la couche d'isolation thermique (7) est inférieur ou égal à 60°, et
une conductivité thermique de la couche d'isolation thermique (7) est de 0-0,08 W/mK.

7. Procédé selon la revendication 6, comprenant en outre :
la formation d'une plaque de recouvrement (15) et d'une couche de dissipation thermique (16) sur un côté de la couche d'encapsulation (14) à l'opposé de la matrice d'éléments émetteurs de lumière organiques, la plaque de recouvrement (15) étant formée entre la couche de dissipation thermique (16) et la couche d'encapsulation (14).

8. Procédé selon la revendication 6, comprenant en outre la formation d'une couche de passivation (6) entre la matrice d'éléments émetteurs de lumière organiques et la matrice de transistors, dans lequel

la couche d'isolation thermique (7) est positionnée entre la couche de passivation (6) et une électrode inférieure (10) de l'élément émetteur de lumière organique dans la matrice d'éléments émetteurs de lumière organiques ; et
la couche de passivation (6) est pourvue d'un trou d'interconnexion de couche de passivation formé à l'intérieur, dont la position correspond à celle du trou d'interconnexion de couche d'isolation thermique, et le drain (5) du transistor dans la matrice de transistors est relié à l'électrode inférieure (10) de l'élément émetteur de lumière organique dans la matrice d'éléments émetteurs de lumière organiques par le biais du trou d'interconnexion de couche de passivation et du trou d'interconnexion de couche d'isolation thermique.

9. Procédé selon la revendication 8, dans lequel l'étape de formation de la couche d'isolation thermique (7) comprend :

le dépôt d'un matériau mixte composé d'un matériau d'isolation thermique et d'une résine photosensible sur la couche de passivation (6) ; et
l'exposition et le développement du matériau mixte déposé sur la couche de passivation (6) par un procédé photolithographique, pour former une couche d'isolation thermique (7) pourvue d'un trou d'interconnexion de couche d'isolation thermique.

10. Dispositif d'affichage, comprenant le fond de panier d'écran selon l'une quelconque des revendications 1 à 5.

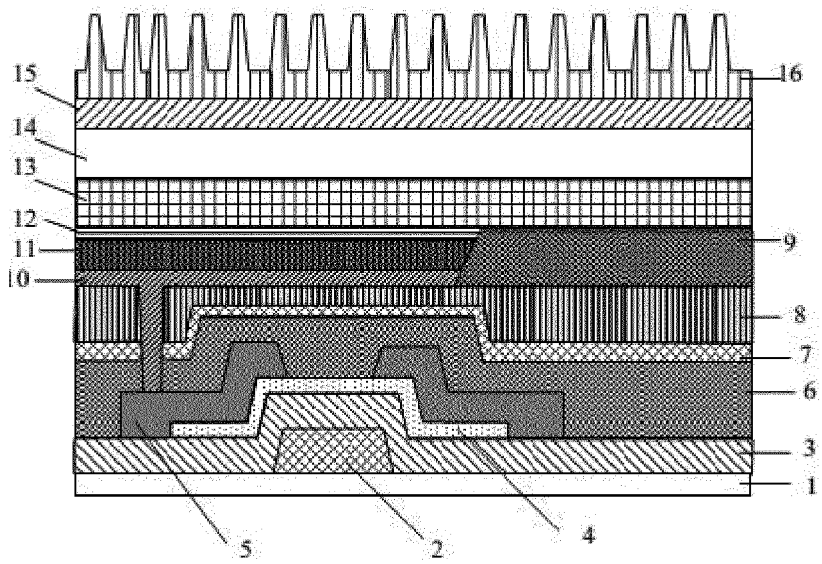

Fig. 1

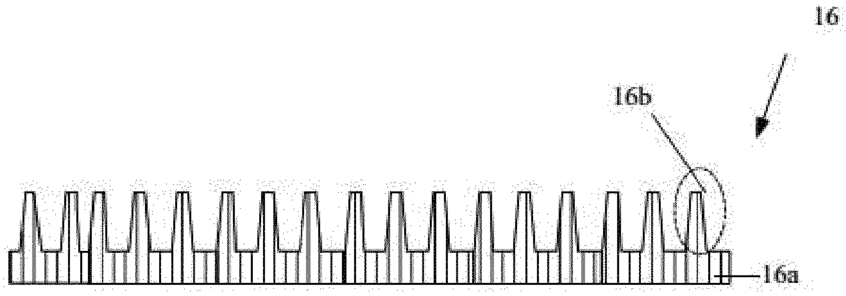

Fig. 2

REFERENCES CITED IN THE DESCRIPTION

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