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(54) PIXEL CIRCUIT, ORGANIC ELECTROLUMINESCENT DISPLAY PANEL AND DISPLAY APPARATUS

PIXELSCHALTUNG, ORGANISCHE ELEKTROLUMINESZENTE ANZEIGETAFEL UND ANZEIGEVORRICHTUNG

CIRCUIT DE PIXEL, PANNEAU D'AFFICHAGE ÉLECTROLUMINESCENT ORGANIQUE ET APPAREIL D'AFFICHAGE

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Description

TECHNICAL FIELD

[0001] The present disclosure relates to a pixel circuit, an organic light emitting display panel and display apparatus.

BACKGROUND

[0002] An organic light emitting display (OLED) is one of hot topics in the research field of flat panel display. Compared with a liquid crystal display, OLED has advantages of low power consumption, low production cost, self-luminescent, broad view angle and fast response speed and so on. At present, in the display field such as mobile phone, PDA and digital camera and the like, OLED has taken the place of the traditional LCD display screen. Unlike that LCD controls luminance by using a stable voltage, OLED is current-driven and a stable current is required to control light emitting.

[0003] At present, for a known pixel circuit that drives OLED to emit light, due to manufacturing processes, device aging and so on, non-uniformity exists in a threshold voltage of a driving transistor of a pixel circuit, thereby resulting in that a change occurs in the current flowing through OLED of each pixel point such that display luminance is non-uniform, which influences display effect of the entire image.

[0004] Therefore, how to ensure the uniformity of the current for driving the light emitting device OLED in the display apparatus so as to ensure the quality of the display picture is an urgent problem to be solved by those skilled in the art.

US 2010/079361 A1 discloses a pixel of a display device wherein a first transistor of which a second terminal is connected to a first terminal of a light emitting element supplies a driving current that corresponds to a voltage between a control terminal and the second terminal to the light emitting elements, and a second terminal of the light emitting element is connected to a driving voltage. At least one second transistor transmits a black voltage that corresponds to a black gray to the control terminal of the first transistor in a first period and a second period, and transmits a gray voltage that corresponds to an input image signal to the control terminal of the first transistor in a third period. A third transistor is connected between the first terminal of the light emitting element and a voltage supply line to transmit a reference voltage, and the third transistor is turned on in the first period and turned off in the second period. A capacitor between the control terminal and the source of the first transistor, stores a control voltage based on a threshold voltage of the first transistor in the second period, and stores a voltage based on the control voltage and the gray voltage in the third period. Document US20130050292A1 discloses an OLED circuit with a monitoring of the OLED anode via an additional transistor connected to the data line.

SUMMARY

[0005] There is provided in embodiments of the present disclosure a pixel circuit, an organic light emitting display panel and a display apparatus, which are used to solve the problem existing in the prior art that a current for driving a light emitting device OLED in the display apparatus has poor uniformity and display luminance is non-uniform.

[0006] The invention is defined in claim 1.

[0007] In a possible implementation, in the pixel circuit provided in the embodiment of the present disclosure, the testing module can comprise: a first switching transistor, and a second switching transistor and a third switching transistor which have a same doping polarity; and the first switching transistor has a doping polarity inverse to the second switching transistor and the third switching transistor respectively;

wherein a gate of the first switching transistor, a gate of the second switching transistor and a gate of the third switching transistor are connected to the test signal respectively;

a source of the first switching transistor and a source of the third switching transistor are connected to the second terminal of the light emitting device respectively;

a drain of the first switching transistor and a source of the second switching transistor are connected to the second terminal of the charging module;

a drain of the second switching transistor is connected to the control terminal of the driving module; and

a drain of the third switching transistor is connected to the second reference signal.

[0008] In a possible implementation, in the pixel circuit provided in the embodiment of the present disclosure, the charging module can comprise a fourth switching transistor;

wherein a gate of the fourth switching transistor is connected to the scan signal, a source of the fourth switching transistor is connected to the data signal, and a drain of the fourth switching transistor is connected to the first terminal and the third terminal of the testing module.

[0009] In a possible implementation, in the pixel circuit provided in the embodiment of the present disclosure, the driving module can comprise: a storage capacitor and a fifth switching transistor;

wherein a source of the fifth switching transistor is connected to the first reference signal, a gate of the fifth switching transistor is connected to the fourth terminal of the testing module, and a drain of the fifth switching transistor is connected to the first terminal of the light emitting device;

when the fifth switching transistor is a P type transistor, the storage capacitor is connected in parallel between the source and the gate of the fifth switching

transistor; and
when the fifth switching transistor is an N type transistor, the storage capacitor is connected in parallel between the drain and the gate of the fifth switching transistor.

[0010] There is provided in an embodiment of the present disclosure an organic light emitting display panel, comprising a plurality of the pixel circuits provided in the embodiment of the present disclosure arranged in array.

[0011] There is provided in an embodiment of the present disclosure a display apparatus, comprising the organic light emitting display panel provided in the embodiment of the present disclosure.

[0012] In a possible implementation, in the display apparatus provided in the embodiment of the present disclosure, it is further comprised: a test controlling unit connected to a test signal terminal through a test signal line, and a compensation processing unit and a driving unit connected to a data signal terminal through a data line;

wherein the test controlling unit is configured to provide a test signal switching between a displaying period of time and a testing period of time to the test signal terminal;
the compensation processing unit is configured to determine a compensation voltage signal for the respective pixel circuits according to a current signal received from the data signal terminal during the testing period of time and transmit the compensation voltage signal to the driving unit; and
the driving unit is configured to superpose the compensation voltage signal transmitted by the compensation processing unit and a data signal received from a signal source and then transmit the superposed signals to the data signal terminal.

[0013] In a possible implementation, in the display apparatus provided in the embodiment of the present disclosure, the compensation processing unit and the driving unit are integrated on a same chip.

[0014] According to an embodiment, a testing module is added to the pixel circuit. The testing module receives the test signal switching between the displaying period of time and the testing period of time, and is configured to connect the second terminal of the charging module with the control terminal of the driving module during the displaying period of time and connect the second reference signal terminal with the second terminal of the light emitting device, so that the charging module provides the driving voltage signal to the driving module under the control of the scan signal terminal, and the driving module drives the light emitting device to emit light under the control of the driving voltage signal, thereby realizing the function of emitting light normally. This testing module is further configured to connect the second terminal of the light emitting device with the output ermine of the charging module during the testing period of time, so that the charging module outputs the current signal of the light emitting device to the data signal terminal under the control of the scan signal terminal, and then an external compensation processing unit determines the compensation voltage signal for the respective pixel circuits according to the current signal received by the data signal terminal, and the driving unit transmits the compensation voltage signal determined by the compensation processing unit and the data signal received from the signal source to the data signal terminal after superposing them. By providing a compensated driving voltage signal for the driving module through the charging module, an external compensation function is realized, which finally realizes that the current signal for driving the light emitting device in each pixel achieves the uniformity standard, so that display luminance of each pixel is uniform and the quality of the display picture is ensured.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015]

Fig.1 is a schematic diagram of a configuration of a known pixel circuit;
Fig.2 is a schematic diagram of a configuration of a pixel circuit provided in an embodiment of the present disclosure;
Fig.3a is a schematic diagram of an exemplary configuration of a pixel circuit provided in an embodiment of the present disclosure;
Fig.3b is an exemplary operation timing diagram of the configuration of the pixel circuit as shown in Fig.3a provided in an embodiment of the present disclosure;
Fig.4a is a schematic diagram of another exemplary configuration of a pixel circuit provided in an embodiment of the present disclosure;
Fig.4b is an exemplary operation timing diagram of the configuration of the pixel circuit as shown in Fig.4a provided in an embodiment of the present disclosure;
Fig.5 is a schematic diagram of a configuration of a display apparatus provided in an embodiment of the present disclosure.

DETAILED DESCRIPTION

[0016] Specific implementations of a pixel circuit, an organic light emitting display panel and a display apparatus provided in embodiments of the present disclosure will be described in detail by combining with accompanying figures.

[0017] Fig.1 is a schematic diagram of a configuration of a known pixel circuit. As shown in Fig.1, the pixel circuit driving OLED to emit light comprises: a driving transistor M1, a second switching transistor M2, a storage capacitor C and a light emitting device OLED; wherein a gate of the driving transistor M1 is connected to a drain of the

second switching transistor M2 and one terminal of the storage capacitor C respectively, a source thereof is connected to the other terminal of the storage capacitor C and a high voltage signal terminal VDD, and a drain thereof is connected to one terminal of the light emitting device OLED; a gate of the switching transistor M2 is connected to a scan signal terminal Gate, and a drain thereof is connected to a data signal terminal Data; the other terminal of the light I emitting device OLED is connected to a low voltage signal terminal VSS. When the driving transistor M1 drives the light emitting device OLED to emit light, a driving current is controlled by the high voltage signal terminal VDD, the data signal terminal Data and the driving transistor M1 jointly. The driving transistor M1 cannot be made completely consistent in the manufacturing process thereof, and non-uniformity exists in a threshold voltage V_{th} of the driving transistor M1 in the respective pixel circuits due to manufacturing process and device aging and so on, which result in a change occurring in a current flowing through OLED of each pixel point, so that the display luminance is non-uniform, thereby influencing the display effect of the entire image.

[0018] Fig.2 shows a schematic diagram of a configuration of a pixel circuit provided in an embodiment of the present disclosure. As shown in Fig.2, the pixel circuit in the embodiment of the present disclosure comprises: a light emitting device 01, a charging module 02, a driving module 03, and a testing module 04.

[0019] In the pixel circuit as shown in Fig.2, a first terminal of the charging module 02 is connected to the data signal terminal Data, a control terminal thereof is connected to the scan signal terminal Gate, and a second terminal thereof is connected to a first terminal a1 and a third terminal b1 of the testing module 04 respectively.

[0020] A control terminal of the driving module 03 is connected to a fourth terminal b2 of the testing module 04, an input terminal thereof is connected to a first reference signal terminal Ref1, and an output terminal thereof is connected to a first terminal of the light emitting device 01.

[0021] A control terminal of the testing module 04 is connected to a test signal terminal TEST, a second terminal a2 thereof is connected to a second terminal of the light emitting device 01, and a fifth terminal b3 thereof is connected to a second reference signal terminal Ref2; the test signal terminal TEST is used to provide a test signal switching between a displaying period of time and a testing period of time.

[0022] During the displaying period, the testing module 04 is configured to connect the second terminal of the charging module 02 with the control terminal of the driving module 03 and connect the second reference signal terminal Ref2 with the second terminal of the light emitting device 01, so that the charging module 02 provides a driving voltage signal to the driving module 03 under the control of the scan signal terminal Gate, and the driving module 03 drives the light emitting device 01 to emit light under the control of the driving voltage signal.

[0023] During the test period, the testing module 04 is configured to connect the second terminal of the light emitting device 01 with the second terminal of the charging module 02, so that the charging module 02 outputs a current signal of the light emitting device 01 to the data signal terminal Data under the control of the scan signal terminal Gate.

[0024] In the pixel circuit provided in the embodiment of the present disclosure, a testing module 04 is added. The testing module 04 receives the test signal switching between the displaying period of time and the testing period of time, and is configured to connect the second terminal of the charging module 02 with the control terminal of the driving module 03 during the displaying period of time, and connect the second reference signal terminal Ref2 with the second terminal of the light emitting device 01, so that the charging module 02 provides the driving voltage signal to the driving module 03 under the control of the scan signal terminal Gate, and the driving module 03 drives the light emitting device 01 to emit light under the control of the driving voltage signal, thereby realizing the function of emitting light normally. The testing module 04 is further configured to connect the second terminal of the light emitting device 01 with the second terminal of the charging module 02 during the testing period of time, so that the charging module 02 outputs the current signal of the light emitting device 01 to the data signal terminal Data under the control of the scan signal terminal Gate, which provides a flowing path for the current signal of the light emitting device 01 to flow into the data signal terminal Data to complete the testing. Thus, it ensures to finally realize that the current signal for driving the light emitting device in each pixel achieves the uniformity standard, so that the display luminance of each pixel is uniform, thereby ensuring the quality of the display picture.

[0025] As shown in Figs.3a and 4a, the testing module 04 in the pixel circuit provided in the embodiment of the present disclosure can comprise: a first switching transistor T1, and a second switching transistor T2 and a third switching transistor T3 which have the same doping polarity; the first switching transistor T1 has a doping polarity inverse to the second switching transistor T2 and the third switching transistor T3.

[0026] In the embodiment as shown in Figs.3a and 4a, a gate of the first switching transistor T1, a gate of the second switching transistor T2 and a gate of the third switching transistor T3 are connected to the test signal terminal TEST respectively;

a source of the first switching transistor T1 and a source of the third switching transistor T3 are connected to the second terminal of the light emitting device;

a drain of the first switching transistor T1 and a source of the second switching transistor T2 are connected to the second terminal of the charging module 02 respectively;

a drain of the second switching transistor T2 is connected to the control terminal of the driving module 03; and

a drain of the third switching transistor T3 is connected to a second reference signal terminal Vss.

[0027] Specifically, when the testing module 04 is composed by adopting the first switching transistor T1, the second switching transistor T2 and the third switching transistor T3, by combining with the operation timing diagrams as shown in Figs.3b and 4b, where Figs.3b and 4b are specific to scan pixel circuits of one row, it has the following operating principle: during a displaying period of time A, the test signal terminal TEST is inputted a test signal to control the first switching transistor T1 to be in a turn-off state and control the second switching transistor T2 and the third switching transistor T3 to be in a turn-on state, so that the charging module 02 outputs the driving voltage signal to the driving module 03, and the driving module 03 drives the light emitting device 01 to emit light under the control of the driving voltage signal. During a testing period of time B, the test signal terminal TEST is inputted a test signal having a polarity inverse to the test signal inputted during the displaying period of time A to control the first switching transistor T1 to be in the turn-on state and control the second switching transistor T2 and the third switching transistor T3 to be in the turn-off state, so that the current signal of the light-emitting device 01 flows into the second terminal of the charging module 02, and the charging module 02 outputs the current signal of the light emitting device 01 to the data signal terminal Data under the control of the scan signal terminal Gate, that is, current flowing directions in the pixel circuit during the displaying period of time A and the testing period of time B are inverse to each other to provide the flowing path of the current signal in order to complete the testing of the driving current signal and the external compensation, , which finally realizes that the current signal for driving the light emitting device 01 in each pixel achieves the uniformity standard, so that the display luminance of each pixel is uniform, thereby ensuring the quality of the display picture.

[0028] In the pixel circuit provided in the embodiment of the present disclosure, the testing module 04 has to complete different operations during the displaying period of time A and the testing period of time B, and thus it requires that the first switching transistor T1 has a doping type inverse to the second switching transistor T2 and the third switching transistor T3 respectively. Specifically, as shown in Fig.3a, the first switching transistor T1 can be set as an N type transistor, while the second switching transistor T2 and the third switching transistor T3 can be set as P type transistors. In this configuration, as shown in Fig.3b, it requires that the test signal terminal TEST is inputted a low level signal during the displaying period of time A to control the first switching transistor T1 to be in the turn-off state and control the second switching transistor T2 and the third switching transistor T3 to be in the turn-on state, and that the test signal terminal TEST is inputted a high level signal during the testing period of time B to control the first switching transistor T1 to be in the turn-on state and control the second switching transistor T2 and the third switching transistor T3 to be in the turn-off state. Also, as shown in Fig.4a, the first switching transistor T1 is set as the P type transistor, while the second switching transistor T2 and the third switching transistor T3 are set as the N type transistor. In this configuration, as shown in Fig.4b, it requires that the test signal terminal TEST is inputted the high level signal during the displaying period of time A to control the first switching transistor T1 to be in the turn-off state and control the second switching transistor T2 and the third switching transistor T3 to be in the turn-on state, and that the test signal terminal TEST is inputted the low level signal during the testing period of time B to control the first switching transistor T1 to be in the turn-on state and control the second switching transistor T2 and the third switching transistor T3 to be in the turn-off state. In this way, the first switching transistor T1, the second switching transistor T2 and the third switching transistor T3 are turned on at different times under the control of the test signal terminal TEST to complete functions of the testing module 04 during different periods of time.

[0029] As shown in Figs.3a and 4a, in the pixel circuit provided in the embodiment, the charging module 02 can comprise: a fourth switching transistor T4, whose gate is connected to the scan signal terminal Gate, source is connected to the data signal terminal Data, and drain is connected to the first terminal a1 and the third terminal b1 of the testing module 04.

[0030] Specifically, the fourth switching transistor T4 can be the P type transistor as shown in Fig.3a. Also, the fourth switching transistor T4 can be the N type transistor as shown in Fig.4a, to which no limitation is made herein.

[0031] When the fourth switching transistor T4 is manufactured by adopting the P type transistor, as shown in Fig.3b, during the displaying period of time A, the scan signal terminal Gate is inputted the low level signal to control the fourth switching transistor T4 to be in the turn-on state, and the turned-on fourth switching transistor T4 outputs the driving voltage signal of the data signal terminal Data to the control terminal of the driving module 03 through the testing module 04, so that the driving module 03 drives the light emitting device 01 to emit light under the control of the driving voltage signal, thereby realizing the function of emitting light normally; during the testing period of time B, the scan signal terminal Gate is still inputted the low level signal to control the fourth switching transistor T4 to be in the turn-on state, and the turned on fourth switching transistor T4 outputs the current signal of the light emitting device 01 outputted by the testing module 04 to the data signal terminal Data, which provides the flowing path for the current signal of the light emitting device 01 to flow into the data signal terminal Data to complete the testing.

[0032] When the fourth switching transistor T4 is man-

ufactured by adopting the N type transistor, as shown in Fig.4b, during the displaying period of time A and the testing period of time B, the scan signal terminal Gate is inputted the high level signal to control the fourth switching transistor T4 to be in the turn-on state, and the function completed by the turned on fourth switching transistor T4 during the displaying period of time A and the testing period of time B is the same as that completed by the fourth switching transistor T4 when it is manufactured by adopting the P type transistor. The repeated description is not given herein.

[0033] As shown in Figs.3a and 4a, in the pixel circuit provided in the embodiment of the present disclosure, the driving module 03 can comprise: a storage capacitor C1 and a fifth switching transistor T5; a source of the fifth switching transistor T5 is connected to the first reference signal terminal Ref1, a gate thereof is connected to the fourth terminal b2 of the testing module 04, and a drain thereof is connected to the first terminal of the light emitting device 01; when the fifth switching transistor T5 is the P type transistor, the storage capacitor C1 is connected in parallel between the source and the gate of the fifth switching transistor T5; when the fifth switching transistor T5 is the N type transistor, the storage capacitor C1 is connected in parallel between the drain and the gate of the fifth switching transistor T5. Specifically, during the displaying period of time A, the fifth switching transistor T5 drives the light emitting device 01 to emit light under the control of the driving voltage signal; during the testing period of time B, since the storage capacitor C1 is discharged to provide the driving voltage signal to the fifth switching transistor T5, the fifth switching transistor T5 is still in the turn-on state and drives the light emitting device 01 to emit light continuously.

[0034] It should be noted that the switching transistors described in the embodiment of the present disclosure can be thin film transistors (TFT) or can be metal oxide semiconductors (MOS), to which no limitation is made herein. In the specific implementation, sources and drains of these transistors can be exchanged with each other, and no specific distinction is made between these sources and drains.

[0035] It should be noted that the pixel circuit provided in the embodiment of the present disclosure can realize the function of external compensation, or can be applicable to a pixel circuit having the function of internal compensation, so that compensation for the threshold voltage of the driving transistor is realized. Its implementation and operating principle are similar to the above pixel circuit provided in the embodiments of the present disclosure, and thus the repeated description is not given herein.

[0036] Based on the same disclosed concept, there is provided in an embodiment of the present disclosure an organic light emitting display panel, comprising a plurality of pixel circuits provided in the embodiment of the present disclosure arranged in array. Since the organic light emitting display panel has a principle for solving the problem similar to the pixel circuit, the implementation of the organic light emitting display panel can refer to the implementation of the pixel circuit. Thus, the repeated description is not further given herein.

[0037] Based on the same disclosed concept, there is provided in an embodiment of the present disclosure a display apparatus, comprising the organic light emitting display panel provided in the embodiment of the present disclosure. The display apparatus can be any product or components having the displaying function, such as a mobile phone, a tablet computer, a TV set, a display device, a notebook computer, a digital photo frame, and a navigator and so on. Since the display apparatus has a principle for solving the problem similar to the organic light emitting display panel, the implementation of the display apparatus can refer to the implementation of the organic light emitting display panel. Thus, the repeated description is not further given herein.

[0038] Fig.5 shows a schematic diagram of a configuration of the display apparatus provided in the embodiment of the present disclosure. As shown in Fig.5, in the specific implementation, besides comprising the organic light emitting display panel provided in the embodiment of the present disclosure, the display apparatus provided in the embodiment of the present disclosure can further comprise:

a test controlling unit 05 connected to the test signal terminal TEST through the test signal line, and a compensation processing unit 06 and a driving unit 07 connected to the data signal terminal Data through the data line;

wherein the test controlling unit 05 is configured to provide a test signal switching between the displaying period of time and the testing period of time to the test signal terminal TEST;

the compensation processing unit 06 is configured to determine a compensation voltage signal for the respective pixel circuits according to the current signal received by the data signal terminal Data during the testing period of time and transmit the compensation voltage signal to the driving unit 07; and

the driving unit 07 is configured to superpose the compensation voltage signal transmitted by the compensation processing unit 06 and the data signal received from the signal source and then transmit the superposed signals to the data signal terminal Data.

[0039] Specifically, in the display apparatus provided in the embodiment of the present disclosure, during the displaying period of time, the charging module 02 in the pixel circuit provides the driving voltage signal to the driving module 03 through the testing module 04 to control the driving module 03 to drive the light emitting device 01 to emit light, thereby realizing the function of emitting light normally; during the testing period of time, the current signal outputted by the second terminal of the light emitting device 01 flows through the testing module 04

to reach the second terminal of the charging module 02, and the charging module 02 outputs the current signal to the data signal terminal Data under the control of the scan signal terminal Gate, so that the compensation processing unit 06 determines the compensation voltage signal for the respective pixel circuits according to the current signal received from the data signal terminal Data, and the driving unit 07 superpose the compensation voltage signal determined by the compensation processing unit 06 and the data signal received from the signal source and then transmit them to the data signal terminal Data, thereby realizing the function of compensating.

[0040] For example, in the display apparatus provided in the embodiment of the present disclosure, during the testing period of time, the compensation processing unit 06, is used, by combining with the gating effect of the scan signal terminal Gate, to determine a corresponding compensation voltage signal according to the current signal received by the data signal terminal Data of each pixel unit, and for the pixel unit whose compensation voltage signal is determined, external compensation is realized through the driving unit 07, and then the current of each pixel unit is tested again until the current of all the pixel units reaches the uniformity standard. At this time, a compensation parameter is written into the driving unit 07, for example, the pixel units in the N-th column and the N-th row need a compensation voltage signal of -0.1V, then in the subsequent pixel driving process, the driving voltage signal of the pixel unit is maintained a reduction of 0.1V. In this way, the driving current of the respective pixel units reaching the uniformity standard is finally realized, and the uniformity of the display luminance of pixels is ensured, so that the quality of the display picture is ensured.

[0041] In the specific implementation, in the display apparatus provided in the embodiment of the present disclosure, the compensation processing unit 06 and the driving unit 07 can be integrated on a same chip. Specifically, in the design of a product, the test controlling unit 05, the compensation processing unit 06 and the driving unit 07 can also be integrated on the same chip. Such a design is advantageous for realizing a simultaneous control of all the pixels by using the smallest occupation space, to avoid that an aperture ratio of the product is affected, the arrangement space is saved, and the production cost is reduced.

[0042] There are provided in the embodiments of the present disclosure a pixel circuit, an organic light emitting display panel and a display apparatus. A testing module is added to the pixel circuit. The testing module receives the test signal switching between the displaying period of time and the testing period of time, and is configured to connect the second terminal of the charging module with the control terminal of the driving module during the displaying period of time, and connect the second reference signal terminal with the second terminal of the light emitting device, so that the charging module provides the driving voltage signal to the driving module under the control of the scan signal terminal, and the driving module drives the light emitting device to emit light under the control of the driving voltage signal, thereby realizing the function of emitting light normally. The testing module is further configured to connect the second terminal of the light emitting device with the second terminal of the charging module during the testing period of time, so that the charging module outputs the current signal of the light emitting device to the data signal terminal under the control of the scan signal terminal, and then the external compensation processing unit determines the compensation voltage signal for the respective pixel circuits according to the current signal received by the data signal terminal, and the driving unit superpose the compensation voltage signal determined by the compensation processing unit and the data signal received from the signal source and then transmit the superposed signals to the data signal terminal. By providing a compensated driving voltage signal for the driving module through the charging module, the external compensation function is realized, and the current signal for driving the light emitting device in each pixel achieving the uniformity standard is finally realized, so that display luminance of each pixel is uniform, thereby ensuring the quality of the display picture.

[0043] The present application claims the priority of a Chinese patent application No. 201410419203.4 filed on August 22, 2014.

Claims

1. A pixel circuit, comprising:

a light emitting device (01) having a first terminal and a second terminal;
a charging module (02) having a first terminal, a second terminal and a control terminal;
a driving module (03) having an input terminal, an output terminal and a control terminal;
a testing module (04) having a first terminal (a1), a second terminal (a2), a third terminal (b1), a fourth terminal (b2), a fifth terminal (b3) and a control terminal;
the first terminal of the charging module (02) is connected to a data signal (Data), the control terminal of the charging module (02) is connected to a scan signal (Gate), and the second terminal of the charging module (02) is connected to the first terminal (a1) and the third terminal (b1) of the testing module (04) respectively;
the control terminal of the driving module (03) is connected to a fourth terminal (b2) of the testing module (04), the input terminal of the driving module (03) is connected to a first reference signal (Ref1), and the output terminal of the driving module (03) is connected to the first terminal of the light emitting device (01); and

the control terminal of the testing module (04) is connected to a test signal (Test), the second terminal (a2) of the testing module (04) is connected to the second terminal of the light emitting device (01), and the fifth terminal (b3) of the testing module (04) is connected to a second reference signal (Ref2),
wherein the testing signal (TEST) is configured to provide switching between a displaying period of time and a testing period of time,
characterized in that:

the testing module (04) is configured, during the displaying period of time, to connect the second terminal of the charging module (02) with the control terminal of the driving module (03), and to connect the second reference signal (Ref2) with the second terminal of the light emitting device (01), so that the charging module (02) provides a driving voltage signal to the driving module (03) under the control of the scan signal (Gate), and the driving module (03) drives the light emitting device (01) to emit light under the control of the driving voltage signal,
and the testing module (04) is configured to, during the testing period of time, connect the second terminal of the light emitting device (01) with the second terminal of the charging module (02), so that the charging module (02) outputs a current signal of the light emitting device (01) to the first terminal of the charging module (02) under the control of the scan signal (Gate).

2. The pixel circuit according to claim 1, wherein the testing module (04) comprises: a first switching transistor (T1), and a second switching transistor (T2) and a third switching transistor (T3) which have a same doping polarity; and the first switching transistor (T1) has a doping polarity inverse to the second switching transistor (T2) and the third switching (T3) transistor respectively; wherein a gate of the first switching transistor (T1), a gate of the second switching transistor (T2) and a gate of the third switching transistor (T3) are connected to the test signal (TEST) respectively;

a source of the first switching transistor (T1) and a source of the third switching transistor (T3) are connected to the second terminal of the light emitting device (01) respectively;
a drain of the first switching transistor (T1) and a source of the second switching transistor (T2) are connected to the second terminal of the charging module (T4); a drain of the second switching transistor (T2) is connected to the control terminal of the driving module (03); and

a drain of the third switching transistor (T3) is connected to the second reference signal (Ref2).

3. The pixel circuit according to claim 2, wherein the first switching transistor (T1) is an N type transistor, while the second switching transistor (T2) and the third switching transistor (T3) are P type transistors; or
the first switching transistor (T1) is the P type transistor, while the second switching transistor (T2) and the third switching transistor (T3) are N type transistors.

4. The pixel circuit according to any one of claims 1 to 3, wherein the charging module (02) comprises: a fourth switching transistor (T4);
wherein a gate of the fourth switching transistor (T4) is connected to the scan signal (Gate), a source of the fourth switching transistor (T4) is connected to the data signal (Data), and a drain of the fourth switching transistor (T4) is connected to the first terminal (a1) and the third terminal (b1) of the testing module (04).

5. The pixel circuit according to any one of claims 1 to 3, wherein the driving module (03) comprises: a storage capacitor (C) and a fifth switching transistor (T5);

a source of the fifth switching transistor (T5) is connected to the first reference signal (Ref1), a gate of the fifth switching transistor (T5) is connected to the fourth terminal (b2) of the testing module (04), and a drain of the fifth switching transistor (T5) is connected to the first terminal of the light emitting device (01); when the fifth switching transistor (T5) is a P type transistor, the storage capacitor (C) is connected in parallel between the source and the gate of the fifth switching transistor (T5); and
when the fifth switching transistor (T5) is an N type transistor, the storage capacitor (C) is connected in parallel between the drain and the gate of the fifth switching transistor (T5).

6. An organic light emitting display panel, comprising a plurality of the pixel circuits according to any one of claims 1 to 5 arranged in array.

7. A display apparatus, comprising the organic light emitting display panel according to claim 6.

8. The display apparatus according to claim 7, further comprising: a test controlling unit (05) connected to a test signal terminal through a test signal line, and a compensation processing unit (06) and a driving unit (07) connected to a data signal terminal through a data line;

wherein the test controlling unit (05) is configured to provide a test signal switching between a displaying period of time and a testing period of time to the test signal terminal;
the compensation processing unit (06) is configured to determine a compensation voltage signal for the respective pixel circuits according to a current signal received from the data signal terminal during the testing period of time and transmit the compensation voltage signal to the driving unit; and
the driving unit (07) is configured to superpose the compensation voltage signal transmitted by the compensation processing unit and a data signal received from a signal source and then transmit the superposed signals to the data signal terminal.

9. The display apparatus according to claim 8, wherein the compensation processing unit (06) and the driving unit (07) are integrated on a same chip.

Patentansprüche

1. Pixelschaltung, umfassend:

eine lichtemittierende Vorrichtung (01), aufweisend einen ersten Anschluss und einen zweiten Anschluss;
ein Lademodul (02), aufweisend einen ersten Anschluss, einen zweiten Anschluss und einen Steuerungsanschluss;
ein Treibermodul (03), aufweisend einen Eingangsanschluss, einen Ausgangsanschluss und einen Steuerungsanschluss;
ein Testmodul (04), aufweisend einen ersten Anschluss (a1), einen zweiten Anschluss (a2), einen dritten Anschluss (b1), einen vierten Anschluss (b2), einen fünften Anschluss (b3) und einen Steuerungsanschluss;
wobei der erste Anschluss des Lademoduls (02) an ein Datensignal (Data) angeschlossen ist, der Steuerungsanschluss des Lademoduls (02) an ein Abtastsignal (Gate) angeschlossen ist und der zweite Anschluss des Lademoduls (02) jeweils an den ersten Anschluss (a1) und den dritten Anschluss (b1) des Testmoduls (04) angeschlossen ist;
wobei der Steuerungsanschluss des Treibermoduls (03) an einen vierten Anschluss (b2) des Testmoduls (04) angeschlossen ist, der Eingangsanschluss des Treibermoduls (03) an ein erstes Referenzsignal (Ref1) angeschlossen ist, und der Ausgangsanschluss des Treibermoduls (03) an den ersten Anschluss der lichtemittierenden Vorrichtung (01) angeschlossen ist; und
wobei der Steuerungsanschluss des Testmoduls (04) an ein Testsignal (Test) angeschlossen ist, der zweite Anschluss (a2) des Testmoduls (04) an den zweiten Anschluss der lichtemittierenden Vorrichtung (01) angeschlossen ist und der fünfte Anschluss (b3) des Testmoduls (04) an ein zweites Referenzsignal (Ref2) angeschlossen ist,
wobei das Testsignal (Test) konfiguriert ist, um Umschaltung zwischen einer Anzeigezeitperiode und einer Testzeitperiode bereitzustellen,
dadurch gekennzeichnet, dass:

das Testmodul (04) konfiguriert ist, während der Anzeigezeitperiode den zweiten Anschluss des Lademoduls (02) mit dem Steuerungsanschluss des Treibermoduls (03) zu verbinden, und das zweite Referenzsignal (Ref2) mit dem zweiten Anschluss der lichtemittierenden Vorrichtung (01) zu verbinden, so dass das Lademodul (02) ein Treiberspannungssignal an das Treibermodul (03) bereitstellt unter der Steuerung des Abtastsignals (Gate), und das Treibermodul (03) die lichtemittierende Vorrichtung (01) ansteuert, um Licht zu emittieren unter der Steuerung des Treiberspannungssignals, und
das Testmodul (04) konfiguriert ist, während der Testzeitperiode den zweiten Anschluss der lichtemittierenden Vorrichtung (01) mit dem zweiten Anschluss des Lademoduls (02) zu verbinden, so dass das Lademodul (02) ein Stromsignal der lichtemittierenden Vorrichtung (01) an den ersten Anschluss des Lademoduls (02) unter der Steuerung des Abtastsignals (Gate) ausgibt.

2. Pixelschaltung gemäß Anspruch 1, wobei das Testmodul (04) umfasst:

einen ersten Schalttransistor (T1), und einen zweiten Schalttransistor (T2) und einen dritten Schalttransistor (T3), die eine gleiche Dotierungspolarität aufweisen; wobei der erste Schalttransistor (T1) eine jeweils zu dem zweiten Schalttransistor (T2) und dem dritten Schalttransistor (T3) inverse Dotierungspolarität aufweist;
wobei ein Gate des ersten Schalttransistors (T1), ein Gate des zweiten Schalttransistors (T2) und ein Gate des dritten Schalttransistors (T3) jeweils an das Testsignal (Test) angeschlossen sind;
wobei eine Source des ersten Schalttransistors (T1) und eine Source des dritten Schalttransistors (T3) jeweils an den zweiten Anschluss der

lichtemittierenden Vorrichtung (01) angeschlossen sind;
wobei ein Drain des ersten Schalttransistors (T1) und eine Source des zweiten Schalttransistors (T2) an den zweiten Anschluss des Lademoduls (T4) angeschlossen sind;
wobei ein Drain des zweiten Schalttransistors (T2) an den Steuerungsanschluss des Treibermoduls (03) angeschlossen ist; und
wobei ein Drain des dritten Schalttransistors (T3) an das zweite Referenzsignal (Ref2) angeschlossen ist.

3. Pixelschaltung gemäß Anspruch 2, wobei der erste Schalttransistor (T1) ein N-Typ-Transistor ist, während der zweite Schalttransistor (T2) und der dritte Schalttransistor (T3) P-Typ-Transistoren sind; oder wobei der erste Schalttransistor (T1) der P-Typ-Transistor ist, während der zweite Schalttransistor (T2) und der dritte Schalttransistor (T3) N-Typ-Transistoren sind.

4. Pixelschaltung gemäß einem der Ansprüche 1 bis 3, wobei das Lademodul (02) umfasst: einen vierten Schalttransistor (T4);
wobei ein Gate des vierten Schalttransistors (T4) an das Scan-Signal (Gate) angeschlossen ist, eine Source des vierten Schalttransistors (T4) an das Datensignal (Data) angeschlossen ist, und ein Drain des vierten Schalttransistors (T4) an den ersten Anschluss (a1) und den dritten Anschluss (b1) des Testmoduls (04) angeschlossen ist.

5. Pixelschaltung gemäß einem der Ansprüche 1 bis 3, wobei das Treibermodul (03) umfasst: einen Speicherkondensator (C) und einen fünften Schalttransistor (T5);

wobei eine Source des fünften Schalttransistors (T5) an das erste Referenzsignal (Ref1) angeschlossen ist, ein Gate des fünften Schalttransistors (T5) an den vierten Anschluss (b2) des Testmoduls (04) angeschlossen ist, und ein Drain des fünften Schalttransistors (T5) an den ersten Anschluss der lichtemittierenden Vorrichtung (01) angeschlossen ist;
wobei, wenn der fünfte Schalttransistor (T5) ein P-Typ-Transistor ist, der Speicherkondensator (C) parallel zwischen die Source und das Gate des fünften Schalttransistors (T5) geschaltet ist; und
wobei, wenn der fünfte Schalttransistor (T5) ein N-Typ-Transistor ist, der Speicherkondensator (C) parallel zwischen den Drain und das Gate des fünften Schalttransistors (T5) geschaltet ist.

6. Organische lichtemittierende Anzeigetafel, umfassend eine Mehrzahl der Pixelschaltungen gemäß einem der Ansprüche 1 bis 5, als Array angeordnet.

7. Anzeigevorrichtung, umfassend die organische lichtemittierende Anzeigetafel gemäß Anspruch 6.

8. Anzeigevorrichtung gemäß Anspruch 7, außerdem umfassend: eine Teststeuerungseinheit (05) angeschlossen an einen Testsignalanschluss durch eine Testsignalleitung, und eine Kompensationsverarbeitungseinheit (06) und eine Treibereinheit (07), angeschlossen an einen Datensignalanschluss durch eine Datenleitung;

wobei die Teststeuerungseinheit (05) konfiguriert ist, ein Testsignal bereitzustellen, das zwischen einer Anzeigezeitperiode und einer Testzeitperiode zu dem Testsignalanschluss schaltet;
wobei die Kompensationsverarbeitungseinheit (06) konfiguriert ist, ein Kompensationsspannungssignal zu bestimmen für die jeweiligen Pixelschaltungen gemäß einem Stromsignal, empfangen von dem Datensignalanschluss während der Testzeitperiode, und das Kompensationsspannungssignal an die Treibereinheit zu übertragen; und wobei die Treibereinheit (07) konfiguriert ist, das Kompensationsspannungssignal, das mittels der Kompensationsverarbeitungseinheit übertragen ist, und ein Datensignal, das von einer Signalquelle empfangen ist, zu überlagern, und dann die überlagerten Signale an den Datensignalanschluss zu übertragen.

9. Anzeigevorrichtung gemäß Anspruch 8, wobei die Kompensationsverarbeitungseinheit (06) und die Treibereinheit (07) auf einem gleichen Chip integriert sind.

Revendications

1. Circuit de pixel, comprenant :

un dispositif émetteur de lumière (01) ayant une première borne et une deuxième borne ;
un module de charge (02) ayant une première borne, une deuxième borne et une borne de commande ;
un module d'entraînement (03) ayant une borne d'entrée, une borne de sortie et une borne de commande ;
un module de test (04) ayant une première borne (a1), une deuxième borne (a2), une troisième borne (b1), une quatrième borne (b2), une cinquième borne (b3) et une borne de commande ;
la première borne du module de charge (02) est connectée à un signal de données (Data), la bor-

ne de commande du module de charge (02) est connectée à un signal de balayage (Gate) et la deuxième borne du module de charge (02) est connectée à la première borne (a1) et à la troisième borne (b1) du module de test (04) respectivement ;
la borne de commande du module d'entraînement (03) est connectée à une quatrième borne (b2) du module de test (04), la borne d'entrée du module d'entraînement (03) est connectée à un premier signal de référence (Ref1), et la borne de sortie du module d'entraînement (03) est connectée à la première borne du dispositif d'émission de lumière (01) ; et
la borne de commande du module de test (04) est connectée à un signal de test (Test), la deuxième borne (a2) du module de test (04) est connectée à la deuxième borne du dispositif émetteur de lumière (01), et la cinquième borne (b3) du module de test (04) est connectée à un second signal de référence (Ref2),
dans lequel le signal de test (Test) est configuré pour fournir une commutation entre une période d'affichage et une période de test,
caractérisé en ce que :

le module de test (04) est configuré, pendant la période d'affichage, pour connecter la deuxième borne du module de charge (02) à la deuxième borne du module d'entraînement (03), et pour connecter le second signal de référence (Ref2) à la deuxième borne du dispositif émetteur de lumière (01) de façon à ce que le module de charge (02) fournisse un signal de tension d'entraînement vers le module d'entraînement (03) sous la commande du signal de balayage (Gate), et le module d'entraînement (03) entraîne le dispositif émetteur de lumière (01) à émettre de la lumière sous la commande du signal de tension d'entraînement, et
le module de test (04) est configuré pour, pendant la période de test, connecter la deuxième borne du dispositif émetteur de lumière (01) à la deuxième borne du module de charge (02) de façon à ce que le module de charge (02) émette un signal de courant du dispositif émetteur de lumière (01) vers la première borne du module de charge (02) sous la commande du signal de balayage (Gate).

2. Circuit de pixel selon la revendication 1, dans lequel le module de test (04) comprend : un premier transistor de branchement (T1), et un deuxième transistor de branchement (T2) et un troisième transistor de branchement (T3) qui ont une même polarité de dopage ; et le premier transistor de branchement (T1) a une polarité de dopage inverse au deuxième transistor de branchement (T2) et au troisième transistor de branchement (T3) respectivement ;

dans lequel une grille du premier transistor de branchement (T1), une grille du deuxième transistor de branchement (T2) et une grille du troisième transistor de branchement (T3) sont connectées au signal de test (Test) respectivement ;
une source du premier transistor de branchement (T1) et une source du troisième transistor de branchement (T3) sont connectées à la deuxième borne du dispositif émetteur de lumière (01) respectivement ;
un drain du premier transistor de branchement (T1) et une source du deuxième transistor de branchement (T2) sont connectés à la deuxième borne du module de charge (T4) ;
un drain du deuxième transistor de branchement (T2) est connecté à la borne de commande du module d'entraînement (03) ; et
un drain du troisième transistor de branchement (T3) est connecté au second signal de référence (Ref2).

3. Circuit de pixel selon la revendication 2, dans lequel le premier transistor de branchement (T1) est un transistor de type N, tandis que le deuxième transistor de branchement (T2) et le troisième transistor de branchement (T3) sont des transistors de type P ; ou le premier transistor de branchement (T1) est le transistor de type P, tandis que le deuxième transistor de branchement (T2) et le troisième transistor de branchement (T3) sont des transistors de type N.

4. Circuit de pixel selon l'une quelconque des revendications 1 à 3, dans lequel le module de charge (02) comprend : un quatrième transistor de branchement (T4) ;
dans lequel une grille du quatrième transistor de branchement (T4) est connectée au signal de balayage (Gate), une source du quatrième transistor de branchement (T4) est connectée au signal de données (Data), et un drain du quatrième transistor de branchement (T4) est connecté à la première borne (a1) et à la troisième borne (b1) du module de test (04).

5. Circuit de pixel selon l'une quelconque des revendications 1 à 3, dans lequel le module d'entraînement (03) comprend : un condensateur de stockage (C) et un cinquième transistor de branchement (T5) ;

une source du cinquième transistor de branchement (T5) est connectée au premier signal de référence (Ref1), une grille du cinquième transistor de branchement (T5) est connectée à la

quatrième borne (b2) du module de test (04), et un drain du cinquième transistor de branchement (T5) est connecté à la première borne du dispositif émetteur de lumière (01) ;
lorsque le cinquième transistor de branchement (T5) est un transistor de type P, le condensateur de stockage (C) est connecté en parallèle entre la source et la grille du cinquième transistor de branchement (T5) ; et
lorsque le cinquième transistor de branchement (T5) est un transistor de type N, le condensateur de stockage (C) est connecté en parallèle entre le drain et la grille du cinquième transistor de branchement (T5) .

6. Panneau d'affichage électro-luminescent organique comprenant une pluralité de circuits de pixel selon l'une quelconque des revendications 1 à 5 agencés en réseau.

7. Appareil d'affichage, comprenant le panneau d'affichage électro-luminescent organique selon la revendication 6.

8. Appareil d'affichage selon la revendication 7, comprenant en outre : une unité de commande de test (05) connectée à une borne de signal de test par une ligne de signal de test, et une unité de traitement de compensation (06) et une unité d'entraînement (07) connectées à une borne de signal de données par le biais d'une ligne de données ;

dans lequel l'unité de commande de test (05) est configurée pour fournir une commutation de signal de test entre une période d'affichage et une période de test vers la borne de signal de test ;
l'unité de traitement de compensation (06) est configurée pour déterminer un signal de tension de compensation pour les circuits de pixels respectifs selon un signal de courant reçu de la borne de signal de données pendant la période de test et transmettre le signal de tension de compensation vers l'unité d'entraînement ; et l'unité d'entraînement (07) est configurée pour superposer le signal de tension de compensation transmis par l'unité de traitement de compensation et un signal de données reçu d'une source de signal puis transmettre les signaux superposés à la borne de signal de données.

9. Appareil d'affichage selon la revendication 8, dans lequel l'unité de traitement de compensation (06) et l'unité d'entraînement (07) sont intégrées sur une même puce.

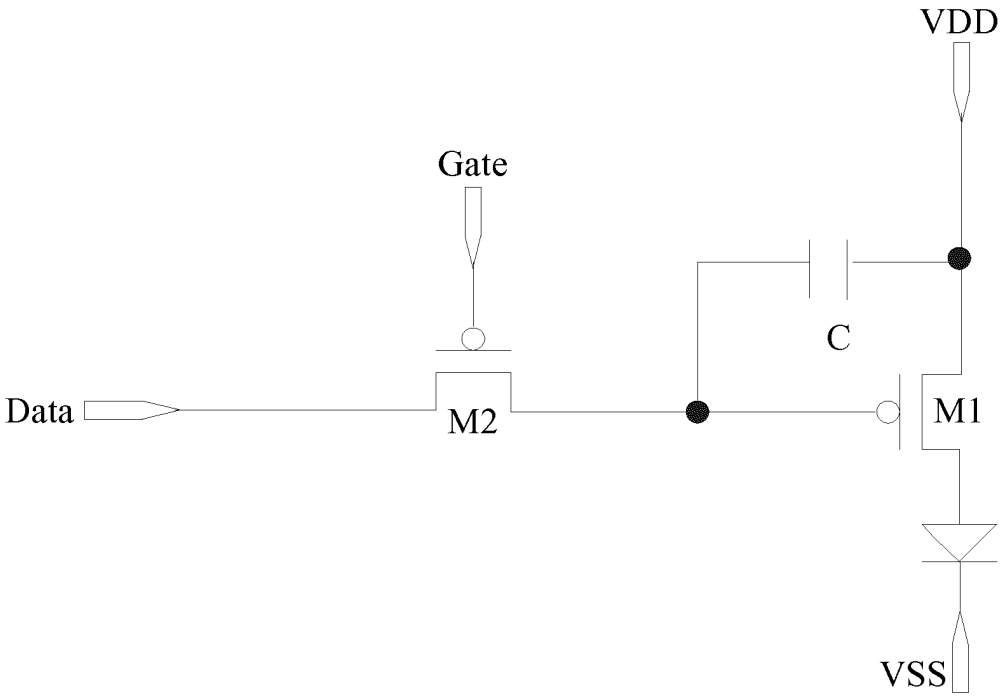
VDD
Gate
C
Data
M2
M1
VSS

Fig.1

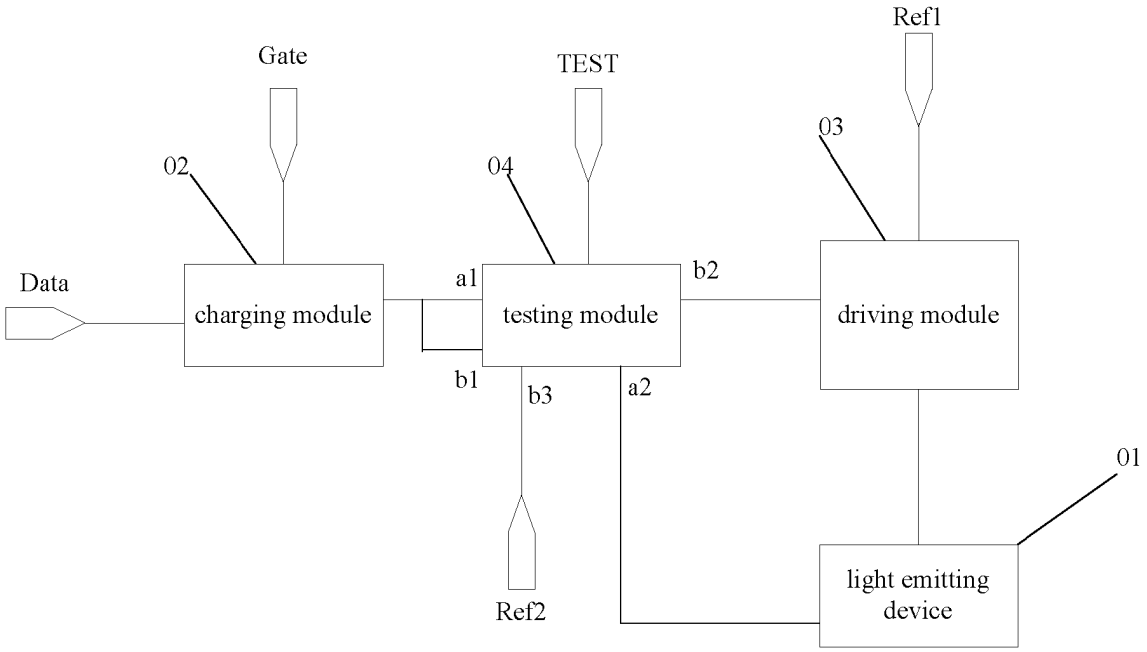
Ref1
Gate
TEST
03
02
04
Data
charging module
a1
testing module
b2
driving module
b1
b3
a2
01
Ref2
light emitting device

Fig.2

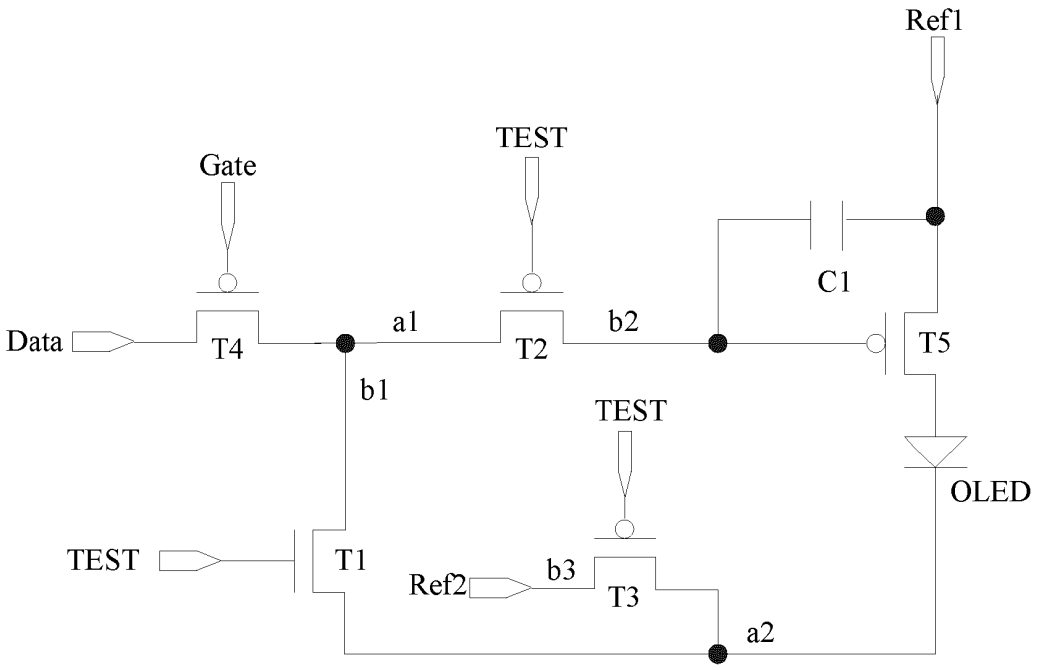
Ref1
TEST
Gate
C1
Data
T4
a1
T2
b2
T5
b1
TEST
OLED
TEST
T1
Ref2
b3
T3
a2

Fig.3a

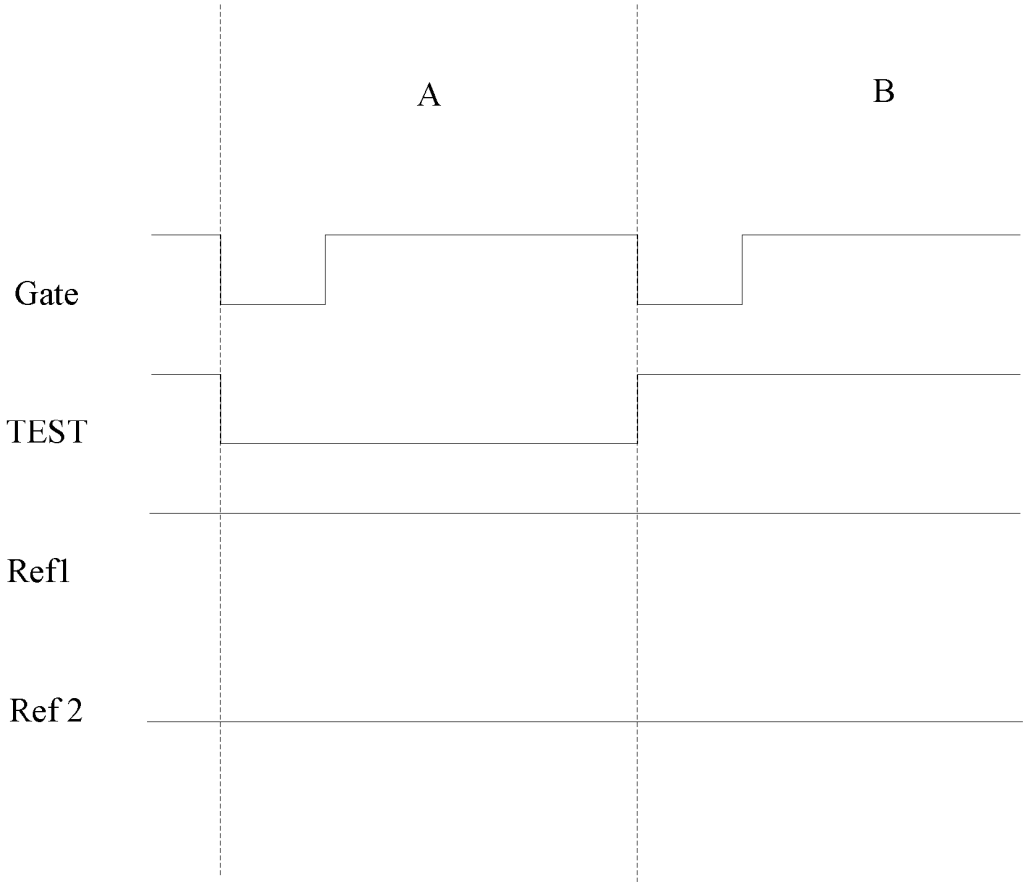
A
B
Gate
TEST
Ref1
Ref 2

Fig.3b

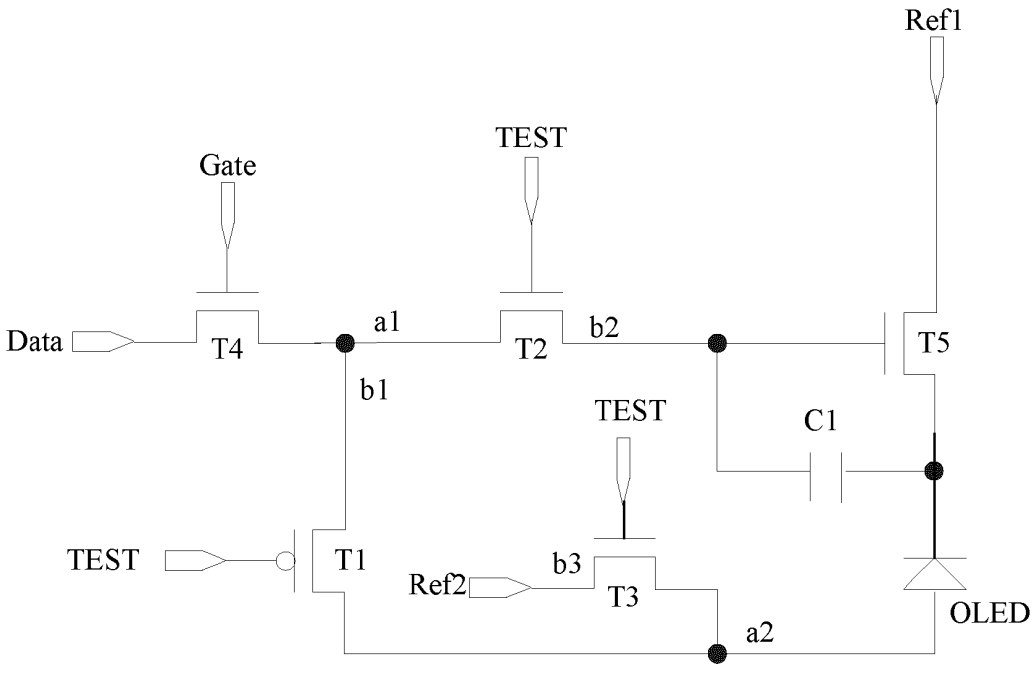
Ref1
TEST
Gate
Data
T4
a1
T2
b2
T5
b1
TEST
C1
TEST
T1
Ref2
b3
T3
OLED
a2

Fig.4a

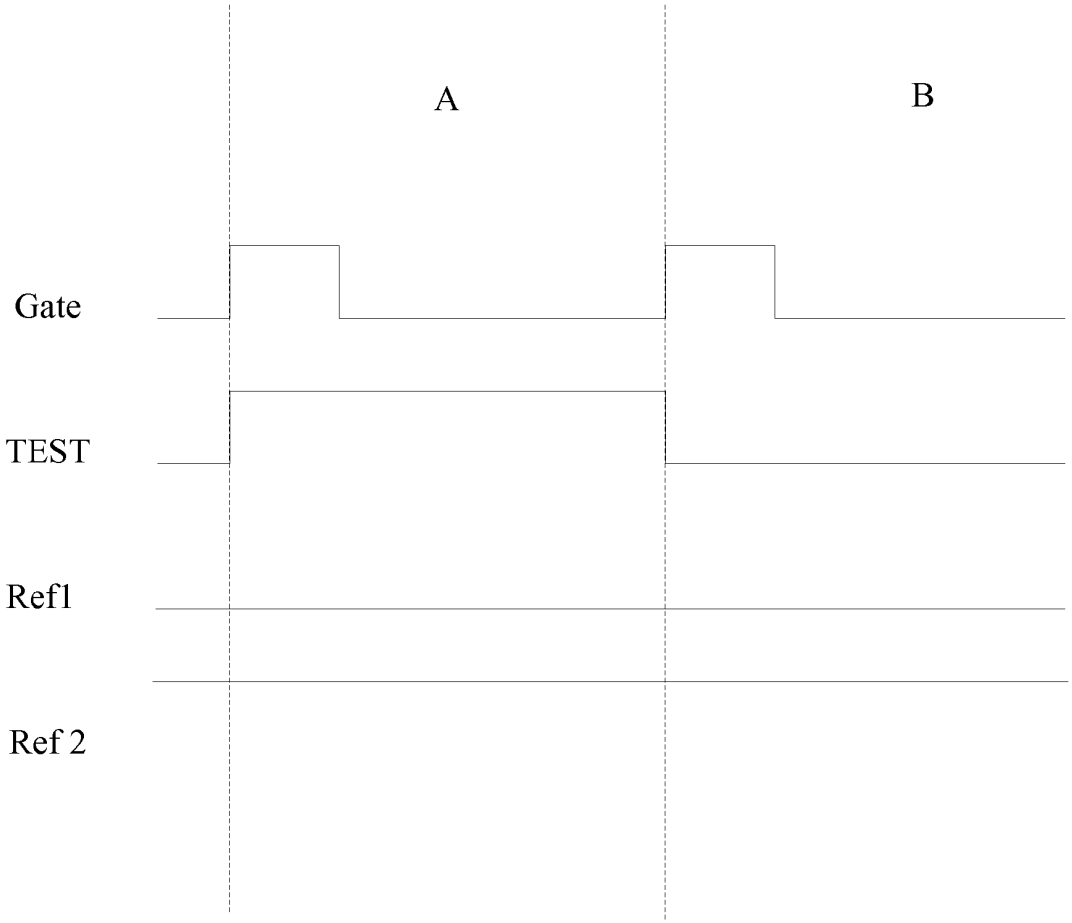
A
B
Gate
TEST
Ref1
Ref 2

Fig.4b

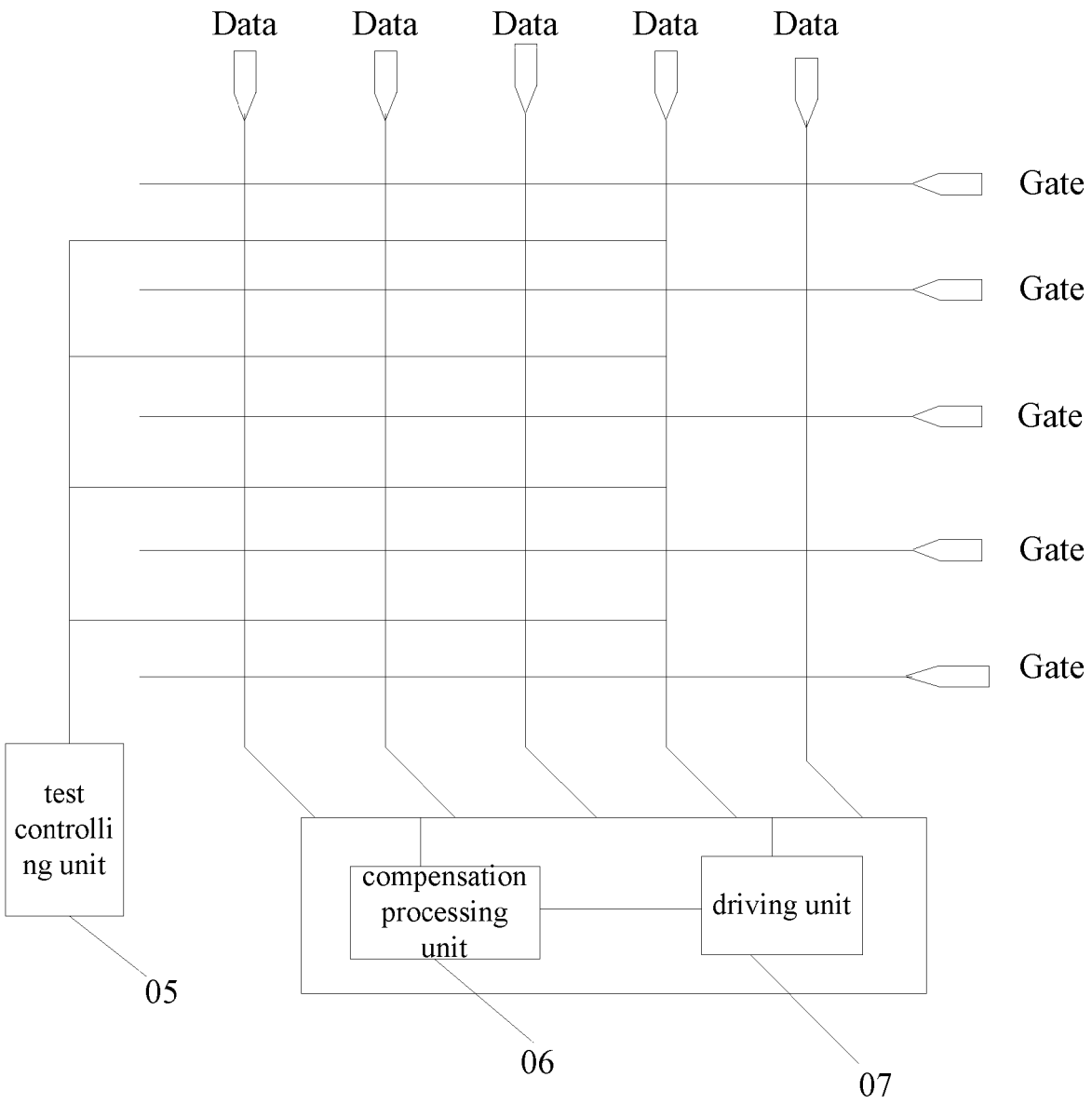
Data
Data
Data
Data
Data
Gate
Gate
Gate
Gate
Gate
test controlling unit
compensation processing unit
driving unit
05
06
07

Fig.5

REFERENCES CITED IN THE DESCRIPTION

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- CN 201410419203 **[0043]**