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(54) **ORGANIC LIGHT-EMITTING DISPLAY PANEL, ORGANIC LIGHT-EMITTING DISPLAY APPARATUS, AND VOLTAGE DROP COMPENSATING METHOD**

ORGANISCHE LICHTEMITTIERENDE ANZEIGETAFEL, ORGANISCHE LICHTEMITTIERENDE ANZEIGEVORRICHTUNG UND VERFAHREN ZUR KOMPENSATION VON SPANNUNGSABFÄLLEN

PANNEAU D'AFFICHAGE ÉLECTROLUMINESCENT ORGANIQUE, DISPOSITIF D'AFFICHAGE ÉLECTROLUMINESCENT ORGANIQUE ET PROCÉDÉ DE COMPENSATION DE CHUTE DE TENSION

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Description

BACKGROUND

1. Field

[0001] The invention relates to an organic light-emitting display panel, an organic light-emitting display apparatus, and a voltage drop compensating method.

2. Description of the Related Art

[0002] An organic light-emitting display apparatus generates images using a plurality of pixels. Each pixel includes an organic light-emitting diode that emits light based on a recombination of electrons and holes in an emitting layer. This type of apparatus has fast response times and low consumption power.

[0003] In terms of structure, the organic light-emitting display apparatus may include a plurality of gate lines, a plurality of source lines, and a plurality of power lines connected to the pixels arranged in a matrix form. The pixels may be driven by an analog driving scheme. In this case, the pixels emit light of various grayscale values by adjusting brightness according to levels of voltage or current data. Alternatively, the pixels may be driven by a digital driving scheme. In this case, the pixels emit light of different grayscale values based on different emission times.

[0004] In operation, a voltage drop (or IR drop) may occur in the power lines. The voltage drop may be caused by relatively higher-level current flowing in each of the power lines and resistance components of the power lines. Due to the voltage drop, source voltages having different voltage levels may be respectively applied to pixels depending on locations of the pixels, and due to the different voltage levels being applied, the pixels may not emit light at the desired brightness.

[0005] US 2014/368416A1 discloses an OLED display device including multiple pixel units arranged in a matrix and a power supply driver chip located at one side of the multiple pixel units. The power supply driver chip provides the input voltages to the multiple pixels units through a plurality of input paths.

SUMMARY

[0006] In accordance with a first aspect of the invention, an organic light-emitting display panel includes the features of Claim 1. Optional features of this aspect of the invention are set out in Claims 2 to 5.

[0007] In accordance with a further aspect of the invention, an organic light-emitting display apparatus includes the features of Claim 6.

[0008] In accordance with a further aspect of the invention, a voltage drop compensating method includes the features of Claim 7 and, optionally, Claim 8.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] Features will become apparent to those of skill in the art by describing in detail exemplary embodiments with reference to the attached drawings in which:

FIG. 1 illustrates an organic light-emitting display apparatus according to an embodiment of the invention;
FIG. 2 illustrates a display panel according to an embodiment of the invention;
FIG. 3 illustrates a pixel according to an embodiment of the invention;
FIGS. 4(a) and 4(b) illustrate examples of voltage drop;
FIG. 5 illustrates examples of voltage drop in according to one embodiment of the invention;
FIGS. 6(a) and 6(b) illustrate a method for compensating voltage drop according to an embodiment of the invention;
FIG. 7 illustrates a method for compensating voltage drop according to a comparative example not forming part of the present invention;
FIG. 8 illustrates operations included in a voltage drop compensating method according to an embodiment of the invention; and
FIG. 9 illustrates operations included in a voltage drop compensating method according to a comparative example not forming part of the present invention.

DETAILED DESCRIPTION

[0010] Example embodiments of the invention will now be described more fully hereinafter with reference to the

accompanying drawings; however, they may be embodied in different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey example implementations to those skilled in the art. The embodiments may be combined to form additional embodiments. Like reference numerals refer to like elements throughout.

[0011] FIG. 1 illustrates an embodiment of an organic light-emitting display apparatus 100 which includes a display panel 110, a gate driver 120, a source driver 130, a controller 140, and a source voltage generator 150.

[0012] The display panel 110 includes a display area DA having a plurality of pixels PX arranged in a matrix form. A first source voltage ELVDD and a second source voltage ELVSS are applied to the pixels PX. A voltage level of the first source voltage ELVDD is higher than that of the second source voltage ELVSS. For example, when the first source voltage ELVDD is applied to an anode of an organic light-emitting device and the second source voltage ELVSS is applied to a cathode of the organic light-emitting device, the organic light-emitting device emits light. The first source voltage ELVDD and the second source voltage ELVSS may be generated by the source voltage generator 150.

[0013] The display panel 110 also includes a plurality of gate lines GL1 to GLn through which a gate signal is applied to the pixels PX, and a plurality of source lines SL1 to SLm through which source signals are respectively applied to the pixels PX. The display panel 110 includes a power wire network for applying the first source voltage ELVDD to the pixels PX. Each of the gate lines GL1 to GLn is connected to a plurality of pixels PX arranged in the same row. Each of the source lines SL1 to SLm is connected to a plurality of pixels PX arranged in the same column. In response to the gate signal received through the gate lines GL1 to GLn, the pixels PX emit light or do not emit light according to logic levels of data signals respectively received through the source lines SL1 to SLm. In this case, the display panel 110 may operate in a digital driving scheme.

[0014] According to another example, the display panel 110 may operate in an analog driving scheme. In this case, in response to the gate signal received through the gate lines GL1 to GLn, the pixels PX may emit light at brightness corresponding to levels of data voltages or levels of currents respectively received through the source lines SL1 to SLm. For illustrative purposes only, example embodiments of the organic light-emitting display apparatus 100 of the invention operating in the digital driving scheme are described. However, other embodiments of the organic light-emitting display apparatus of the invention may operate in the analog driving scheme.

[0015] As illustrated in FIG. 1, the power wire network includes a power transfer line PTL, a power input line PIL, a connection part CN, and first and second power wires PW1 and PW2. The power transfer line PTL extends in a first direction and transfers the first source voltage ELVDD. The power input line PIL extends in the first direction and applies the first source voltage ELVDD. The connection part CN transfers the first source voltage ELVDD from the power transfer line PTL to the power input line PIL. The first and second power wires PW1 and PW2 extend in a second direction (e.g., outside the display area DA) and supply the first source voltage ELVDD to the power input line PIL.

[0016] The first and second power wires PW1 and PW2 are outside the display area DA in the second direction, which perpendicularly intersects the first direction in which the power input line PIL extends. The first power voltage ELVDD generated by the source voltage generator 150 may be directly applied to the first and second power wires PW1 and PW2. Since the first and second power wires PW1 and PW2 have a lower line resistance than that of the power input line PIL, voltage drop caused by current flow is small to be negligible. FIG. 1 illustrates that the first power wire PW1 may be disposed above the display area DA, and the second power wire PW2 may be disposed below the display area DA. In another embodiment, one or both of the power wires may be disposed on a left side and/or a right side of the display area DA, respectively on both sides, or may be disposed to surround the display area DA.

[0017] In FIG. 1, only one power input line PIL is illustrated. In the embodiment of the invention, a plurality of power input lines PIL are arranged in the display panel 110 and connected to the first and second power wires PW1 and PW2. As illustrated in FIG. 1, the power input lines PIL are connected between the first and second power wires PW1 and PW2. Each of the power input lines PIL has a first end connected to the first power wire PW1 and a second end connected to the second power wire PW2. When a power wire is disposed on the left side and/or the right side of the display area DA, the power input lines PIL may extend in a row direction (a horizontal direction in FIG. 1). When the power wire is disposed to surround the display area DA, the power input lines PIL may be arranged in a mesh form. In one embodiment, the power input lines PIL are disposed across a whole portion of the display area DA and are directly connected to the first and second power wires PW1 and PW2, so as to be connected to all the pixels PX from a pixel of a first row to a pixel of a last row in the display area DA.

[0018] In FIG. 1, only one power transfer line PTL is illustrated. In the embodiment of the invention, a plurality of power transfer lines PTL are arranged in the display panel 110 and are not directly connected to the pixels PX, unlike the power input lines PIL. As illustrated in FIG. 1, the power transfer lines PTL may extend in a column direction (a vertical direction in FIG. 1). In another embodiment, the power transfer lines PTL may extend in the row direction or may be arranged in a mesh form. In one embodiment, the power transfer lines PTL are disposed across the whole portion of the display area DA and are directly connected to the first and second power wires PW1 and PW2.

[0019] The connection part CN electrically connects the power input line PIL to the power transfer line PTL. The connection part CN is connected to a middle portion of the power transfer line PTL and the power input line PIL. In the

embodiment, the middle portion of each of the power input lines PIL corresponds to a portion adjacent to a center point of the power transfer line PTL along a lengthwise direction of the power input line PIL.

[0020] According to the example embodiment of the invention illustrated in FIG. 1, the first source voltage ELVDD generated by the source voltage generator 150 is applied to the first and second power wires PW1 and PW2 and is applied to the pixels PX through the power input line PIL. In the embodiment of the invention, the first source voltage ELVDD is applied to the first and second power wires PW1 and PW2 and is applied to the pixels PX through the power transfer line PTL, the connection part CN, and the power input line PIL. Therefore, a current I flowing through the power input line PIL may flow from the first and second power wires PW1 and PW2 to a center point of the power input line PIL.

[0021] Also, the current I flowing through the power transfer line PTL flows from the center point of the power input line PIL to the first power wire PW1 or the second power line PW2 via the connection part CN from the first and second power wires PW1 and PW2.

[0022] Since the power transfer line PTL and the power input line PIL have a resistance component, a voltage drop occurs based on a current which flows through the power transfer line PTL and the power input line PIL. Due to the voltage drop, the level of a voltage, which is applied to a pixel PX1 closest to the first power wire PW1 or a pixel PX3 closest to the second power wire PW2 among a plurality of pixels PX connected to the power input line PIL, is higher than that of a voltage applied to a plurality of pixels PX2 and PX4 disposed close to the connection part CN.

[0023] The second source voltage ELVSS generated by the source voltage generator 150 may be applied to the pixels PX through a common electrode. The common electrode may correspond to one electrode (for example, a cathode electrode) of a light-emitting device of each of the pixels PX, and all the pixels PX may be connected to the common electrode. The common electrode may be provided to completely cover the pixels PX in the display area DA. The second source voltage ELVSS may be applied from an outer portion of the display area DA to the common electrode. Since a voltage level of the second source voltage ELVSS is lower than that of the first source voltage ELVDD, a current supplied to each of the pixels PX may leak to the source voltage generator 150 through the common electrode. Therefore, a voltage level at an outer portion of the common electrode to which the second source voltage ELVSS is applied may be lower than a voltage level at a center portion of the common electrode. For example, a current may flow from the center portion of the common electrode to the outer portion of the common electrode.

[0024] Similarly to the first source voltage ELVDD in the example embodiment of FIG. 1, the second source voltage ELVSS may be applied from the upper edge and the lower edge of the display area DA to the common electrode. In another embodiment, the second source voltage ELVSS may be applied from at least one of the upper edge, power end, left side, or right side of the display area DA to the common electrode.

[0025] FIG. 2 illustrating an example of a configuration of the display panel 110 in the organic light-emitting display apparatus 100 of FIG. 1. Referring to FIG. 2, the display panel 110 includes the power input line PIL, the power transfer line PTL, and the first and second power wires PW1 and PW2. Also, the display panel 110 includes an organic light-emitting device OLED, which receives a source voltage to emit light, and one or more thin film transistors TFT that supply the source voltage to the organic light-emitting device OLED.

[0026] The power transfer line PTL extends in the first direction and receives the first source voltage ELVDD through the first and second power wires PW1 and PW2. Also, the power transfer line PTL is connected to a middle point of the power input line PIL through the connection part CN and transfers the first source voltage ELVDD to the power transfer line PTL. As illustrated in FIG. 2, a plurality of power transfer lines PTL are provided. The number of power transfer lines PTL may be different depending, for example, on the total number of pixels in and the size of the display panel 110.

[0027] The power input line PIL extends in the first direction, like the power transfer line PTL, and receives the first source voltage ELVDD through the first and second power wires PW1 and PW2. Also, the power input line PIL is connected to the power transfer line PTL at a middle point of the power input line PIL and receives the first source voltage ELVDD through the power transfer line PTL.

[0028] The first and second power wires PW1 and PW2 extends in the second direction. The first and second power wires PW1 and PW2 may be connected to the source voltage generator 150. The first source voltage ELVDD from the source voltage generator 150 is applied to the first and second power wires PW1 and PW2. The first and second power wires PW1 and PW2 are directly connected to the power transfer line PTL and the power input line PIL. The first source voltage ELVDD is applied to the power transfer line PTL and the power input line PIL through the first and second power wires PW1 and PW2 .

[0029] A current flowing through the power input line PIL may flow to the pixels PX due to the first source voltage ELVDD applied to the power input line PIL. The current supplied to each of the pixels PX flows through a pixel circuit including the thin film transistor TFT and an anode and a cathode of the organic light-emitting device OLED.

[0030] The pixels PX is directly connected to the power input line PIL, and the first source voltage ELVDD is applied to the pixels PX through the power input line PIL. As illustrated in FIG. 2, the pixels PX are not directly connected to the power transfer line PTL. Depending on the location connected to the power input line PIL, the pixels PX receive the first source voltage ELVDD directly supplied from the first power wire PW1 or the second power wire PW2 to the power input line PIL.

[0031] In the embodiment of the invention, depending on the location connected to the power input line PIL, the pixels PX receive the first source voltage ELVDD transferred through the power transfer line PTL, the connection part CN, and the power input line PIL from the first power wire PW1 or the second power wire PW2. Therefore, the first source voltage ELVDD supplied to the pixels PX will have different levels for each of the pixels PX.

[0032] For example, the level of the first source voltage ELVDD supplied to a pixel PX close to the first power wire PW1 or the second power wire PW2 will be higher than that of the first source voltage ELVDD supplied to a pixel PX close to the connection part CN. This is because the first source voltage ELVDD is supplied to the pixel PX, which is disposed close to the first power wire PW1 or the second power wire PW2, through the power input line PIL from the first power wire PW1 or the second power wire PW2. However, the first source voltage ELVDD is supplied to the pixel PX, which is disposed close to the connection part CN, via the power transfer line PTL, the connection part CN, and the power input line PIL from the first power wire PW1 or the second power wire PW2. A voltage drop therefore occurs due to resistance components of the power transfer line PTL, the power input line PIL, and the connection part CN. For this reason, the level of the first source voltage ELVDD is changed depending on the location of the pixels PX.

[0033] In FIG. 2, the first power wire PW1 connected to the power input line PIL and the first power wire PW1 connected to the power transfer line PTL are separately illustrated. However, it may be understood that the first power wire PW1 may be connected to the power input line PIL and the power transfer line PTL in common and is substantially the same wire. Also, the second power wire PW2 connected to the power input line PIL and the second power wire PW2 connected to the power transfer line PTL are separately illustrated. However, it may be understood that the second power wire PW2 may be connected to the power input line PIL and the power transfer line PTL in common and is substantially the same wire.

[0034] In FIG. 2, the cathode may be an electrode from which a current flowing in a pixel PX is output, and may be provided as the common electrode to cover all the pixels PX. Also, the second source voltage ELVSS generated by the source voltage generator 150 is applied to the cathode.

[0035] The first and second power wires PW1 and PW2 are outside the display area DA of the display panel 110. A portion of the power input line PIL and a portion of the power transfer line PTL are in the display area DA. Another portion of the power input line PIL and another portion of the power transfer line PTL are outside the display area DA. The display area DA may also include the pixels PX.

[0036] As illustrated in FIG. 2, the first source voltage ELVDD is applied from the first and second power wires PW1 and PW2 to the plurality of power input lines PIL and the plurality of power transfer lines PTL. A voltage drop, which occurs along a lengthwise direction of each of the first and second power wires PW1 and PW2, are small to negligible. Therefore, voltages applied to the first and second power wires PW1 and PW2 are the same along a lengthwise direction. Also, the levels of the first source voltage ELVDD applied to the power input lines PIL and the power transfer line PTL are the same irrespective of location.

[0037] FIG. 3 illustrates an embodiment of a pixel PX which is connected to a gate line GL of the same row and a source line SL of the same column. The pixel PX includes a pixel circuit and a light-emitting device. The pixel circuit includes a first transistor M1, a second transistor M2, and a storage capacitor Cst. The light-emitting device includes an organic light-emitting device OLED.

[0038] Each of the first and second transistors M1 and M2 may be a thin film transistor (TFT). The first transistor M1 includes a first connection terminal connected to the source line SL, a second terminal connected to a node Nd, and a control terminal connected to the gate line GL. The second transistor M2 includes a first connection terminal connected to the power input line PIL to which the first source voltage ELVDD is applied, a control terminal connected to the node Nd, and a second connection terminal connected to a first electrode of the organic light-emitting device OLED. The storage capacitor Cst may include a first terminal connected to the first connection terminal of the second transistor M, and a second terminal connected to the node Nd.

[0039] The organic light-emitting device OLED includes the first electrode connected to the second connection terminal of the second transistor M2 and a second electrode connected to a common electrode CE to which the second source voltage ELVSS is applied. The first electrode of the organic light-emitting device OLED may be an anode electrode, and the second electrode of the organic light-emitting device OLED may be a cathode electrode.

[0040] The pixel PX receives a scan signal S through the gate line GL and receives a data signal D through the source line SL. The first transistor M1 transfers the data signal D to the control terminal of the second transistor M2 in response to the scan signal S. The second transistor M2 may be turned on or off according to a logic level of the transferred data signal D. When the second transistor M2 is turned on, the second transistor M2 may transfer the first source voltage ELVDD to the first electrode of the organic light-emitting device OLED. The storage capacitor Cst may maintain a turn-on state or a turn-off state of the second transistor M2 based on the logic level of the data signal D during a subfield time period. For example, when the digital data signal D has a first logic level, the first source voltage ELVDD may be applied to the first electrode of the organic light-emitting device OLED, and the organic light-emitting device OLED may emit light. When the digital data signal D has a second logic level, the second transistor M2 may be turned off, and thus, the first source voltage ELVDD may not be applied to the first electrode of the organic light-emitting device OLED. Thus,

the organic light-emitting device OLED may not emit light. In another embodiment, the pixel PX may have a different configuration.

[0041] FIGS. 4(a) and 4(b) illustrate examples of a voltage drop when a source voltage is applied through only one of a power input line or a power transfer line. In FIGS. 4(a) and 4(b), a panel edge indicates a location where the first power wire PW1 or the second power wire PW2 is disposed, and a panel center indicates a center point of the first power wire PW1 and the second power wire PW2 (i.e. a center point is between the first power wire PW1 and the second power wire PW2). The panel edge may be a location to which a source voltage from the source voltage generator 150 is directly supplied through the first power wire PW1 or the second power wire PW2, and thus may have a highest voltage level among source voltages supplied to the display panel 110. The source voltage denotes the first source voltage ELVDD.

[0042] FIG. 4(a) illustrates a voltage drop when a source voltage is applied through only the power transfer line PTL of the display panel 110 described above with reference to FIGS. 1 and 2. When the source voltage is applied through only the power transfer line PTL, the first source voltage ELVDD is applied through the power transfer line PTL, the connection part CN, and the power input line PIL. Thus, due to voltage drop, the first source voltage ELVDD having a relatively low level is applied to a pixel PX close to the first power wire PW1 or the second power wire PW2 among a plurality of pixels PX 6 connected to the power input line PIL. The notation $ELVDD_{edge}$ denotes a first source voltage which is supplied to a pixel PX closest to the first power wire PW1 or the second power wire PW2 among a plurality of pixels PX.

[0043] Due to a resistance component of the power transfer line PTL, the level of the first source voltage ELVDD supplied through the first power wire PW1 or the second power wire PW2 is reduced, while being transferred to the connection part CN connected to a middle point of the power input line PIL through the power transfer line PTL. Also, the first source voltage ELVDD supplied to the power input line PIL through the connection part CN is continuously reduced from the middle point of the power input line PIL, towards the panel edge while being supplied to the pixels PX along a lengthwise direction. In this case, the level of the first source voltage ELVDD is nonlinearly reduced due to resistance components of the organic light-emitting device and the pixel circuit connected to the power input line PIL.

[0044] Also, in FIG. 4(a), the magnitude of voltage drop which occurs in the display panel 110 may be defined as $ELVDD - ELVDD_{edge}$.

[0045] FIG. 4(b) shows voltage drop when a source voltage is applied through only the power input line PIL of the display panel 110 described above with reference to FIGS. 1 and 2. When the source voltage is applied through only the power input line PIL, the first source voltage ELVDD is not applied through the power transfer line PTL and the connection part CN. Thus, due to voltage drop, the first source voltage ELVDD having a relatively low level may be applied to a pixel PX close to the connection part CN among a plurality of pixels PX connected to the power input line PIL.

[0046] Due to a resistance component of the power input line PIL, the level of the first source voltage ELVDD supplied through the first power wire PW1 or the second power wire PW2 is progressively reduced while being transferred through the power input line PIL. Also, a level of the first source voltage ELVDD supplied through the power input line PIL is nonlinearly reduced due to the resistance components of the organic light-emitting device and the pixel circuit connected to the power input line PIL.

[0047] Also, in FIG. 4(b), the magnitude of voltage drop which occurs in the display panel 110 may be defined as $ELVDD - ELVDD_{center}$, where $ELVDD_{center}$ denotes the level of a voltage applied to the connection part CN.

[0048] When the first source voltage ELVDD is supplied through only the power input line PIL, a current flowing to the power transfer line PTL does not need to be generated. Thus, voltage drop caused by the power transfer line PTL is be considered.

[0049] FIG. 5 illustrates an example of voltage drop in the display panel 110 according to an example embodiment of the invention. As described above with reference to FIGS. 1 and 2, in the display panel 110 the power input line PIL and the power transfer line PTL is connected to the first power wire PW1 or the second power wire PW2. Also, the first source voltage ELVDD is applied to the power input line PIL and the power transfer line PTL.

[0050] Referring to FIG. 5, the level of the first source voltage ELVDD supplied through the power transfer line PTL is linearly reduced by a resistance component of the power transfer line PTL, while the first source voltage ELVDD is being transferred from the panel edge to the panel center. Also, the level of the first source voltage ELVDD, which is supplied to the pixel PX through the power transfer line PTL, the connection part CN, and the power input line PIL, is reduced along the lengthwise direction of the power input line PIL from the center point of the power input line PIL, namely, the connection part CN. However, since the power input line PIL receives the first source voltage ELVDD from the first power wire PW1 or the second power wire PW2 as well as the power transfer line PTL, the level of the first source voltage ELVDD supplied through the power input line PIL again increases toward the panel edge.

[0051] In FIG. 5, the magnitude of voltage drop which occurs in the display panel 110 may be defined as $ELVDD - ELVDD_{min}$. The location corresponding to $ELVDD_{min}$ may be calculated based on Equation (1).

$$Location = \frac{L}{2(1+a)} \quad (1)$$

where L denotes a distance from the panel center to the panel edge, and a denotes a ratio of a resistance value of the power transfer line to a resistance value of the power input line.

[0052] FIG. 5 illustrates a case (e.g., a case where a = 1) where the resistance value of the power transfer line is the same as that of the power input line. In FIG. 5, the location where a level of the supplied first source voltage ELVDD is the minimum ($ELVDD_{min}$) is L/4.

[0053] As shown in FIG. (4a), when the first source voltage ELVDD is supplied through only the power transfer line PTL, the value "ELVDD - $ELVDD_{center}$" may be defined as V_D. Thus, the value "$ELVDD_{center}$ - $ELVDD_{edge}$" may be calculated as $V_D/2$. Therefore, in FIG. 4(a), voltage drop may be $3V_D/2$. The value "$ELVDD_{center}$ - $ELVDD_{edge}$" may be derived from accumulated voltage drop at every pixel between Panel Center and Panel Edge. The accumulated voltage drop may be calculated as,

$$nI \times r + (n-1)I \times r + \cdots + I \times r = \frac{n(n+1)}{2} I \times r \approx \frac{1}{2} nI \times nr = \frac{1}{2} V_D \ (\because n \gg 1)$$

where n denotes the number of pixels between Panel Center and Panel Edge, r denotes resistance of power input line PIL between two adjacent pixels and I denotes current flows through one pixel.

[0054] Moreover, it may be understood that voltage drop in the display panel 110 according to the example embodiment is calculated as $9V_D/32$, as shown in FIG. 5, and the display panel 100 has voltage drop of about 19%, compared to the case shown in FIG. 4(a).

[0055] The voltage drop from Panel Edge to the location corresponding to $ELVDD_{min}$ through power transfer line PTL and power input line PIL may be calculated as,

$$mI \times nr + mI \times r + (m-1)I \times r + \cdots + I \times r = mnI \times r + \frac{m(m+1)}{2} I \times r$$

where m denotes the number of pixels between Panel Center and the location of $ELVDD_{min}$, n denotes the number of pixels between Panel Center and Panel Edge, r denotes resistance of power input line PIL and power transfer line PTL between two adjacent pixels and I denotes current flows through one pixel.

[0056] The voltage drop from Panel Edge to the location corresponding to $ELVDD_{min}$ through power input line PIL may be calculated as,

$$(n-m)I \times r + (n-m-1)I \times r + \cdots + I \times r = \frac{(n-m)(n-m+1)}{2} I \times r$$

where m denotes the number of pixels between Panel Center and the location of $ELVDD_{min}$, n denotes the number of pixels between Panel Center and Panel Edge, r denotes resistance of power input line PIL between two adjacent pixels and I denotes current flows through one pixel. where m denotes the number of pixels between Panel Center and the location of $ELVDD_{min}$, n denotes the number of pixels between Panel Center and Panel Edge, r denotes resistance of power input line PIL and power transfer line PTL between two adjacent pixels and I denotes current flows through one pixel.

[0057] The voltage drop from Panel Edge to the location corresponding to $ELVDD_{min}$ through power transfer line PTL and power input line PIL and the voltage drop from Panel Edge to the location corresponding to $ELVDD_{min}$ through power input line PIL are the same, it may be derived as,

$$m = \frac{n+1}{4n+2} n \approx \frac{1}{4} n \ (\because n \gg 1)$$

[0058] Using the relationship between m and n, the voltage drop from Panel Edge to the location corresponding to $ELVDD_{min}$ through power transfer line PTL and power input line PIL may be simplified as,

$$mnI \times r + \frac{m(m+1)}{2} I \times r \approx mnI \times r + \frac{1}{2} m^2 I \times r \ (\because m \gg 1)$$

$$\approx \frac{1}{4} nI \times nr + \frac{1}{32} nI \times nr = \frac{1}{4} V_D + \frac{1}{32} V_D$$

[0059] As the voltage drop value increases, a larger compensation margin may be required for image data. When the compensation margin is large (e.g., above a predetermined value), compensation time increases. Thus, an emission duty cycle may be relatively or proportionately reduced. Therefore, the level of a source voltage may increase for emitting light at a sufficient luminance for a short time. When a higher source voltage is supplied, power consumption increases.

[0060] Moreover, in generating compensation data for compensating voltage drop, as the voltage drop value increases (e.g., as a deviation of a source voltage applied to a plurality of pixels increases), the probability that an error will occur in generating the compensation data increases.

[0061] To solve such problems, it is important to reduce a voltage drop value. The display panel 110 according to embodiment of the invention supplies a source voltage through the power input line and the power transfer line, thereby decreasing a source voltage deviation between a plurality of pixels caused by voltage drop.

[0062] FIGS. 6(a) and 6(b) illustrates an embodiment of a method for compensating voltage drop in an organic light-emitting display panel according to the invention. In FIGS. 6(a) and 6(b), the panel edge denotes the first power wire PW1 or the second power wire PW2, and the panel center denotes a center point of the first power wire PW1 and the second power wire PW2.

[0063] FIG. 6(a) shows measuring the voltage at the panel center when the power transfer line PTL is disconnected from the first power wire PW1 and the second power wire PW2 and the first source voltage ELVDD is supplied through the power input line PIL. A voltage illustrated as a dashed line denotes a voltage (IRD calculated V) in which voltage drop calculated based on resistance components of the power input line PIL and the power transfer line PTL is reflected. Also, a voltage illustrated as a solid line denotes a corrected voltage (IRD corrected V) in which a voltage value obtained by measuring a panel center voltage is reflected. This is to say the voltage (IRD corrected V) illustrated as the dashed line denotes a predicted voltage. Here, the panel center voltage $ELVDD_{center}$ may be obtained by measuring a voltage applied to the power transfer line PTL, instead of measuring the panel center voltage. This is possible, as a current flowing to the power transfer line PTL does not occur, and a resistance of the connection part CN that connects the power transfer line PTL to the power input line PIL is negligible, such that, the level of the panel center voltage $ELVDD_{center}$ is almost equal to that of a voltage applied to the power transfer line PTL.

[0064] The difference between the panel center voltage $ELVDD_{center}$ and a voltage (hereinafter referred to as ELVDD) measured from the panel edge may be defined based on Equation (2).

$$ELVDD - ELVDD_{center} = \frac{V_D}{2a} \qquad (2)$$

where a denotes a ratio of a resistance value of the power transfer line to a resistance value of the power input line.

[0065] FIG. 6(b) shows that when the power input line PIL is disconnected from the first power wire PW1 and the second power wire PW2 and the first source voltage ELVDD is supplied through the power transfer line PTL, the voltage at the panel edge is measured. Since it may be difficult to measure the panel center voltage $ELVDD_{center}$ without a separate measurement line, the voltage at the panel edge may be measured, and a level of a source voltage applied to the power transfer line PTL may be corrected by reflecting a difference between a predicted voltage (IRD calculated V) and the measured voltage.

[0066] The difference between the first source voltage ELVDD and the panel center voltage $ELVDD_{center}$ and a difference between the panel center voltage $ELVDD_{center}$ and the panel edge voltage $ELVDD_{edge}$ may be determined based on Equation (3)

$$\begin{aligned} ELVDD - ELVDD_{center} &= V_D \\ ELVDD_{center} - ELVDD_{edge} &= \frac{V_D}{2a} \end{aligned} \qquad (3)$$

where a denotes a ratio of a resistance value of the power transfer line to a resistance value of the power input line.

[0067] Equation (4) may be obtained from Equations (2) and (3).

$$ELVDD - ELVDD_{edge} = \frac{V_D}{2a} + V_D \quad (4)$$

where the left term denotes a value which is known through direct measurement, and a first order of the right term denotes a value which is known through direct measurement as in Equation (2). Therefore, the value "V_D" may be calculated. Also, the value "a" may be calculated by substituting the calculated value "V_D" into Equation (2) or (4).

[0068] As described above, the value "a" denotes the ratio of a resistance value of the power transfer line to a resistance value of the power input line. Since the resistance components of the power input line and the power transfer line are the largest factors causing voltage drop, the ratio (e.g., the value "a") becomes a variable that may be used to calculate a voltage drop compensation value in the display panel. Therefore, an actual value "a" may be calculated through the method in FIG. 6, and the accuracy of voltage drop compensation may be enhanced by reflecting the calculated actual value "a".

[0069] FIG. 7 illustrates a comparative example not forming part of the present invention of a method for compensating voltage drop in an organic light-emitting display panel. In FIG. 7, a voltage change curve is the same as a voltage change curve in FIG. 5.

[0070] The voltage drop compensating method in FIG. 7 may directly measure a panel center voltage $ELVDD_{center}$ through a voltage measurement line used to measure the panel center voltage $ELVDD_{center}$. The difference between the first source voltage ELVDD and the panel center voltage $ELVDD_{center}$ may be based on Equation (5)

$$ELVDD - ELVDD_{edge} = \frac{aV_D}{2(a+1)} \quad (5)$$

where V_D denotes a voltage which is calculated by using a resistance of the power transfer line and a current flowing through the power input line, and a denotes a ratio of a resistance value of the power transfer line to a resistance value of the power input line.

[0071] The resistance of the power transfer line may be calculated using the level of a current, which flows from the first power wire PW1 or the second power wire PW2 to the connection part CN, and the potential difference between the first source voltage ELVDD and the panel center voltage $ELVDD_{center}$. Also, the level of a current flowing through the power input line PIL may have the same value as a total sum of currents which respectively flow in the pixels PX in the display panel.

[0072] A variety of methods may be used to measure the level of current. For example, a method may be used which measures and sums levels of currents respectively input to the pixels PX, or a method may be used which measures and sums levels of currents which respectively flow in the power input lines PIL.

[0073] In Equation (5), V_D of a left term and V_D of a right term may be calculated by direct measurement. Thus, the value "a" in Equation (5) may be calculated. As shown in FIG. 6, the actual value "a" may be calculated and reflected, thereby enhancing the accuracy of voltage drop compensation. Moreover, the location where the first source voltage is minimum may be calculated by substituting the calculated actual value "a" into Equation (1).

[0074] FIG. 8 is a flowchart illustrating operations included in an embodiment of a voltage drop compensating method for an organic light-emitting display panel. The display panel includes a power input line which extends in a first direction and through which a source voltage is applied, a power transfer line which extends in the first direction and is connected to a center point of the power input line to transfer the source voltage to the power input line, and first and second power wires which supply the source voltage to the power input line and the power transfer line. The organic light-emitting display panel corresponds, for example, to the display panel 100.

[0075] Referring to FIG. 8, the method includes a first operation S110 of disconnecting the power transfer line from the first and second power wires, second operation S120 of measuring a level of a voltage applied to the power transfer line, third operation S130 of connecting the first and second power wires to the power transfer line and disconnecting the first and second power wires from the power input line, fourth operation S140 of measuring a level of a voltage at one end of the power input line, and fifth operation S150 of calculating a ratio of a resistance value of the power transfer line to a resistance value of the power input line.

[0076] The flowchart of FIG. 8 corresponds to the method of FIG. 6. First operation S110 denotes the source voltage supplied through only the power input line. In second operation S120, it may be understood that measuring the level of a voltage applied to the power transfer line is to perform the same measurement as measurement of a panel center voltage. Therefore, the value expressed in Equation (2) may be calculated through first operation S110 and second operation S120.

[0077] Operation S130 denotes the source voltage supplied through only the power transfer line. In fourth operation S140, it may be understood that measuring a voltage at one end of the power input line is to measure a panel edge voltage. Therefore, the value expressed in Equation (3) may be calculated through third operation S130 and fourth operation S140.

[0078] In fifth operation S150, the ratio may be calculated based on a difference between the source voltage and the voltage measured through second operation S120 and a difference between the source voltage and the voltage measured through fourth operation S140. For example, in fifth operation S150, the ratio (the value "a" in Equations (2) to (4)), namely, the ratio of a resistance value of the power transfer line to a resistance value of the power input line, may be calculated by substituting the values calculated through Equations (2) and (3) into Equation (4).

[0079] The ratio calculated through an actual measurement may be applied to a voltage drop compensating equation obtained by reflecting a resistance component of the organic light-emitting display panel, thereby enhancing accuracy of voltage drop compensation.

[0080] FIG. 9 is a flowchart illustrating a comparative example not forming part of the present invention of a voltage drop compensating method for an organic light-emitting display panel. The organic light-emitting display panel includes a power input line which extends in a first direction and through which a source voltage is applied, a power transfer line which extends in the first direction and is connected to a center point of the power input line to transfer the source voltage to the power input line, a voltage measurement line that measures a voltage at the center point of the power input line, and first and second power wires which supply the source voltage to the power input line and the power transfer line. The organic light-emitting display panel is, for example, the display panel 100.

[0081] Referring to FIG. 9, the method includes an operation S210 of measuring a resistance of the power transfer line, operation S220 of measuring a voltage at the center point of the power input line by using the voltage measurement line, operation S230 of measuring a level of a current which flows through the power input line, and operation S240 of calculating a ratio of a resistance value of the power transfer line to a resistance value of the power input line.

[0082] In operation S210, the resistance of the power transfer line may be calculated based on a level of current, which flows from the first or second power wire to a center point of the power transfer line, and a potential difference between the first source voltage ELVDD and the panel center voltage $ELVDD_{center}$. A different resistance measurement method may be used in another embodiment.

[0083] In operation S220, the voltage at the center point (e.g., a point where the power input line is connected to the power transfer line) of the power input line may be directly measured using the voltage measurement line. The voltage measured through operation S220 may be the panel center voltage described above with reference to FIGS. 6 and 7.

[0084] In operation S230, the level of current flowing in the power input line may be measured by summing all currents which respectively flow in a plurality of pixels in the organic light-emitting display panel. In one embodiment, a method of measuring and summating all levels of currents flowing in a plurality of the power input lines may be used.

[0085] In operation S240, the ratio may be calculated based on Equation (6)

$$ELVDD - ELVDD_{center} = \frac{aV_D}{2(a+1)} \qquad (6)$$

where ELVDD denotes the source voltage, $ELVDD_{center}$ denotes the voltage measured through operation S220, V_D denotes a voltage which is calculated by using a resistance of the power transfer line and the current measured through operation S230, and a denotes the ratio.

[0086] In Equation (6), V_D may be calculated by multiplying the resistance value measured through operation S210 and the current value measured through operation S230. As a result, the ratio (the value "a") in Equation (6) may be calculated. Also, the ratio (the value "a") calculated through an actual measurement may be applied to a voltage drop compensating equation which is obtained by reflecting a resistance component of the organic light-emitting display panel, thereby enhancing the accuracy of voltage drop compensation.

[0087] According to the one or more of the above exemplary embodiments, an organic light-emitting display panel, an organic light-emitting display apparatus, and a voltage drop compensating method decrease luminance deviation caused by a voltage drop of a source voltage line.

[0088] Example embodiments of the invention have been disclosed herein, and although specific terms are employed, they are used and are to be interpreted in a generic and descriptive sense only and not for purpose of limitation. In some instances, as would be apparent to a skilled person in the art, features, characteristics, and/or elements described in connection with a particular embodiment may be used singly or in combination with features, characteristics, and/or elements described in connection with other embodiments unless otherwise indicated. Accordingly, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the scope of the invention as set forth in the following claims.

Claims

1. An organic light-emitting display panel (110), comprising:

N power input lines (PIL) extending in a first direction of a display area (DA);
N power transfer lines (PTL) extending in the first direction;
a first power wire (PW1) and a second power wire (PW2) extending in a second direction outside the display area (DA), the second direction being perpendicular to the first direction, the first power wire (PW1) and the second power wire (PW2) each being directly connected to both the N power input lines (PIL) and the N power transfer lines (PTL), wherein the first power wire (PW1) and the second power wire (PW2) are positioned at opposite ends of the N power input lines (PIL) and at opposite ends of the N power transfer lines (PTL);
a plurality of pixels (PX) arranged in a matrix in the display area (DA), the pixels being arranged in N columns extending in the first direction, the pixels in each column being connected to a respective one of the N power input lines (PIL); and
N connection parts (CN), wherein each of the N power transfer lines (PTL) is connected to a respective one of the N power input lines (PIL) via a respective one of the N connection parts (CN) and wherein each of the N connection parts (CN) is directly connected to the center point of the respective power transfer line (PTL) and to the center point of the respective power input line (PIL);
wherein the pixels (PX) are indirectly connected to the N power transfer lines (PTL) via the N connection parts (CN) and the N power input lines (PIL);
characterized in that
the N power transfer lines (PTL) are not directly connected to any of the said pixels (PX) such that the only connection between each of said pixels (PX) and said N power transfer lines (PTL) is formed by a respective one of said N power input lines (PIL), a respective one of said N connection parts (CN) and said first and second power wires (PW1, PW2).

2. The panel according to claim 1, wherein the organic light-emitting display panel further comprises a common electrode connected to each pixel (PX).

3. The panel according to claim 2, wherein each of the pixels (PX) includes:

a pixel circuit; and
a light-emitting device that includes a first electrode connected to the pixel circuit and the common electrode.

4. The panel according to claim 3, wherein:

the first electrode is an anode electrode, and
the common electrode is a cathode electrode.

5. The panel according to claim 3 or claim 4, further comprising:

a plurality of gate lines (GL1-GLn);
a plurality of source lines (SL1-CLm);

wherein the pixel circuit includes:

a first thin film transistor (M1) configured to be turned on by a scan signal (S) applied through a gate line (GL) and to transfer a data signal applied through a source line (SL);
a second thin film transistor (M2) configured to be turned on according to a logic level of the data signal and to transfer a first source voltage (ELVDD) to the light-emitting device; and
a capacitor (Cst) configured to maintain a turn-on state or a turn-off state of the second thin film transistor (FL2) based on a logic level of the data signal during a subfield time period;

6. An organic light-emitting display apparatus, comprising:

a source voltage generator (150) configured to generate a first source voltage (ELVDD) and a second source voltage (ELVSS) having a lower voltage level than a level of the first source voltage (ELVDD), to provide the first source voltage (ELVDD) to the first and second power wires (PW1, PW2) and to provide the second source

voltage (ELVSS) to the common electrode; and
the organic light-emitting display panel (110) according to any of claims 2 to 5.

7. A voltage drop compensating data determining method for the organic light-emitting display panel (110) according to claim 1 the voltage drop compensating method comprising:

(a) applying the first source voltage (ELVDD) via the first and second power wires (PW1, PW2) and a second source voltage (ELVSS) to the pixels (PX);
(b) disconnecting the N power transfer lines (PTL) from the first and second power wires (PW1, PW2);
(c) determining a level of a voltage at a center point of the N power input lines (PIL) by measuring a level of a voltage applied to the N power transfer lines (PTL);
(d) calculating a difference between a level of the first source voltage (ELVDD) and a level of the voltage determined in step (c);
(e) connecting the first and second power wires (PW1, PW2) to the N power transfer lines (PTL) and disconnecting the first and second power wires (PW1, PW2) from the N power input lines (PIL);
(f) measuring a level of a voltage at one end of the N power input lines (PIL); and
(g) calculating a ratio of a resistance value of the N power transfer lines (PTL) to a resistance value of the N power input lines (PIL) based on the following Equation:

$$ELVDD - EVLDD_{edge} = \frac{V_D}{2a} + V_D$$

wherein ELVDD denotes the first source voltage, $ELVDD_{edge}$ denotes the voltage measured at step (f), $V_D/2a$ denotes a voltage calculated at step (d) and a denotes the ratio.

8. A method according to claim 7, wherein the step of calculating the ratio includes:
calculating the ratio based on a difference between the first source voltage (ELVDD) and the voltage, which is measured in the step of measuring the level of the voltage applied to the power transfer line (PTL), and a difference between the first source voltage (ELVDD) and the voltage which is measured in the step of measuring the level of the voltage at the one end of the N power input lines (PIL).

Patentansprüche

1. Organisches Leuchtanzeigefeld (110), umfassend:

N Stromeingangsleitungen (PIL), die sich in einer ersten Richtung eines Anzeigebereichs (DA) erstrecken;
N Stromübertragungsleitungen (PTL), die sich in der ersten Richtung erstrecken;
einen ersten Stromversorgungsdraht (PW1) und einen zweiten Stromversorgungsdraht (PW2), die sich in einer zweiten Richtung außerhalb des Anzeigebereichs (DA) erstrecken, wobei die zweite Richtung senkrecht zu der ersten Richtung ist, wobei der erste Stromversorgungsdraht (PW1) und der zweite Stromversorgungsdraht (PW2) jeweils direkt sowohl mit den N Stromeingangsleitungen (PIL) als auch mit den N Stromübertragungsleitungen (PTL) verbunden sind, worin der erste Stromversorgungsdraht (PW1) und der zweite Stromversorgungsdraht (PW2) an gegenüberliegenden Enden der N Stromeingangsleitungen (PIL) und an gegenüberliegenden Enden der N Stromübertragungsleitungen (PTL) angeordnet sind;
eine Vielzahl von Pixeln (PX), die im Anzeigebereich (DA) in einer Matrix angeordnet sind, wobei die Pixel in N Spalten angeordnet sind, die sich in der ersten Richtung erstrecken, wobei die Pixel in jeder Spalte mit einer jeweiligen der N Stromeingangsleitungen (PIL) verbunden sind; und
N Verbindung steile (CN), wobei jede der N Stromübertragungsleitungen (PTL) mit einer jeweiligen der N Stromeingangsleitungen (PIL) über einen jeweiligen der N Verbindungsteile (CN) verbunden ist und wobei jeder der N Verbindungsteile (CN) direkt mit dem Mittelpunkt der jeweiligen Stromübertragungsleitung (PTL) und mit dem Mittelpunkt der jeweiligen Stromeingangsleitung (PIL) verbunden ist;
wobei die Pixel (PX) über die N Verbindungsteile (CN) und die N Stromeingangsleitungen (PIL) indirekt mit den N Stromübertragungsleitungen (PTL) verbunden sind;

dadurch gekennzeichnet, dass
die N Stromübertragungsleitungen (PTL) nicht direkt mit einem der Pixel (PX) verbunden sind, sodass die einzige

Verbindung zwischen jedem der Pixel (PX) und den N Stromübertragungsleitungen (PTL) durch eine jeweilige der N Stromeingangsleitungen (PIL), einen jeweiligen der N Verbindungsteile (CN) und den ersten und den zweiten Stromversorgungsdraht (PW1, PW2) gebildet wird.

2. Feld nach Anspruch 1, wobei das organische Leuchtanzeigefeld ferner eine gemeinsame Elektrode umfasst, die mit jedem Pixel (PX) verbunden ist.

3. Feld nach Anspruch 2, wobei jedes der Pixel (PX) Folgendes einschließt:

eine Pixelschaltung; und
eine Leuchtvorrichtung, die eine erste Elektrode einschließt, die mit der Pixelschaltung und der gemeinsamen Elektrode verbunden ist.

4. Feld nach Anspruch 3, wobei:

die erste Elektrode eine Anodenelektrode ist, und
die gemeinsame Elektrode eine Kathodenelektrode ist.

5. Feld nach Anspruch 3 oder Anspruch 4, ferner umfassend:

eine Vielzahl von Gate-Leitungen (GL1-GLn);
eine Vielzahl von Source-Leitungen (SL1-SLm);
wobei die Pixelschaltung Folgendes einschließt:

einen ersten Dünnschichttransistor (M1), der dafür konfiguriert ist, durch ein über eine Gate-Leitung (GL) angelegtes Rastersignal (S) eingeschaltet zu werden und ein über eine Source-Leitung (SL) angelegtes Datensignal zu übertragen;
einen zweiten Dünnschichttransistor (M2), der dafür konfiguriert ist, gemäß einem Logikpegel des Datensignals eingeschaltet zu werden und eine erste Source-Spannung (ELVDD) zu der Leuchtvorrichtung zu übertragen; und
einen Kondensator (Cst), der dafür konfiguriert ist, einen Einschaltzustand oder einen Ausschaltzustand des zweiten Dünnschichttransistors (M2) auf der Grundlage eines Logikpegels des Datensignals während eines Teilfeldzeitabschnitts beizubehalten;

6. Organische Leuchtanzeigevorrichtung, umfassend:

einen Source-Spannungsgenerator (150), der dafür konfiguriert ist, eine erste Source-Spannung (ELVDD) und eine zweite Source-Spannung (ELVSS) mit einem niedrigeren Spannungspegel als einem Pegel der ersten Source-Spannung (ELVDD) zu erzeugen, um die erste Source-Spannung (ELVDD) für den ersten und den zweiten Stromversorgungsdraht (PW1, PW2) bereitzustellen und die zweite Source-Spannung (ELVSS) für die gemeinsame Elektrode bereitzustellen; und
das organische Leuchtanzeigefeld (110) nach einem der Ansprüche 2 bis 5.

7. Verfahren zum Bestimmen von Daten zur Kompensation des Spannungsabfalls für das organische Leuchtanzeigefeld (110) nach Anspruch 1, wobei das Verfahren zur Kompensation des Spannungsabfalls umfasst:

(a) Anlegen der ersten Source-Spannung (ELVDD) über den ersten und den zweiten Stromversorgungsdraht (PW1, PW2) und einer zweiten Source-Spannung (ELVSS) an die Pixel (PX);
(b) Trennen der N Stromübertragungsleitungen (PTL) vom ersten und vom zweiten Stromversorgungsdraht (PW1, PW2);
(c) Bestimmen eines Pegels einer Spannung an einem Mittelpunkt der N Stromeingangsleitungen (PIL) durch Messen eines Pegels einer an die N Stromübertragungsleitungen (PTL) angelegten Spannung;
(d) Berechnen einer Differenz zwischen einem Pegel der ersten Source-Spannung (ELVDD) und einem Pegel der in Schritt (c) bestimmten Spannung;
(e) Verbinden des ersten und des zweiten Stromversorgungsdrahts (PW1, PW2) mit den N Stromübertragungsleitungen (PTL) und Trennen des ersten und des zweiten Stromversorgungsdrahts (PW1, PW2) von den N Stromeingangsleitungen (PIL);
(f) Messen eines Pegels einer Spannung an einem Ende der N Stromeingangsleitungen (PIL); und

(g) Berechnen eines Verhältnisses eines Widerstandswerts der N Stromübertragungsleitungen (PTL) zu einem Widerstandswert der N Stromeingangsleitungen (PIL) auf der Grundlage der folgenden Gleichung:

$$ELVDD - EVLDD_{edge} = \frac{V_D}{2a} + V_D$$

wobei ELVDD die erste Source-Spannung bezeichnet, $ELVDD_{edge}$ die in Schritt (f) gemessene Spannung bezeichnet, $V_D/2a$ eine in Schritt (d) berechnete Spannung bezeichnet und a das Verhältnis bezeichnet.

8. Verfahren nach Anspruch 7, wobei der Schritt des Berechnens des Verhältnisses Folgendes einschließt:

Berechnen des Verhältnisses auf der Grundlage einer Differenz zwischen der ersten Source-Spannung (ELVDD) und der Spannung, die in dem Schritt des Messens des Pegels der an die Stromübertragungsleitung (PTL) angelegten Spannung gemessen wird, und einer Differenz zwischen der ersten Source-Spannung (ELVDD) und der Spannung, die in dem Schritt des Messens des Pegels der Spannung an dem einen Ende der N Stromeingangsleitungen (PIL) gemessen wird.

Revendications

1. Panneau d'affichage électroluminescent organique (110), comprenant :

N lignes d'entrée de puissance (PIL) qui s'étendent dans une première direction d'une zone d'affichage (DA) ;
N lignes de transfert de puissance (PTL) qui s'étendent dans la première direction ;
un premier fil de puissance (PW1) et un second fil de puissance (PW2) qui zs'étendent dans une seconde direction à l'extérieur de la zone d'affichage (DA), la seconde direction étant perpendiculaire à la première direction, le premier fil de puissance (PW1) et le second fil de puissance (PW2) étant chacun connectés directement à la fois aux N lignes d'entrée de puissance (PIL) et aux N lignes de transfert de puissance (PTL), dans lequel le premier fil de puissance (PW1) et le second fil de puissance (PW2) sont positionnés au niveau d'extrémités opposées des N lignes d'entrée de puissance (PIL) et au niveau d'extrémités opposées des N lignes de transfert de puissance (PTL) ;
une pluralité de pixels (PX) qui sont agencés dans une matrice dans la zone d'affichage (DA), les pixels étant agencés dans N colonnes qui s'étendent dans la première direction, les pixels dans chaque colonne étant connectés à l'une respective des N lignes d'entrée de puissance (PIL) ; et
N parties de connexion (CN), dans lequel chacune des N lignes de transfert de puissance (PTL) est connectée à l'une respective des N lignes d'entrée de puissance (PIL) via l'une respective des N parties de connexion (CN) et dans lequel chacune des N parties de connexion (CN) est connectée directement au point central de la ligne de transfert de puissance respective (PTL) et au point central de la ligne d'entrée de puissance respective (PIL) ;
dans lequel les pixels (PX) sont connectés indirectement aux N lignes de transfert de puissance (PTL) via les N parties de connexion (CN) et aux N lignes d'entrée de puissance (PIL) ;

caractérisé en ce que :

les N lignes de transfert de puissance (PTL) ne sont pas connectées directement à l'un quelconque desdits pixels (PX) de telle sorte que la seule connexion entre chacun desdits pixels (PX) et lesdites N lignes de transfert de puissance (PTL) est formée par l'une respective desdites N lignes d'entrée de puissance (PIL), par l'une respective desdites N parties de connexion (CN) et par lesdits premier et second fils de puissance (PW1, PW2).

2. Panneau selon la revendication 1, dans lequel le panneau d'affichage électroluminescent organique comprend en outre une électrode commune qui est connectée à chaque pixel (PX).

3. Panneau selon la revendication 2, dans lequel chacun des pixels (PX) inclut :

un circuit de pixel ; et
un dispositif électroluminescent qui inclut une première électrode qui est connectée au circuit de pixel et à l'électrode commune.

4. Panneau selon la revendication 3, dans lequel :

la première électrode est une électrode d'anode ; et
l'électrode commune est une électrode de cathode.

5. Panneau selon la revendication 3 ou la revendication 4, comprenant en outre :

une pluralité de lignes de grille (GL1-GLn) ; et
une pluralité de lignes de source (SL1-SLm) ;
dans lequel le circuit de pixel inclut :

un premier transistor à film mince (M1) qui est configuré pour être rendu passant par un signal de balayage (S) qui est appliqué par l'intermédiaire d'une ligne de grille (GL) et pour transférer un signal de données qui est appliqué par l'intermédiaire d'une ligne de source (SL) ;
un second transistor à film mince (M2) qui est configuré pour être rendu passant en fonction d'un niveau logique du signal de données et pour transférer une première tension de source (ELVDD) au dispositif électroluminescent ; et
un condensateur (Cst) qui est configuré pour maintenir un état passant ou un étatbloqué du second transistor à film mince (M2) sur la base d'un niveau logique du signal de données pendant une période temporelle de sous-trame.

6. Appareil d'affichage électroluminescent organique, comprenant :

un générateur de tension de source (150) qui est configuré pour générer une première tension de source (ELVDD) et une seconde tension de source (ELVSS) qui présente un niveau de tension plus faible qu'un niveau de la première tension de source (ELVDD), pour appliquer la première tension de source (ELVDD) sur les premier et second fils de puissance (PW1, PW2) et pour appliquer la seconde tension de source (ELVSS) sur l'électrode commune ; et
le panneau d'affichage électroluminescent organique (110) selon l'une quelconque des revendications 2 à 5.

7. Procédé de détermination de données de compensation de chute de tension pour le panneau d'affichage électroluminescent organique (110) selon la revendication 1, le procédé de compensation de chute de tension comprenant :

(a) l'application de la première tension de source (ELVDD) via les premier et second fils de puissance (PW1, PW2) et d'une seconde tension de source (ELVSS) sur les pixels (PX) ;
(b) la déconnexion des N lignes de transfert de puissance (PTL) des premier et second fils de puissance (PW1, PW2) ;
(c) la détermination d'un niveau d'une tension au niveau d'un point central des N lignes d'entrée de puissance (PIL) en mesurant un niveau d'une tension qui est appliquée sur les N lignes de transfert de puissance (PTL) ;
(d) le calcul d'une différence entre un niveau de la première tension de source (ELVDD) et un niveau de la tension qui est déterminé au niveau de l'étape (c) ;
(e) la connexion des premier et second fils de puissance (PW1, PW2) aux N lignes de transfert de puissance (PTL) et la déconnexion des premier et second fils de puissance (PW1, PW2) des N lignes d'entrée de puissance (PIL) ;
(f) la mesure d'un niveau d'une tension au niveau d'une extrémité des N lignes d'entrée de puissance (PIL) ; et
(g) le calcul d'un rapport d'une valeur de résistance des N lignes de transfert de puissance (PTL) sur une valeur de résistance des N lignes d'entrée de puissance (PIL) sur la base de l'équation qui suit :

$$ELVDD - EVLDD_{edge} = \frac{V_D}{2a} + V_D$$

dans laquelle ELVDD représente la première tension de source, $ELVDD_{edge}$ représente la tension qui est mesurée au niveau de l'étape (f), $V_D/2a$ représente une tension qui est calculée au niveau de l'étape (d) et a représente le rapport.

8. Procédé selon la revendication 7, dans lequel l'étape de calcul du rapport inclut :

le calcul du rapport sur la base d'une différence entre la première tension de source (ELVDD) et la tension qui est mesurée au niveau de l'étape de mesure du niveau de la tension qui est appliquée sur la ligne de transfert de puissance (PTL), et d'une différence entre la première tension de source (ELVDD) et la tension qui est mesurée au niveau de l'étape de mesure du niveau de la tension au niveau de l'extrémité considérée des N lignes d'entrée de puissance (PIL).

FIG. 1

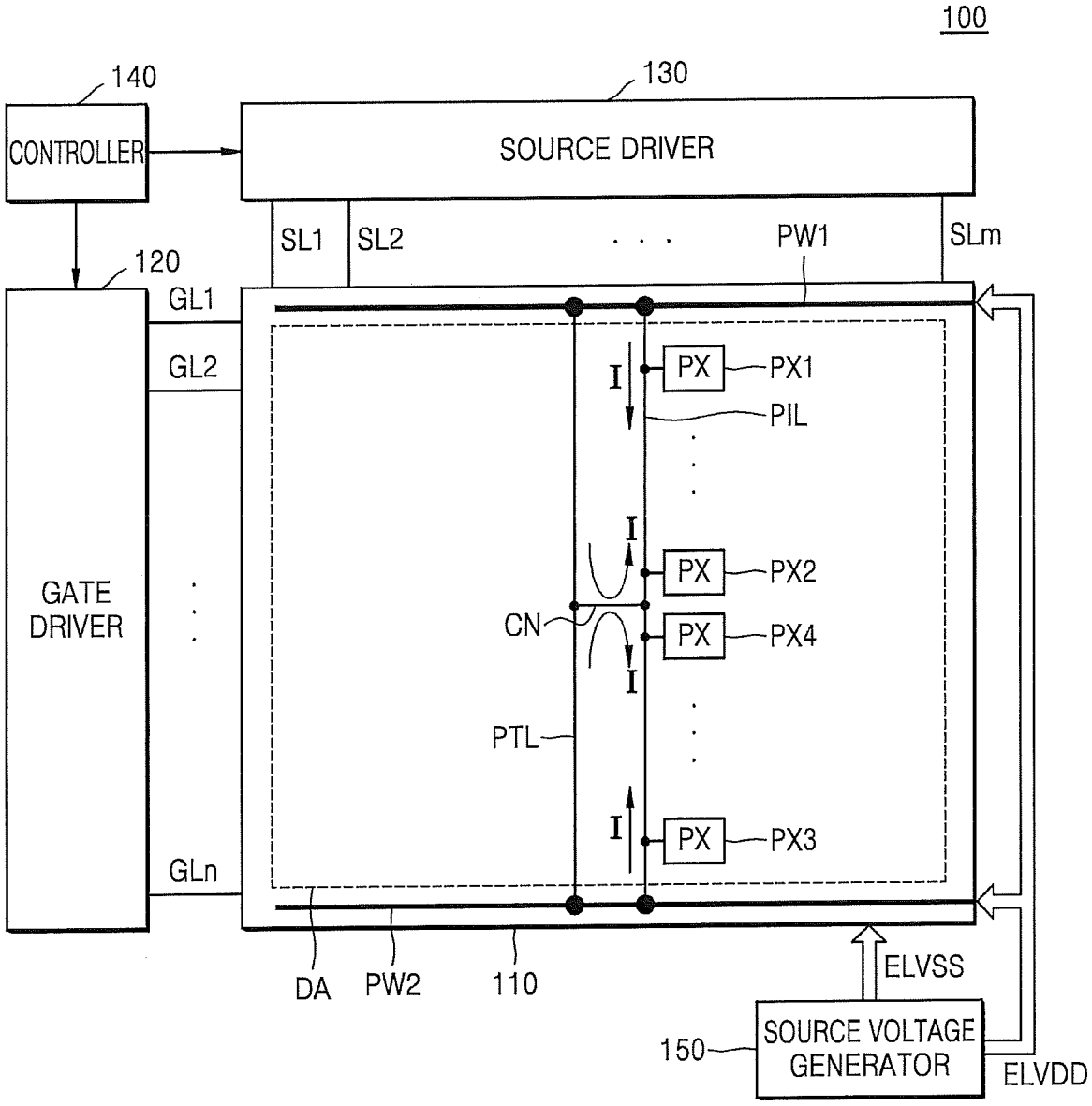

100
140
CONTROLLER
130
SOURCE DRIVER
SL1
SL2
PW1
SLm
120
GL1
GL2
GATE DRIVER
GLn
I
PX
PX1
PIL
PX2
CN
PX4
PTL
PX3
DA
PW2
110
ELVSS
150
SOURCE VOLTAGE GENERATOR
ELVDD

FIG. 2

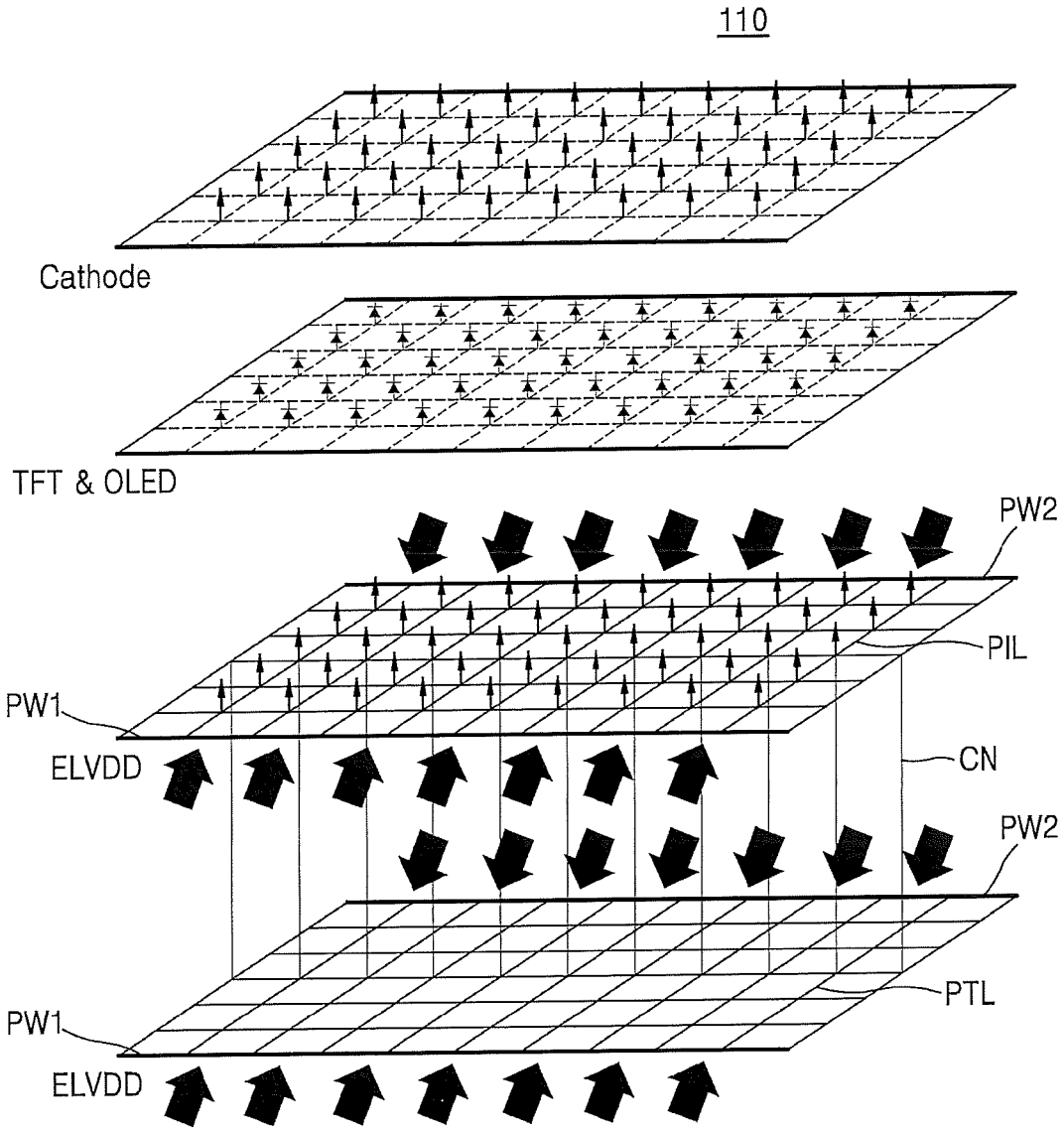


FIG. 3

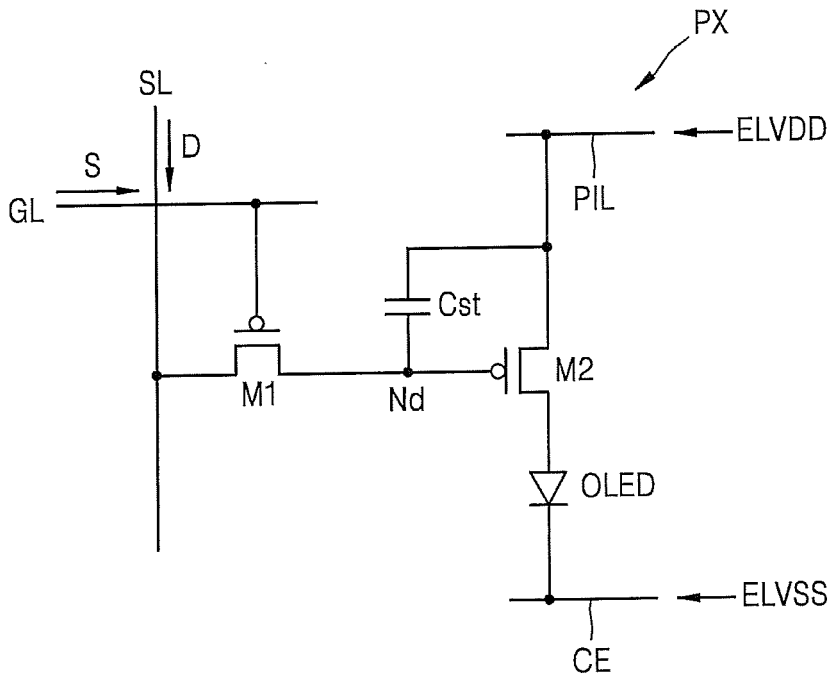


FIG. 4(a)

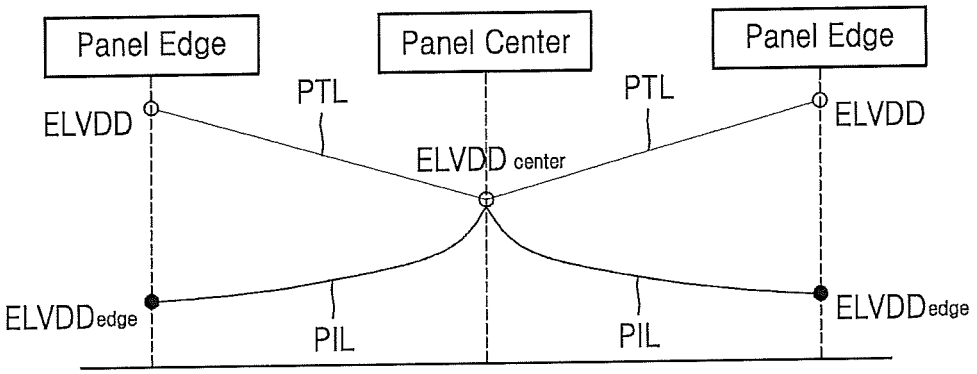

Panel Edge
Panel Center
Panel Edge
ELVDD
PTL
PTL
ELVDD
ELVDD center
ELVDDedge
PIL
PIL
ELVDDedge

FIG. 4(b)

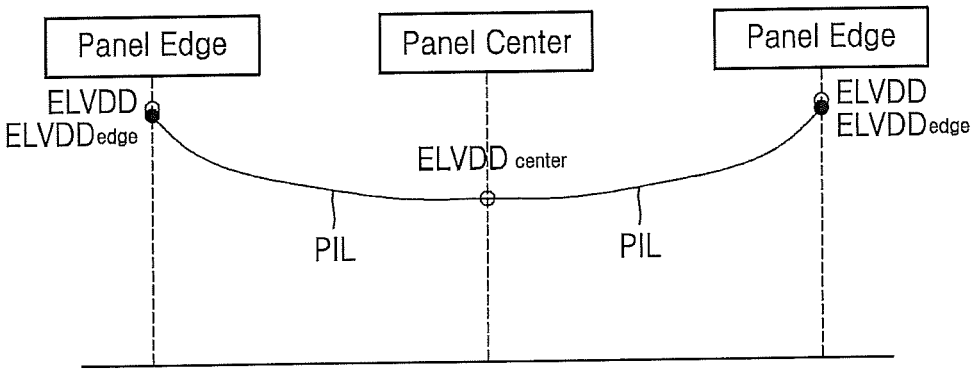

Panel Edge
Panel Center
Panel Edge
ELVDD
ELVDDedge
ELVDD center
ELVDD
ELVDDedge
PIL
PIL

FIG. 5

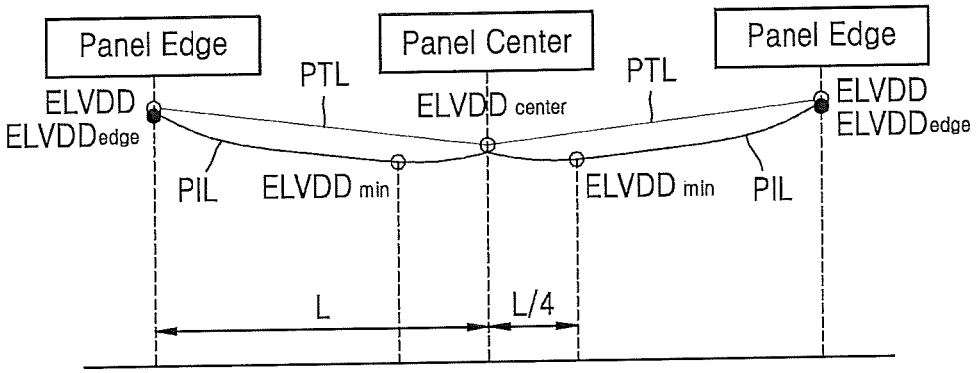

Panel Edge
Panel Center
Panel Edge
PTL
PTL
ELVDD
ELVDDedge
ELVDD center
ELVDD
ELVDDedge
PIL
ELVDD min
ELVDD min
PIL
L
L/4

FIG. 6(a)

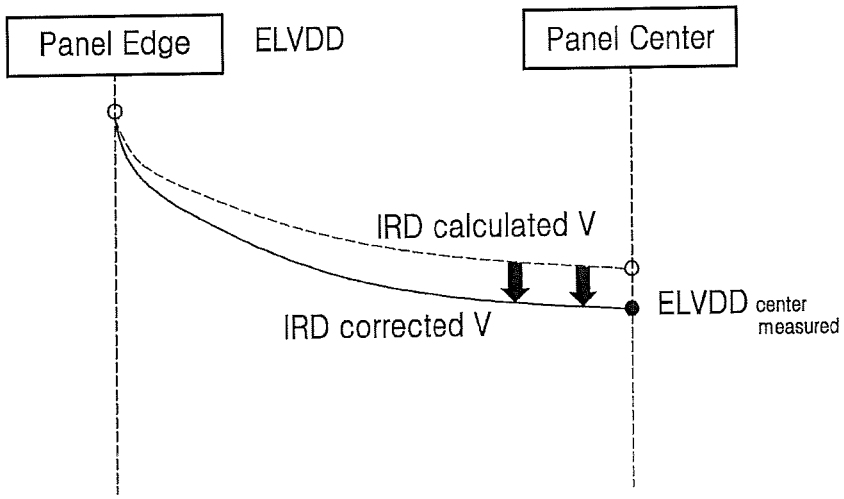

Panel Edge
ELVDD
Panel Center
IRD calculated V
IRD corrected V
ELVDD center measured

FIG. 6(b)

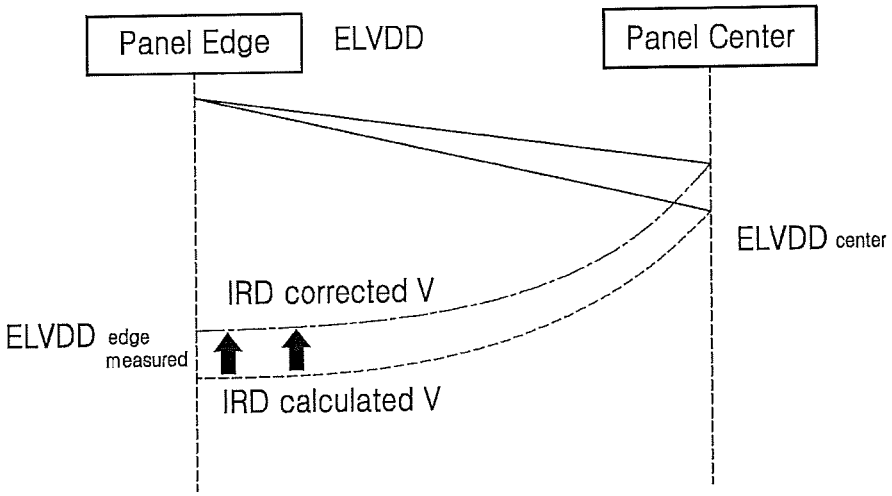

Panel Edge
ELVDD
Panel Center
ELVDD center
IRD corrected V
ELVDD edge measured
IRD calculated V

FIG. 7

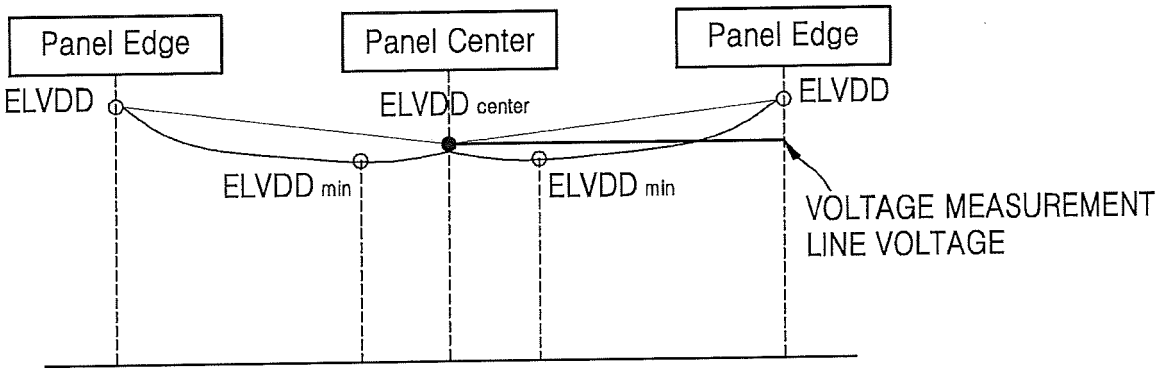

Panel Edge
Panel Center
Panel Edge
ELVDD
ELVDD center
ELVDD
ELVDD min
ELVDD min
VOLTAGE MEASUREMENT
LINE VOLTAGE

FIG. 8

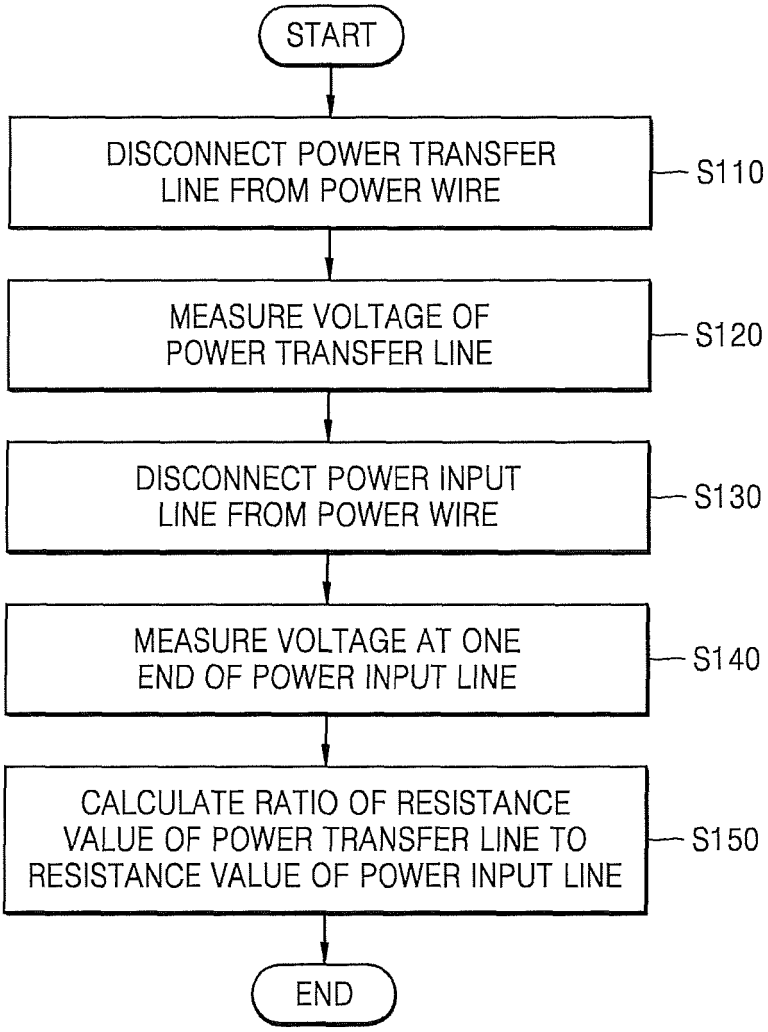
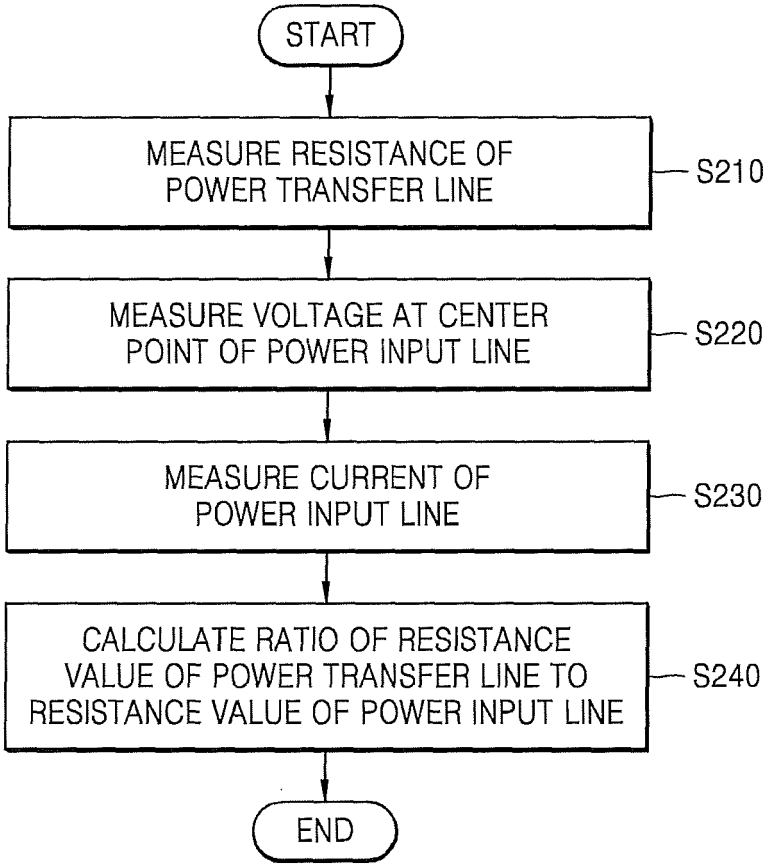

START
DISCONNECT POWER TRANSFER LINE FROM POWER WIRE
S110
MEASURE VOLTAGE OF POWER TRANSFER LINE
S120
DISCONNECT POWER INPUT LINE FROM POWER WIRE
S130
MEASURE VOLTAGE AT ONE END OF POWER INPUT LINE
S140
CALCULATE RATIO OF RESISTANCE VALUE OF POWER TRANSFER LINE TO RESISTANCE VALUE OF POWER INPUT LINE
S150
END

FIG. 9


START
MEASURE RESISTANCE OF POWER TRANSFER LINE
S210
MEASURE VOLTAGE AT CENTER POINT OF POWER INPUT LINE
S220
MEASURE CURRENT OF POWER INPUT LINE
S230
CALCULATE RATIO OF RESISTANCE VALUE OF POWER TRANSFER LINE TO RESISTANCE VALUE OF POWER INPUT LINE
S240
END

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- US 2014368416 A1 **[0005]**